PRELIMINARY

# 28F400BV-T/B 4-MBIT (256K x 16, 512K x 8) SmartVoltage BOOT BLOCK FLASH MEMORY

*SmartDie™ Product Specification*

- **Intel SmartVoltage Technology**
  - 5V or 12V Program/Erase
  - 3.3V or 5V Read Operation
  - 60% Faster Typical Programming at 12V $V_{PP}$
- **Very High Performance Read**
  - 5V: 80 ns Max. Access Time, 40 ns Max. Output Enable
  - 3V: 150 ns Max. Access Time, 90 ns Max. Output Enable
- **Low Power Consumption**
  - Maximum 60 mA Read Current at 5V
  - Maximum 30 mA Read Current at 3V
- **x8/x16-Selectable Input/Output Bus**
  - 28F400 for High Performance 16- or 32-bit CPUs
- **Optimized Array Blocking Architecture**
  - One 16-KB Protected Boot Block
  - Two 8-KB Parameter Blocks
  - One 96-KB Main Block
  - Three 128-KB Main Blocks
  - Top or Bottom Boot Locations
- **Absolute Hardware-Protection for Boot Block**
- **Software EEPROM Emulation with Parameter Blocks**
- **Extended Cycling Capability**
  - 100,000 Block Erase Cycles (Commercial Temperature)
- **Automated Word/Byte Write and Block Erase**
  - Industry Standard Command User Interface
  - Status Registers
  - Erase Suspend Capability
- **SRAM-Compatible Write Interface**
- **Automatic Power Savings Feature**
  - 1 mA Typical $I_{CC}$ Active Current in Static Operation
- **Reset/Deep Power-Down Input**
  - 0.2 µA $I_{CC}$ Typical
  - Provides Reset for Boot Operations
- **Hardware Data Protection Feature**
  - Erase/Write Lockout during Power Transitions
- **ETOX™ IV Flash Technology**
- **Intel SmartDie Product**
  - Full AC/DC Testing at Die Level
  - 0°C to +80°C (Junction) Temperature Range

**NOTICE:** This document contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

**REFERENCE INFORMATION:** The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Refer to the Standard Package Data Sheet/Book (Order No. 290530) for additional product information and specifications not found in this document.

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# 28F400BV-T/B 4-MBIT (256K x 16, 512K x 8) SmartVoltage BOOT BLOCK FLASH MEMORY

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## 1.0 DIE SPECIFICATIONS

Figure 1 shows an actual die photo; Figure 2 shows the die/bond pad layout in the same orientation as the die photo. Table 1 (pg. 3) shows X/Y coordinates of all bond pads.

**Figure 1. 28F400BV 4-MBIT (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Die Photo**

## 1.1 Pad Description

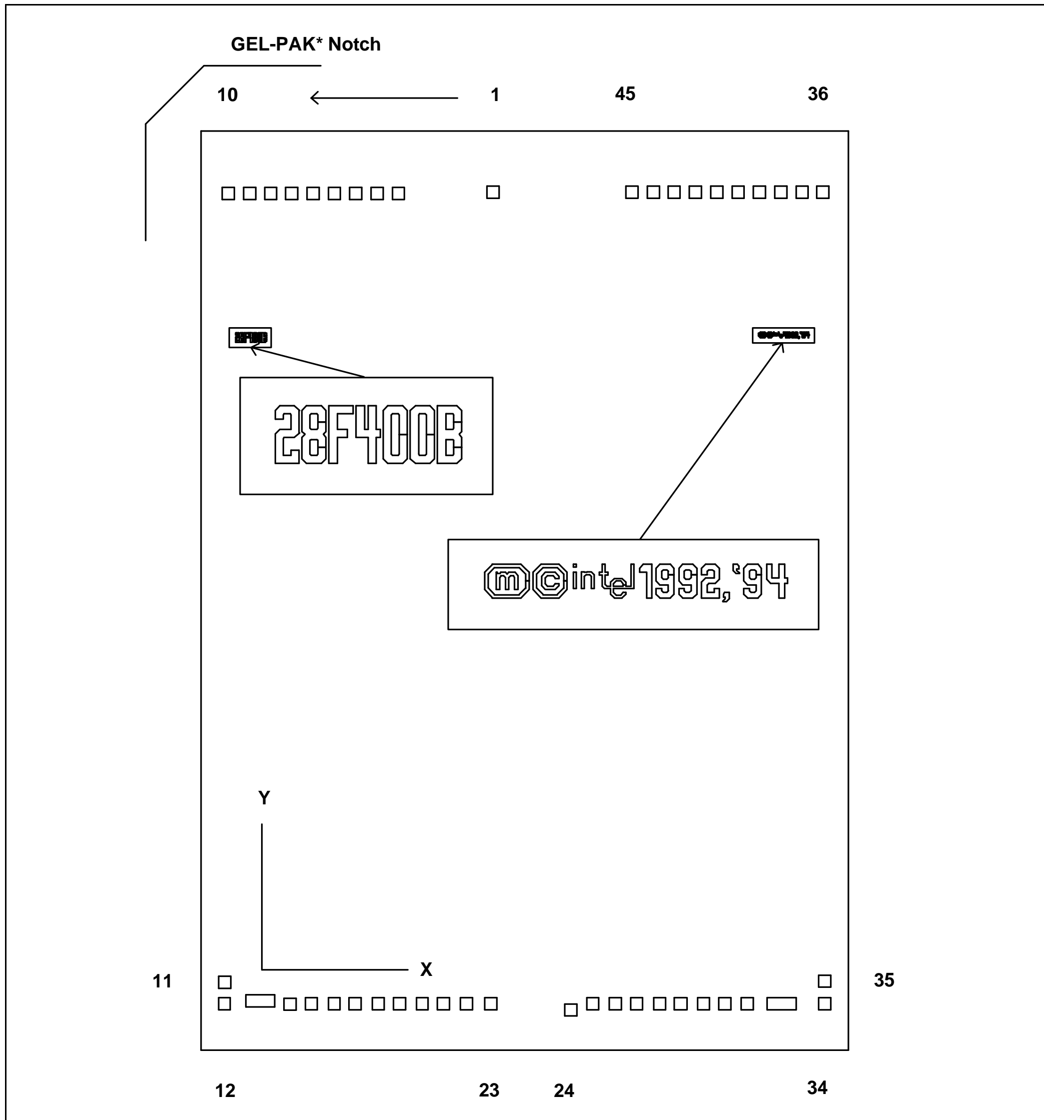


Figure 2. 28F400BV 4-MBIT (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Die/Bond Pad Layout

**Table 1. 28F400BV 4-MBIT (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Bond Pad Center Data** (Sheet 1 of 2)

| PAD# | SIGNAL | Pad Center | | | |
|---|---|---|---|---|---|
| | | Mils (=.001 inch) | | Microns | |
| | | X | Y | X | Y |
| 001 | VPP | -11.0 | 136.6 | -279 | 3469 |
| 002 | WP# | -43.4 | 136.2 | -1102 | 3460 |
| 003 | A17 | -50.7 | 136.2 | -1287 | 3460 |
| 004 | A7 | -58.0 | 136.2 | -1472 | 3460 |
| 005 | A6 | -65.3 | 136.2 | -1657 | 3460 |
| 006 | A5 | -72.5 | 136.2 | -1842 | 3460 |
| 007 | A4 | -79.8 | 136.2 | -2027 | 3460 |
| 008 | A3 | -87.1 | 136.2 | -2212 | 3460 |
| 009 | A2 | -94.4 | 136.2 | -2397 | 3460 |
| 010 | A1 | -101.7 | 136.2 | -2582 | 3460 |
| 011 | A0 | -102.8 | -134.3 | -2611 | -3411 |
| 012 | CE# | -102.9 | -141.6 | -2613 | -3596 |
| 013 | GND (3) | -90.6 | -140.7 | -2302 | -3574 |
| 014 | OE# | -80.4 | -141.8 | -2043 | -3601 |
| 015 | DQ0 | -73.1 | -141.6 | -1858 | -3598 |
| 016 | DQ8 | -65.3 | -141.6 | -1660 | -3598 |
| 017 | DQ1 | -58.1 | -141.6 | -1475 | -3598 |
| 018 | DQ9 | -50.2 | -141.6 | -1276 | -3598 |
| 019 | DQ2 | -43.0 | -141.6 | -1091 | -3598 |
| 020 | DQ10 | -35.1 | -141.6 | -893 | -3598 |
| 021 | DQ3 | -27.9 | -141.6 | -708 | -3598 |
| 022 | DQ11 | -20.1 | -141.6 | -509 | -3598 |
| 023 | VCC | -11.7 | -141.6 | -296 | -3598 |
| 024 | VCC0 | 15.7 | -143.8 | 400 | -3654 |
| 025 | DQ4 | 23.2 | -141.6 | 590 | -3598 |
| 026 | DQ12 | 31.0 | -141.6 | 788 | -3598 |
| 027 | DQ5 | 38.3 | -141.6 | 973 | -3598 |
| 028 | DQ13 | 46.1 | -141.6 | 1172 | -3598 |
| 029 | DQ6 | 53.4 | -141.6 | 1357 | -3598 |
| 030 | DQ14 | 61.2 | -141.6 | 1555 | -3598 |
| 031 | DQ7 | 68.5 | -141.6 | 1740 | -3598 |

**Table 1. 28F400BV 4-MBIT (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Bond Pad Center Data** (Sheet 2 of 2)

| PAD# | SIGNAL | Pad Center | | | |
|---|---|---|---|---|---|
| | | Mils (=.001 inch) | | Microns | |
| | | X | Y | X | Y |
| 032 | DQ15/A-1 | 76.3 | -141.6 | 1938 | -3598 |
| 033 | GND (3) | 88.0 | -141.6 | 2235 | -3597 |
| 034 | BYTE# | 102.8 | -141.6 | 2611 | -3596 |
| 035 | A16 | 102.8 | -133.9 | 2611 | -3400 |
| 036 | A15 | 102.2 | 136.6 | 2596 | 3469 |
| 037 | A14 | 94.9 | 136.6 | 2411 | 3469 |
| 038 | A13 | 87.6 | 136.6 | 2226 | 3469 |
| 039 | A12 | 80.3 | 136.6 | 2041 | 3469 |
| 040 | A11 | 73.1 | 136.6 | 1856 | 3469 |
| 041 | A10 | 65.8 | 136.6 | 1671 | 3469 |
| 042 | A9 | 58.5 | 136.6 | 1486 | 3469 |
| 043 | A8 | 51.2 | 136.6 | 1301 | 3469 |
| 044 | WE# | 43.9 | 136.6 | 1116 | 3469 |
| 045 | RP# | 36.6 | 136.6 | 931 | 3469 |

**NOTES:**

1. The symbol “#” is used at the end of the signal to denote an active low signal.
2. X-Y pad coordinates represent bond pad centers and are relative to the center of the die.
3. Double-wide bond pad.

## 2.0 INTEL DIE PRODUCTS PROCESSING

### 2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie™ products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

### 2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

### 2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

### 2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that moves the good die to GEL-PAKs*. The good die are submitted to the same visual inspection as standard packaged product. After visual inspection GEL-PAKs are packed for shipment.

### 2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

**NOTE:**

GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

### 2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

### 2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

### 2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

## 3.0 SPECIFICATIONS

Specifications within this data sheet are specific to a particular die stepping and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

## 3.1 Handling Requirements

Two key areas of concern for the 28F400BV product are:

- It is recommended that Flash devices are NOT exposed to ultraviolet (UV) light. Exposure to UV light — in addition to erasing data in the memory array — also erases the device-specific control information stored on-chip.
- Avoid exposure to temperatures above 350° C for more than 10 minutes. Operation above this time/temperature may cause damage to the device reference calls.

## 3.2 Physical Specifications

**Table 2. 28F400BV 4-MBIT (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Physical Specifications**

| | |
|---|---|
| **Die Revision:** | B-0 |
| **Post-Saw Die Dimensions:** | Mils: X = 221 ± 0.5, Y = 314 ± 0.5<br>See associated Die/Bond Pad Layout for X, Y orientation. |
| **Die Thickness:** | 17 ± 1.0 mils |
| **Minimum Pad Pitch:** | Pads are not evenly pitched.<br>Minimum pitch is 185 microns (7.3 mils). |
| **Pad Passivation Opening Size:** | Mils: 4.1 x 4.1 (Single pads)<br>Microns: 105 x 105 (Single pads)<br>Mils: 10.0 x 4.1 (Double pads)<br>Microns: 253 x 105 (Double pads) |
| **Bond Pad Metallization:**<br>(outermost layer first) | 0.9 microns Aluminum (0.5% copper)<br>0.1 micron Titanium |
| **Pads per Die:** | 45 |
| **Die Backside Material:**<br>(outermost layer first) | Polished bare silicon. |
| **Passivation:**<br>(outermost layer first) | 2.3 microns B-Pyrox, 1.5 microns Oxynitride |
| **Intel Fabrication Process:** | ETOX™ IV (min. feature size 0.6 microns) |
| **Substrate Bias Condition:** | Float (Self-biasing to $V_{SS}$). Alternative is to drive $V_{SS}$. |

## 3.3 DC Specifications

**ABSOLUTE MAXIMUM RATINGS**[1]

GEL-PAK Storage Temperature ...................... 0°C to +70°C
Junction Temperature Under Bias ........................... see note
Voltage wrt. $V_{SS}$ ..................................................... see note
Voltage on other pads ............................................ see note

**NOTE:**

1. For absolute maximum rating values, refer to the 4 MBIT (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Data Sheet, Order No. 290530.

**NOTICE**: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

***WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### 3.3.1 OPERATING CONDITIONS*

**Table 3. Operating Conditions**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $T_j$ | Operating Temperature | 0 | 80 | °C | |
| $V_{CC}$ | 3.3V $V_{CC}$ Supply Voltage (±0.3V) | 3.0 | 3.6 | V | |
| | 5V $V_{CC}$ Supply Voltage (10%) | 4.50 | 5.50 | V | 1 |

**NOTE:**

1. 10% $V_{CC}$ specifications apply to the 80 ns product versions in standard test configuration.

## 4.0 DEVICE NOMENCLATURE

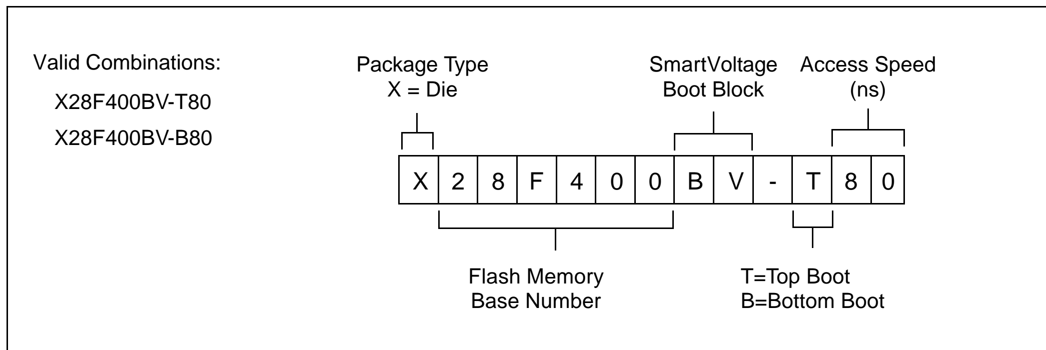


**Figure 3. Available Options and Designators**

## 5.0 REFERENCE INFORMATION

| Document Title | Order # |
|---|---|
| AB-60 *2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family* Application Brief | 292154 |
| AP-604 *Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM* Application Note | 292148 |
| Standard Package Data Sheet/Book | 290530 |

## 6.0 REVISION HISTORY

| Revision | Date | Description |
|---|---|---|
| -001 | 10/95 | Initial Release |
| -002 | 1/96 | Dropped support of 120/180 ns @ 5 V/3.3 V. Reworded section 2.4 Die Inspection. |