IXF3208

Octal T1/E1/J1 Framer with On-Chip PRM

Advance Information Datasheet

The Intel® IXF3208 with On Chip PRM is an octal framer for T1/E1/J1 and ISDN primary rate interfaces operating at 1.544 Mbps or 2.048 Mbps. Each framer consists of a receive and transmit framer, receive and transmit slip buffer. Each of the eight framers operates independently, allowing each channel to be individually configured for T1, E1, or J1 operation through software. The Intel® IXF3208 interfaces directly with the Intel® LXT3108 Octal T1/E1/J1 Long-Haul Short-Haul Line Interface Unit or the Intel® LXT384 Octal T1/E1/J1 Short-Haul Line Interface Unit. To comply with both ANSI T1.231, T1.403 and ETSI G.821 specifications, comprehensive performance monitoring is done on-chip providing Intel On-chip Performance Report Messaging (Intel PRM). The PRM collects 18 parameters every second, 15 minutes and 24 hours. The Intel IXF3208 is the ideal framer for voice and data applications as it incorporates 24 independent HDLC controllers that can be allocated to any time slot in the 8 T1/E1/J1 links it supports. This greatly simplifies the implementation of scalable GR-303 and V5.2 interfaces. GR-303 and V5.2 are interface standards to a digital switching facility comprised by multiple T1/E1/J1 links. The Intel IXF3208 has an 8 bit microprocessor bus supporting both Intel and Motorola interface. A flexible TDM interface supports bus rates from 1.544 MHz to 16.384 MHz and industry-standard buses including MVIP, HMVIP, H100, CHI etc. The Intel IXF3208 is available in a 17x17 mm PBGA package to enable the design of high-port density, multi-service line cards.

Applications

- Voice over packet gateways
- Integrated Multi-service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse multiplexing for ATM (IMA)
- Wireless base stations
- Routers
- Frame relay access devices, CSU/DSU equipment

Product Features

- Intel Performance Report Message (PRM) per T1.231 T1.403 and ITU G.826 is done on-chip offloading the system CPU and speeds development by gathering and building the performance monitoring database, which is an essential part of the network reliability data.
- Framer support for T1: SF, ESF, SLC96, J1-12, J1-24. E1: G.704, G.706, FAS/NFAS, CAS, CRC-4-CAS, CRC4.
- Separate or multiplexed system bus operating at either 1x, 2x, 4x, 8x of the data rate.
- FDL and DDL support. HDLC formatting for FDL or transparent mode.
- BERT generators and analyzers for extensive testing on chip.
- 24 HDLC controllers on chip allow compliance to V5.1, V5.2 and GR-303 specifications. Frame relay applications can be designed without the use of external HDLC controllers.

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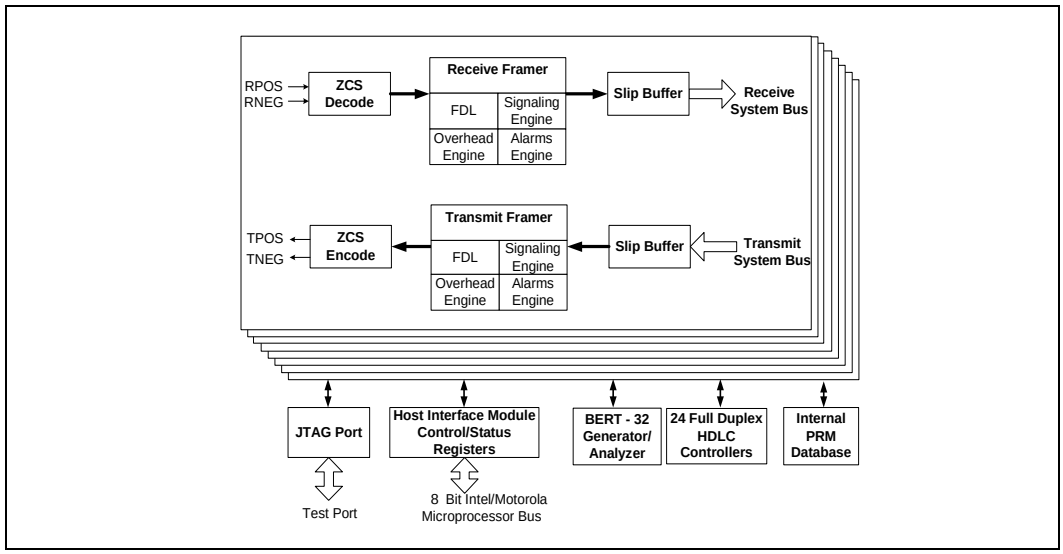
Figure 1. IXF3208 Block Diagram



1.0 Introduction

The IXF3208 is an eight-channel framer for T1/E1/J1 and Integrated Service Digital Network (ISDN) primary rate interfaces operating at 1.544 Mbps or 2.048 Mbps. All framers are completely independent and each port can be configured for either T1/E1/J1 operation. An 8 bit microprocessor interface is provided that supports both Intel® and Motorola microprocessors. The internal registers are directly addressable through the microprocessor interface. Extensive support to the data link channels (SLC96 DDL, FDL, Sa bits, CCS) is also provided.

IXF3208 offers on-chip Performance Report Message (PRM). The on-chip PRM processing is done automatically with data stored on the device. The internal database with performance monitor units (accessible by a host) provides status and performance parameters already integrated and filtered according to the available configurations. This feature offloads the external processor from the handling of the parameters associated with the functions of this device.The standards supported are ANSI T1.231 (T1) and ITU G.826 (E1). Support is also provided for ETSI ETS 300 011 and ETS 300 233.

Each of the channels supports T1-D4 SF, T1-ESF, T1-SLC96, J1-12, J1-24, E1-FAS/NFAS, E1-CRC4, E1-CAS, E1-CRC4/CAS, G.704, and G.706 frame structures. CRC inter-working is also supported.

Each port is independent in timing and format from the others. For plesiochronous applications independent two-frame deep slip buffers are provided in both transmit and receive directions. Smaller elastic store depths are available for minimum delay applications.

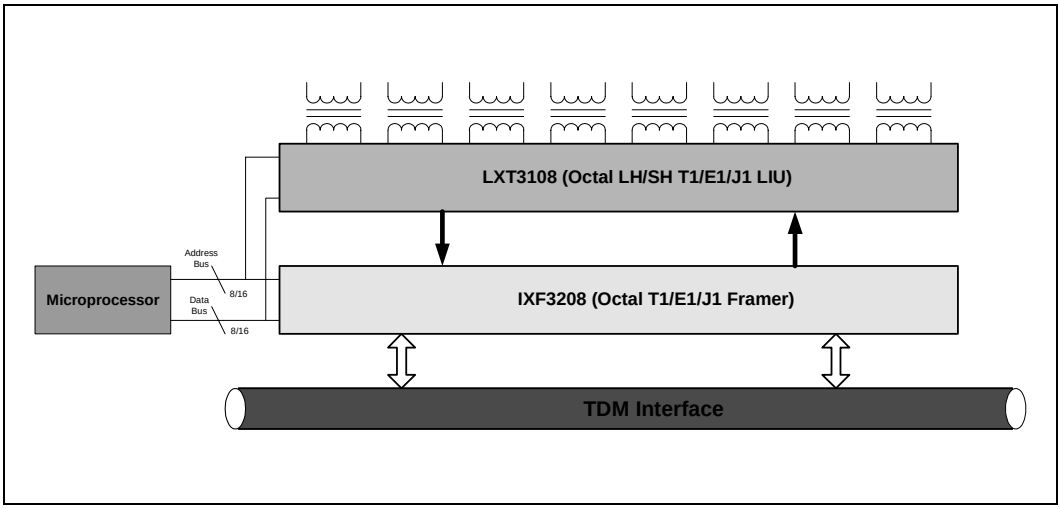
The system back-plane can be configured to handle different rates and waveforms. The back-plane has data, signaling, and framing indication pins. The clock can be run at speeds of 1x, 2x, 4x, and 8x of the data rate. The Time Division Multiplexing (TDM) highway can be configured to handle different industry standard buses such as MVIP, HMVIP, IOM/GCI, CT-Bus (H.100), SCSA (S.100), and CHI bus interfaces. Gapped clock for fractional T1/E1 applications is also supported.

Test and diagnostic functions are provided through a full set of loopbacks and a Bit Error Rate Test (BERT) module. Local Loopback, Dual Loopback, Payload Loopback, Line Loopback, and per-time slot loopbacks are available. The BERT module can handle simultaneously 8 generators and analyzers. Any generator and analyzer is available for each port and can be set to any time slot or set of time slots. Subrate testing is also available using a mask to define which bits in the time slots are tested. The generators and analyzers can be set to operate on either the line or system sides.

Signaling support, robbed bit, and TS16CAS are provided for all eight ports. Signaling information is available either from the system back-plane bus or from a table that can be accessed by the external host. The signaling at the Tx direction on the system back-plane can be sent to the line side. Also, the user can set a table of signaling values to be sent in any direction. The freeze and de-bouncing functions are programmable. Two, four, nine and sixteen signaling states are available.

Alarms and error conditions at DS1/E1 levels are detected and reported. These include AIS, LOS, yellow, and TS16 AIS. Integration times are applied to the detected defects in order to provide the failure indications (LOS, LOF, AIS, RAI failures). TDM blanking, AIS, Digital milliwatt, and DRS codes can be sent to either the line or system backplane.

Figure 2. LXT3108/IXF3208 PRI



2.0 Pin Description

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
	Line Side		
C3	RCLK8	I	Clock from LIU.
D2	RCLK7	I	
B16	RCLK6	I	
A14	RCLK5	I	
R13	RCLK4	I	
T16	RCLK3	I	
N3	RCLK2	I	
T3	RCLK1	I	
B3	RPOS8	I	Receive POS data from LIU.
D3	RPOS7	I	
C14	RPOS6	I	
A13	RPOS5	I	
T13	RPOS4	I	
R15	RPOS3	I	
R1	RPOS2	I	
T4	RPOS1	I	
A2	RNEG8	I	Receive NEG data from LIU.
C1	RNEG7	I	
C15	RNEG6	I	
C13	RNEG5	I	
P12	RNEG4	I	
T15	RNEG3	I	
P2	RNEG2	I	
R4	RNEG1	I	
C2	TCLK8	O	Clock to LIU.
E2	TCLK7	O	
D15	TCLK6	O	
B15	TCLK5	O	
R14	TCLK4	O	
N14	TCLK3	O	
N2	TCLK2	O	
R2	TCLK1	O	
A1	TPOS8	O	Transmit POS data to LIU.
E3	TPOS7	O	
D14	TPOS6	O	
A15	TPOS5	O	
T14	TPOS4	O	
R16	TPOS3	O	
P3	TPOS2	O	
T2	TPOS1	O	

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
B2	TNEG8	O	Transmit NEG to LIU.
D1	TNEG7	O	
C16	TNEG6	O	
B14	TNEG5	O	
P13	TNEG4	O	
P15	TNEG3	O	
P1	TNEG2	O	
R3	TNEG1	O	
	Backplane Side		
T12	BRCLK8	I/O	Receive clock at the back-plane.
K15	BRCLK7	I/O	
H12	BRCLK6	I/O	
F14	BRCLK5	I/O	
E10	BRCLK4	I/O	
C8	BRCLK3	I/O	
C6	BRCLK2	I/O	
D4	BRCLK1	I/O	
R11	BRDATA8	O	Receive data at the back-plane.
K14	BRDATA7	O	
H13	BRDATA6	O	
F13	BRDATA5	O	
B11	BRDATA4	O	
A8	BRDATA3	O	
A6	BRDATA2	O	
B4	BRDATA1	O	
P11	BRFP8	I/O	Receive frame pulse at the back-plane.
L16	BRFP7	I/O	
H16	BRFP6	I/O	
F15	BRFP5	I/O	
D11	BRFP4	I/O	
D8	BRFP3	I/O	
C7	BRFP2	I/O	
A3	BRFP1	I/O	
T11	BRMFP8	O	Receive multi-frame pulse at the back-plane.
M16	BRMFP7	O	
J13	BRMFP6	O	
F16	BRMFP5	O	
A11	BRMFP4	O	
D9	BRMFP3	O	
B7	BRMFP2	O	
C5	BRMFP1	O	

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
P10	BRSIG8	O	Rx signalling at the back-plane.
M13	BRSIG7	O	
J15	BRSIG6	O	
G15	BRSIG5	O	
C11	BRSIG4	O	
C9	BRSIG3	O	
D6	BRSIG2	O	
B5	BRSIG1	O	
R10	BTCLK8	I/O	Transmit clock at the back-plane.
N13	BTCLK7	I/O	
J14	BTCLK6	I/O	
G16	BTCLK5	I/O	
D13	BTCLK4	I/O	
B9	BTCLK3	I/O	
E7	BTCLK2	I/O	
A4	BTCLK1	I/O	
T10	BTDATA8	I	Transmit data at the back-plane.
M14	BTDATA7	I	
J16	BTDATA6	I	
G14	BTDATA5	I	
A12	BTDATA4	I	
A9	BTDATA3	I	
A7	BTDATA2	I	
A5	BTDATA1	I	
T9	BTFP8	I/O	Transmit frame pulse at the back-plane.
L15	BTFP7	I/O	
L13	BTFP6	I/O	
G13	BTFP5	I/O	
B12	BTFP4	I/O	
D10	BTFP3	I/O	
D7	BTFP2	I/O	
D5	BTFP1	I/O	
P9	BTMFP8	I	Transmit multi-frame pulse at the back-plane.
L14	BTMFP7	I	
K13	BTMFP6	I	
H14	BTMFP5	I	
C12	BTMFP4	I	
C10	BTMFP3	I	
E8	BTMFP2	I	
E6	BTMFP1	I	

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
R9	BTSIG8	I	Tx signaling at the back-plane.
M15	BTSIG7	I	
K16	BTSIG6	I	
H15	BTSIG5	I	
D12	BTSIG4	I	
B10	BTSIG3	I	
B8	BTSIG2	I	
B6	BTSIG1	I	
C4	ALOS8	I	Loss of Signal Indicator from LIU.
B1	ALOS7	I	
A16	ALOS6	I	
B13	ALOS5	I	
R12	ALOS4	I	
N11	ALOS3	I	
T1	ALOS2	I	
P4	ALOS1	I	
	Host Side		
G2	ADR15	I	Microprocessor address lines.
G1	ADR14	I	
G3	ADR13	I	
H4	ADR12	I	
H1	ADR11	I	
H3	ADR10	I	
H2	ADR9	I	
J1	ADR8	I	
J3	ADR7	I	
K1	ADR6	I	
J2	ADR5	I	
J4	ADR4	I	
K4	ADR3	I	
K3	ADR2	I	
L1	ADR1	I	
K2	ADR0	I	
N1	DB7	I/O	Microprocessor data bus.
M3	DB6	I/O	
M2	DB5	I/O	
N4	DB4	I/O	
M1	DB3	I/O	
L3	DB2	I/O	
M4	DB1	I/O	
L2	DB0	I/O	
N12	INTELMOT	I	Intel = 1, Motorola = 0.
F1	MOTOTYPE	I	MPC860 = 0, MC68302 = 1.
F3	CSB	I	Chip select, active low.
N16	RWB	I	Read = 1, Write = 0.

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
N15	RDYB	O	Ready signal, active low.
P16	INTB	O	Hardware interrupt output.
F2	WEB	I	Write enable, active low (for MPC860).
P14	DSB	I	Data strobe, active low.
	Clock References		
P5	E1x24	I	Clock input to be used to generate E1 rates locked to the reference with jitter removed.
T5	T1x24	I	Clock input to be used to generate T1 rates locked to the reference with jitter removed.
	System Clock		
E1	SYSCLK	I	The system clock used for the internal state machines. Typically a 33 MHz clock.
R6	RESETB	I	Master hardware reset, active low.
	Clock Outputs		
R5	REFCLK	O	Reference clock that can be taken from any of the Rx lines or the internal circuitry.
	JTAG		
E15	TMS	I	JTAG Test Mode.
E14	TCK	I	JTAG clock.
D16	TDI	I	JTAG data input.
E13	TDO	O	JTAG data output.
E16	TRSTB	I	JTAG reset, active low.
	Test		
R7	TESTENB	I	Normal operation = 1, Scan mode = 0.
P7	SCANEN	I	
T7	TRISTB	I	Normal operation = 1, Tristate all outputs = 0.
P6	ARCTMSB	I	ARC Test.
T6	ARCTDO	O	ARC Test port.
P8	TDRIN	I	Reserved.
R8	TDROUT	O	Reserved.
H6			Reserved (This pin must be a No Connect).
T8			Reserved (This pin must be a No Connect).

Table 1. IXF3208 Ball Description

PBGA	Ball Name	I/O	Description
A10, E4, E5, E12, F4, F8, F9, F11, F12, G4, G6, G7, G8, G9, G10, G11, H5, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, K12, L4, L5, L6, L7, L8, L9, L10, L11, M5, M11, M12, N5, N6, N7, N8, N9, N10	VSS		Ground.
F5, F7, F10, G12, J12, K5, M7, M9	VDD_IO		Connect to 3.3V power supply.
E9, E11, F6, G5, J5, L12, M6, M8, M10	VDD_CORE		Connect to 1.8V power supply.

3.0 T1/E1 Nomenclature

The nomenclature in this document follows telecommunication industry standard conventions, i.e., bit, channel (timeslot), and frame numbering increase sequentially with time. In the case of bit ordering, unless otherwise stated, the Most Significant Bit (MSB) is transmitted first and is designated Bit 1.

Both T1 and E1 conventions define the numbering of bits within a timeslot to be designated “Bit 1” through “Bit 8,” with Bit 1 defined as the MSB.

The T1 convention is to sequentially number channels (timeslots) beginning with “1”, i.e., the first channel in a T1 frame is frame number 1. The E1 convention is to number this timeslot “0”, i.e., the first timeslot in a E1 frame is timeslot number 0.

In multiframe structures, the T1 convention is to sequentially number frames beginning with “1”, i.e. the first frame in a T1 multiframe is frame number 1. The E1 convention is to number this frame “0”, i.e., the first frame in a E1 multiframe is frame number 0.

T1 bits within a frame are numbered from 1 to 193, with bit 1 being the “F’ (framing) bit. E1 bits within a frame are numbered from 0 to 255, with bits 1 to 8 occupying the FAS/NFAS Word timeslot (timeslot 0).

In T1 terminology, “Yellow Alarm” and “Remote Alarm Indication” (RAI) are synonymous. Also, “Blue Alarm” and “Alarm Indication Signal” (AIS) are synonymous.

The terms “Out of Frame” (OOF) and “Loss of Frame” (LOF) are used interchangeably in this document.

4.0 IXF3208 Nomenclature

The IXF3208 is an octal device, meaning that it supports up to eight T1/E1/J1 links. The links are numbered sequentially, beginning with one (1) and ending with eight (8). The time slots are numbered 1 to 24 for T1 cases and 0 to 31 for E1 cases. Please note that T1 channel 1 corresponds to TS0, channel 2 to TS1, etc.

A link is defined as the standard 4-wire receive/transmit pair T1/E1/J1 interface. The terms *link*, *port*, and *span* may be used interchangeably in this document.

5.0 Feature Set

Table 2. IXF3208 Feature Set - General

Feature	Description
Operating Voltage	1.8 ± .18 and 3.3 ± 0.3 Volts
Operating Temperature	-40°C to 85°C
I/O type	5 Volt tolerant IO, CMOS/TTL Compatible - TTL input thresholds.
Packaging[1]	17 x 17 mm 256 PBGA
External Timing Reference	Only one timing signal, system clock, is required for T1, E1 or J1 operation.
Power Consumption	TBD
Boundary Scan (JTAG)	Built-in self test enabled via µP register bits per IEEE 1149.4.
BIST	Self test is available for RAMs.

Table 3. Line and Framing

Feature	Description
Interface	Bipolar: POS, NEG, CLK Unipolar: NRZ, CLK
Line Coding	T1: Selectable AMI (per ANSI T1.102) B8ZS (per ANSI T1.102) ZCS (bit 7) E1: Selectable AMI (per ITU G.703) HDB3 (per ITU G.703)
Line Monitoring	T1 – Maskable interrupt generated for all conditions. AIS - Alarm Indication Signal. A ones density of at least 99.9% in a window of 3 ms to 75 ms. (Per ANSI T1.231 and ITU G.775). BPV - Bipolar violation EXZ - Excess zero detection LOS - Loss of signal: 175 ± 75 clocks with no pulse transitions (per ANSI T1.231). E1 - Maskable interrupt generated for all conditions AIS - Alarm Indication Signal. Two or less 0s in a windows of 512 bits (per ITU G.775) BPV - Bipolar Violation Detection. Two consecutive marks of the same polarity. HDB3 – Two consecutive BPVs of the same polarity. LOS - Loss of signal: N consecutive intervals with no pulse transitions, where N is in the range of 10 to 255 (per ITU G.775).
Framing modes	T1: D4-SF (per ANSI T1.107, T1.403) ESF (per ANSI T1.107, T1.403) SLC96 (per Bellcore TR-TSY-008, GR-303) E1: FAS/NFAS double frame (per ITU G.704, G.706) CRC-4 Multiframe (per ITU G.704, G.706) CAS multiframe (per ITU G.704, G.706, G.732) CRC4 and CAS multiframe (per ITU G.704, G.706, G.732) J1: J1 12 frame multiframe (per JT G.703, JT G.704, JT G.706, I.431) J1 24 frame multiframe (per JT G.703, JT G.704, JT G.706, I.431) Transparent: The device does not search or generate framing information. T1 or E1 transparent. If a frame pulse is generated or received at the backplane it must follow the T1 or E1 frame duration (193 or 256 bits).

Table 3. Line and Framing

Feature	Description
Maximum average reframe time	T1 – D4 SF 5 ms (per G.704) T1 – ESF 15 ms (per G.706) T1 – SLC96 50 ms (per G.706) J1 – D4 SF 5 ms (per PUB 43801) J1 – ESF 15 ms (per G.706) E1 – FAS/NFAS E1 – CRC4 E1 – CAS E1 – CRC4/CAS
False framing protection	T1 - D4 SF: Ft coupled with Fs framing bits. T1- ESF: Fe framing bits coupled with CRC-6 error detection bits. T1- SLC96: Ft framing bits coupled with Fs bits plus DDL spoiler bits. E1 - CRC4: FAS/NFAS coupled with CRC4 sync sequence. CRC4 calculation also checked.
Out of Frame conditions	Out of frame detection (OOF) - Maskable interrupt generated. Resynchronization Automatic or manual resynchronization upon detection of OOF condition. Change of Frame Alignment (COFA) Latest receiver synchronization results in a change of frame or multiframe alignment. T1 D4: out of frame is forced when there are M errors in a programmable window of N consecutive Ft or Fs bits. N= 1,2,...,7, M= 1,2,...,7 T1 ESF: out of frame is forced when there are M errors in a programmable window of N consecutive Fe bits. M, N= 1,2,...,7 If the number of CRC6 errors exceed 320 in a one second this will also force reframe (optional). E1 Doubleframe: three consecutive errors in FAS or three consecutive errors in NFAS. E1 CAS: two consecutive CAS multiframe alignment words received in error. E1 CRC: two consecutive errors in FAS or two consecutive errors in NFAS. If 915 or more CRC errors are detected in a one second window then the reframe process is started. E1 CRC: if N errors in a window of M bits occur, loss of CRC can be declared (optional) .
CRC of T1 ESF and E1 CMF disabling	CRC checking/generation can be disabled. The CRC bits can be taken from the back-plane data.

Table 4. Slip Buffers

Feature	Description
Slip Buffers	Separate slip buffers for both the receive and transmit paths. Always engaged, the options are Minimum delay or Two Frames. Read and Write pointer can be accessed (read and write) from external host. Slip indication Slip direction indication Pointer separation indication (RdPtr – WrPtr)

Table 5. Signaling

Feature	Description
Signaling	T1/J1-Robbed bit signaling D4 SF – Two or Four states, A or AB bits ESF -- Two, Four or Sixteen states A, AB or ABCD bits SLC96 – Two, Four or Nine states A, AB or AB+toggling T1/E1/J1 Common Channel Signaling (CCS) Available using FDL module. E1 Channel Associated Signaling (CAS) On TS16 (per ITU G.704) T1/E1/J1: Signaling Freeze per DS1/E1 Triggered by loss of Frame conditions. (LOS, AIS, OOF, OOCAS) Signaling Debounce Disable or two multiframes Signaling forced by the host The external host can define the signaling to Tx in each direction This value is kept until the host changes it or releases it Signaling access Signaling can be accessed through the microprocessor port or on the signaling bus Signaling Change Indicators per DS0

Table 6. Data Links

Feature	Description
T1 data links	SLC96 Derived Data Link (per Bellcore TR-TSY-008). ESF Facility Data link (FDL) (per ANSI T1.403 and Bellcore TR-TSY-499). ESF Facility Data Link (FDL) (per AT&T TR 54016).
E1 Data Links	TS0 Sa4 bit data link (M chanel0 (per ITU I.431 and G.962 (ETS 300 233). Any combination of Sa(4:8) bits is allowed. CCS available by selecting any TS.

Table 7. T1 Performance Monitoring

Feature	Description
Compliance	ANSI T1.231, T1.403
PRM	Automatic generation and detection of one second T1.403 PRM.
Counters	15 minutes 24 hours Automatic integration and parameterization of primitives and alarms.
Performance Primitives	(per ANSI T1 231) Anomalies: Line BPV -- Bipolar Violations Pulse of the same polarity as previous pulse excluding those which are a part of the B8ZS Code. EXZ -- Excess zeroes AMI/ZCS - Any string with greater than 15 consecutive 0's B8ZS - Any string with greater than 7 consecutive 0's Optional FCC definition (per Part 68.318-1987/47CFR) Path CRC-6 -- CRC errors Any received CRC-6 code that is not identical to the corresponding locally calculated code. FE -- Frame bit errors SF - any Ft or Ft and Fs bit error ESF - any Fe Bit error CS -- Controlled slips The intentional occurrence of a replication or deletion of an entire DS1 frame to maintain framing under differing Line/System clock conditions. Change of Frame Alignment (COFA) Indication. Defects: Line LOS -- Loss of signal OOF – Out Of Frame Path SEF -- Severely Errored Seconds In SF 2 or more Ft bit errors in a 0.75 ms window (2 of 3 Ft bits in error). In ESF mode 2 or more Fe bit errors in a 3 ms window (2 of 6 Fe bits in error). AIS -- Alarm Indication Signal
Performance failures	Detected Performance Failures (per ANSI T1.231) Line Path LOS -- LOS defect for more than 2 seconds AIS -- AIS defect for more than 2 seconds LOF -- OOF defect for more than 2 seconds RAI – Remote Alarm Indication. Indicated as soon as alarm is detected
Far End Performance Reporting	(per ANSI T1.403) User controllable Automatic message assembly and Transmission. FDL PRM support in both receive and transmit directions.

Table 7. T1 Performance Monitoring

Feature	Description
Other Indicators, Signals, and Parameters	The following indicators and signals are supported. Also, the Noted Path Failure Parameters are Collected (per: ANSI T1.231). Path-Related Remote Alarm Indication (RAI) - Defined in Table 10. Selectable automatic transmission upon detection of LOF Failure. Minimum duration = 1 second. Near-End Path Failure Count parameter (FC-P) - count of number of occurrences of near-end path failure events (LOF or AIS Failure, as defined above). Far-End Path Failure Count (FC-PFE) - count of number of occurrences of far-end path failure events (RAI Failure, as defined above).
Performance parameters	The following performance parameters are collected, integrated and stored (per: ANSI T1.231). The Parameters are Accessible via the Microprocessor Interface. Line Parameters - Near End CV-L ES-L SES-L LOSS-L Line Parameters - Far End ES-LFE Path Parameters - Near End CV-P ES-P ESA-P ESB-P SES-P SAS-P AISS-P CSS-P UAS-P Path Parameters - Far End CV-PFE ES-PFE ESA-PFE ESB-PFE SES-PFE SEFS-PFE CSS-PFE UAS-PFE

Table 8. E1 Performance Monitoring

Feature	Description
Compliance	ITU G.821, G.826, o.150, ETS 300 011, ETS 300 233
Counters	15 minutes minimum storage 24 hour storage Automatic integration/parameterization of primitives and alarms
Line code violations	(per ITU O.161) AMI - Two consecutive marks of the same polarity HDB3 - Two consecutive marks of the same polarity
Performance primitives	(per ITU G.826) Near End Anomalies a_1 an errored frame alignment signal; a_2 an EB as indicated by the CRC not matching the received CRC4 Near End Defects d_1 loss of signal d_2 alarm indication signal d_3 loss of frame alignment Far End FE-a1 E bit received set (0) FE-d1 RAI is received set
Performance parameters	The following performance parameters are collected and stored (per ITU G.826). The parameters are accessible via the microprocessor interface. Events - EB -- Errored block ES – Errored second SES – Severely Errored Second BEB – Background Error Block Parameters - ESR -- Errored Seconds Ratio SESR – Severely Errored Seconds ratio BBER – Background Block Error ratio Far End Performance Monitoring - RAI FERF and FEBE
Loss of Signal (LOS)	Detection (per: ITU G.775) Distinguished from OOF Set when less than three 0's are detected in each of two consecutive double frame periods (512 Bits). Cleared when each of two consecutive double frame periods (512 Bits) contains 3 or more 0's or when the Frame Alignment Signal (FAS) has been found.
Loss of Frame Sync	(per: ITU G.704, G.706)
Out Of Frame (OOF)	(per: ITU G.704, G.706)
Change of Frame Alignment (COFA)	

Table 8. E1 Performance Monitoring

Feature	Description
Loss of signaling Multiframe Alignment	(per: ITU G.704, G.706)
Loss of CRC Multiframe Alignment	(per: ITU G.704, G.706)
CRC-4 Error (CRC)	(per: ITU G.704, G.706)
Far End Block Error (FEBE)	(per: ITU G.704, G.706)
CS (Controlled Slip)	Tx and Rx Elastic Store Frame Slip/Repeat events are reported.

6.0 Alarm and Fault Indicators

This refers to interrupt, status, counters, FIFOs or databases available to the host to convey the state of the device.

Table 9. Main T1 Indicators

Feature	Description
Out of Frame (OOF) Defect	T1 D4: Selectable on N/M frame bits (Ft&Fs or Ft only) in error. N, M = 1,2, ..7 OOF condition clears when the receiver frames T1 ESF: Selectable on N/M frame bits (Fe) in error On ESF only, 320 or more CRC6 errors.
Loss of Signal (LOS) Defect	(per ITU G.775) T1: 175 +- 75 contiguous spaces LOS clears when the average ones density is at least 12.5% over a period of 175+- 75 contiguous pulse positions (per ANSI T1.231) (per ITU I.431). Set when there are no transitions in 1 ms windows, at least. Clear occurs when the programmable ones density is met.
AIS (Alarm Indication Signal) Defect	(per ANSI T1.231 and ITU G.775) At least 99.9% of ones density in a window of 3 to 75 ms. A particular case is: Set when less than 5 zeroes are detected in a 3ms window of data. Cleared if more than 6 zeroes are detected in a 3 ms window.

Table 9. Main T1 Indicators

Feature	Description
Yellow: Remote Alarm Indication (RAI)	SF and SLC96. Normal mode Sets when bit 2 is 0 in every channel (per ANSI T1.231). Clears when the set condition is not present. Detected when 254 out of 256 TS have bit 2 set to 0?????? The minimum detect time is 335 ms??? SF Alternate mode (J1 D4 SF) Sets when 12th framing bit = 1 for two consecutive superframes. Clears when 12th framing bit = 0 for two consecutive superframe. ESF Sets when FDL BOM = 1111111100000000 occurs in 15 out of 16 contiguous pattern intervals. Cleared when the above pattern does not occur in 15 out of 16 intervals. Maskable interrupt generated. Line Transmission ESF - transmit Yellow Alarm Code on BOM of FDL.
LOF Failure (Red Alarm)	Sets when an OOF defect persists for a period of 2.5 +- 0.5 seconds. Clears when OOF has been removed for a period of 20 seconds or fewer. (per ANSI T1.231). Selectable N/M frame bits (Ft., Fs, Ft & Fs, Fe) in error. Maskable interrupt is generated.
LOS Failure	Sets when an LOS defect persists for a period of 2.5 +- 0.5 seconds. Clears when LOS has been removed for a period of 20 seconds or fewer. (per ANSI T1.231).
AIS Failure (Blue Alarm)	Sets when an AIS defect persists for a period of 2.5 +- 0.5 seconds. Clears when AIS has been removed for a period of 20 seconds or fewer. (per ANSI T1.231). Maskable interrupt is generated.
COFA	COFA is declared when the new frame location is different to the previous one.
CRC6 errors Indicator and count	CRC errors latched indicator CRC errors counter
Ft/Fe bit errors Indicator and count	Framing error indication Ft (D4) or Fe (ESF) counter
Fs bit errors Indicator and count	Fs error counter
Ft+Fs errors Indicator and count	Counter of Ft plus Fs errors
Slip Indicator and count	Slip indicator and counter
PRM detected	PRM reception indicator
MOP detected Indication plus other status info	MOP detected (it does not include PRM)
BOP Indication and count	BOP detected indicator BOP counter (number of times it has been received) Saturated counter.

Table 9. Main T1 Indicators

Feature	Description
DS0 Yellow: (DS0-RAI)	(per: Bellcore GR-253, Bellcore GR-303) Line Detection Sets when ABCD signaling Bits = 0111 for two consecutive superframes. Clears when ABCD signaling Bits do not = 0111 for four consecutive superframes. Line Transmission Force ABCD = 0111 for selected DS0
DS0 AIS:	(per: Bellcore GR-253, Bellcore GR-303) Line Detection Sets when ABCD signaling Bits = 0010 for two consecutive superframes Clears when ABCD signaling Bits do not = 0010 for four consecutive superframes Line Transmission Force ABCD = 0010 for selected DS0
Japanese Application Support	Compliance with JT-G.704: Yellow Alarm generation and detection CRC checking and transmission

Table 10. Main E1 Indicators

Feature	Description
Out of Frame (OOF) Defect	E1: Selectable to 3 FAS, or to 3 FAS or 3 NFAS consecutive words in error OOF condition clears when the receiver frames again. In E1 CRC4 mode, if there are 915 or more CRC4 errors in a one second window, then reframe is restarted (G.706).
Loss of Signal (LOS) Defect	(per ITU G.775) Set when there are no transitions in a window of 10 to 255 bit periods. Cleared when there is at least one transition in a window of 10 to 255 bit periods. (per G.775): The LOS defect is cleared when the incoming signal has "transitions", i.e. when the signal level is greater than or equal to a signal level of P dB below nominal, for N consecutive pulse intervals, where $10 \leq N \leq 255$. (per ITU I.431, ETS 300 233) Set when there are no transitions in a window of 1 ms (2048 bits). Clear occurs when the programmable ones density is met.
Blue Alarm (AIS) Defect	(per ITU G.775) Set when less than three 0s are detected in each of two consecutive double frame periods (512 bits). Cleared when each of two consecutive double frame periods (512 bits) contain three or more 0s or when the Frame Alignment Signal (FAS) has been found. On Tx the framer is forced to send an unframed all ones. ETS 300 233 Requires LOF to be present also before declaring AIS. Both conditions, LOF and the number of 0s.

Table 10. Main E1 Indicators

Feature	Description
Remote Alarm Indication (RAI)	(per ITU G.704) Set when bit 3 in timeslot 0 of NFAS =1 for one time (ETS 300 011) or N times (G.775?). Cleared when bit 3 of TS 0 in NFAS frames = 0 On Tx, bit 3 of TS0 of NFAS frames is set to 1 To support ETS 300 011 RAI is generated on every re-sync forced by the CMF (CRC Multiframe) circuitry.
Remote Multiframe Alarm (TS16 RAI)	(per ITU G.704) Set when bit 6 of TS16 of frame 0 = 1 for two consecutive multiframes. Cleared when bit 6 of TS16 of frame 0 = 0 for two consecutive multiframes. On Tx bit 6 of TS16 of frame 0 = 1
TS 16 AIS	Line detection (per ITU G.775) on both line and system side. Set when there are less than four 0s in TS16 in each of two consecutive multiframes. Cleared when each of two consecutive multiframe periods contain 4 or more 0s or when the Multiframe Alignment Signal (MFAS) has been found. Line Transmission - force transmitter to send unframed all-ones in TS-16.
TS 16 LOS	(per ITU G.732) Set when all the TS16 bytes are 0 in two consecutive multiframes. Cleared when at list a 1 is present in a TS16 preceding the multiframe alignment signal.
Red Alarm	(per G.775) Indicated when the OOF conditions exists for 100ms. Cleared when 3 or more zeroes are detected in a 512 bits period.
COFA	COFA is declared when the new frame location is different to the previous one.
AUX-P	Detected when the sequence “10” has been detected more than 253 times in a 512 bits window and the state is LOF (*per ETS 300 233*). Cleared when three or more non ‘10” patterns are found in the 512 bit window.
CRC4 errors Indicator and count	CRC4 errors indicator and count
FAS errors Indicator and count	FAS error indicator and counter
NFAS bit errors Indicator and count	NFAS error indicator and counter
FAS+NFAS errors Indicator and count	FAS+NFAS error indicator and counter
Slip Indicator and count	Slip indicator and counter
Code word Indication and count	Code word detected indicator Code word counter. It indicates the number of times the codeword has been detected
MOP detected Indication plus other status info	MOP detected MOP status, length

Table 11. IXF3208 Feature Set - Data Links

Feature	Detail
Dedicated FDL Controller	Dedicated transmit and receive FDL processor per line port Independent from HDLC processor.s
T1 Data Links	Supported Data Links: SLC96 Derived Data Link (DDL) (per: Bellcore TR-TSY-008) ESF Facility Data Link (FDL) (per: ANSI T1.403, and Bellcore TR-TSY-499) ESF Facility Data Link (FDL) (per: AT&T TR 54016) ISDN PRI D-Channel handler Support (per: Bellcore TR-TSY-754) The Data Link is accessed through the Microprocessor Interface.
E1 Data Links	Supported Data Links: TS0 Sa4 Bit Data Link (M Channel) (per: ITU I.431 and G.962 (ETS 300 233) User may select any combination of the Si bit from the FAS frame, the Si bit from the NFAS frame or any of the Sa(4:8) bits. TS16 Data Link V5.2 DLC Data Link Support (Timeslots 15, 16, 31) (per: ETS 300 347-1, ITU G.965). The Data Link is accessed through the Microprocessor Interface.

Table 12. IXF3208 Feature Set - Embedded HDLC Controller

Feature	Detail
General	Three full duplex controller, each mappable from one payload bit on any line port, up to the entire clear payload.
Data Rates	From 8 Kbps (one payload bit) up to the entire payload (minus framing and signaling bits). Consecutive/Non-Consecutive channel concatenation for H0, H11, H12 support.
Control/Access	Control via Processor Interface Access via FIFO registers Maskable Interrupts for each channel/source Programmable data transfer size (byte, word)
Applications/ Protocols Supported	ISDN LAPD/LAPB (HDLC) protocol messaging (per ITU Q.921) Integrated DLC (per: Bellcore GR-303) V5.1 & V5.2 Interfaces (per: ITU G.964/ETS 300 324, ITU G.965/ETS 300 347)
Modes	Support Modes: HDLC LAPB and LAPD protocols without procedure support. Framed Transparent: Includes starting and ending flags. Fully Transparent: without starting and ending flags.

Table 12. IXF3208 Feature Set - Embedded HDLC Controller

Feature	Detail
HDLC Features	Non-Automatic Mode Supports All LAPx protocols Programmable rate per channel: Any combination of bits, including DS0 sub-rate, DS1, H0, H11, H12 Bit oriented functions: Flag generation/recognition Address recognition Bit stuffing, zero insertion/deletion CRC generation/check Abort generation/recognition Inter-frame time fill change recognition Non octet frame content recognition Minimum frame length check and maximum frame length check and cut off
	Framed Transparent Mode Starting and ending flag of 7E generation/recognition Extraction of starting and ending flag and interframe time fill at receive side Maximum frame length check Fully Transparent Mode Bits synchronous data transmission Interframe time fill generation: 7E (flag) or programmable
FIFO Buffers	Transmit FIFO depth of 128 bytes (128 x 2 bytes) Receive FIFO depth of 128 bytes (64 x 4 bytes) FIFO status via Processor Interface

Table 13. IXF3208 Feature Set - Pattern Generator/Receiver and BER Tester

Feature	Detail
Compliance	ANSI T1.231, AT&T TR 62411, Bellcore TR-TSY-820, Bellcore TR-NWT-001219 ITU O.150, ITU O.151, ITU O.152, ITU O.153
Pattern Generation and BERT (Bit Error Rate Test)	Eight Programmable Pattern Generator and Receiver. Can be used for line and system side testing. Generator can insert selected fixed, PRBS, or User Programmable (2 to 32 Bits) patterns. All patterns support DS0 timeslot boundaries. Receiver counts mismatches between the received stream and expected pattern BERT can be performed on entire payload or on individual DS0s. Subrate support by selecting any combination of bits in the time slot. Selectable Fixed Patterns: (per: AT&T TR 62411, Bellcore TR-NWT-001219, ITU 0.150, O.151, O.152) All One's (Mark) All Zeroes (Space) Alternating Ones and Zeroes (1:1) 1 in 3 (in band loop down code) 1 in 4 (in band loop up code) 1 in 5 1 in 7 1 in 8 1 in 16 3 in 24 Selectable PRBS patterns: (per: AT&T TR 62411, Bellcore TR-NWT-001219, ITU O.150, O.151, O.152) 26-1 27-1 28-1 29-1 211-1 215-1 220-1 QRSS (220-1, with no more than 14 consecutive zeroes) 223-1
Pattern Receiver	User Programmable Pattern with Programmable Length Up to 32 Bits. Can detect Pattern Match, Inverse Pattern Match, Integrated Pattern Match.
Counters	24-bit Bit Counter 24-bit Bit Error Counter

Table 14. IXF3208 Feature Set - Interfaces

Feature	Detail
Processor Interface	Selectable 8 bit parallel data interface Multiplexed and non-multiplexed modes 16 bit address bus Supports MPC860, MPC8260 (PowerQicc2), M68302, I486 Motorola and Intel busses supported with appropriate endian support Asynchronous bus support Zero wait state operation to 33 MHz Internal wait state generator One open drain interrupt outputs Internal one second timer for performance data latching Support for interrupt-driven, polled, or mixed access architectures
Line Interface	Types: Bipolar data (POS & NEG) and clock NRZ data and clock Independent clock and data inputs/outputs for each channel
System Interface: General Features	Non-multiplexed or N-Channel multiplexed operation (N = 1, 2, 4 or 8) Byte replication in multiplexed Mode Clock source selection for each port Programmable clock rate selection (1x, 2x data rates) Full user control of frame sync polarity, width, and position MVIP/ST-BUS, HMVIP, IOM/GCI, CHI, H.100, etc. compatibility Support for gapped clock generation
System Interface: Timing	Port timing is independent Tx and Rx timing on each port is fully independent (Tx and Rx can work asynchronously) and use independent clock/frame sync pairs. Selectable internal clock source generated from a single reference Selectable Master or Slave Operation Tx and Rx Clock/Frame Sync pairs can be inputs (Slave) and/or outputs (Master) When the Tx or Rx timing signals are outputs (Master) their timing can be derived from the internal clock source or from a selected Rx Line Clock. Selectable Loop Timing Options Any line port can be selected for loop timing Selectable System Timing Options Master Clock input can be N x 1.536 MHz, N x 1.544 MHz or N x 2.048 MHz (N = 1, 2 or 4)
System Interface: Overhead Ports	Signaling data is accessible: In band Signaling TDM port Microprocessor Interface The method of access is independent of data direction (i.e., Tx and Rx for a particular port can use different means of access). FDL data is accessible: Microprocessor Interface

Table 15. IXF3208 Feature Set - Maintenance/Miscellaneous

Feature	Detail
Maintenance Loopbacks	The following line-side loopbacks are supported: T1 Line (per: ANSI T1.403, AT&T TR 54016) T1 Payload (per: ANSI T1.403, AT&T TR 54016) T1 DS0 payload (Up to 24 DS0's simultaneously per port) T1 local loopback T1 remote loopback E1 Line E1 Payload E1 DSO payload (Up to 32 timeslots simultaneously per port) E1 local loopback E1 remote loopback The following system-side loopbacks are supported: Timeslot (Up to 32 timeslots simultaneously per port) Both types of loopback can be active at the same time. Selective Manual or Automatic Loopback support: T1: SF Fractional T1 Loopback (T1.403 Annex B) T1: SF Line Loopback (T1.403) T1: ESF Line Loopback (T1.403) T1: ESF Line Loopback (TR 54016) T1: ESF Payload Loopback (T1.403) T1: ESF Payload Loopback (TR 54016) E1: Sa5/Sa6 Codeword (ETS 300 233) Automatic AIS transmit upon loopback activation is selectively supported.
Error Injection	Selectable BPV, F-bit (T1)/ FAS Word (E1), and CRC Error Injection. Single errors One error per frame One error per multiframe One error per 1000 bits One error per second
External Indicators	Multiframe signals per line port are reported to the system. Frame Sync polarity, width and position are fully programmable. The polarity, width and position of the multiframe signal follows that of the corresponding Frame Sync.
Timeslot Code Insertion	T1: Programmable idle code and digital milliwatt insertion (as ANSI T1.403) T1 DRS pattern E1: Selectable digital milliwatt pattern insertion (as per ITU G.711) E1 DRS pattern

7.0 Mechanical Specification

Figure 3. IXF3208 256 PBGA Mechanical Specification