LXT3108 Octal T1/E1/J1 LH/SH LIU Interfacing with IXF3208 Octal Framer

Application Note

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Application Note

Contents

Figures

Tables

Revision History

Revision	Date	Description
-001	10/09/01	Initial Issue.

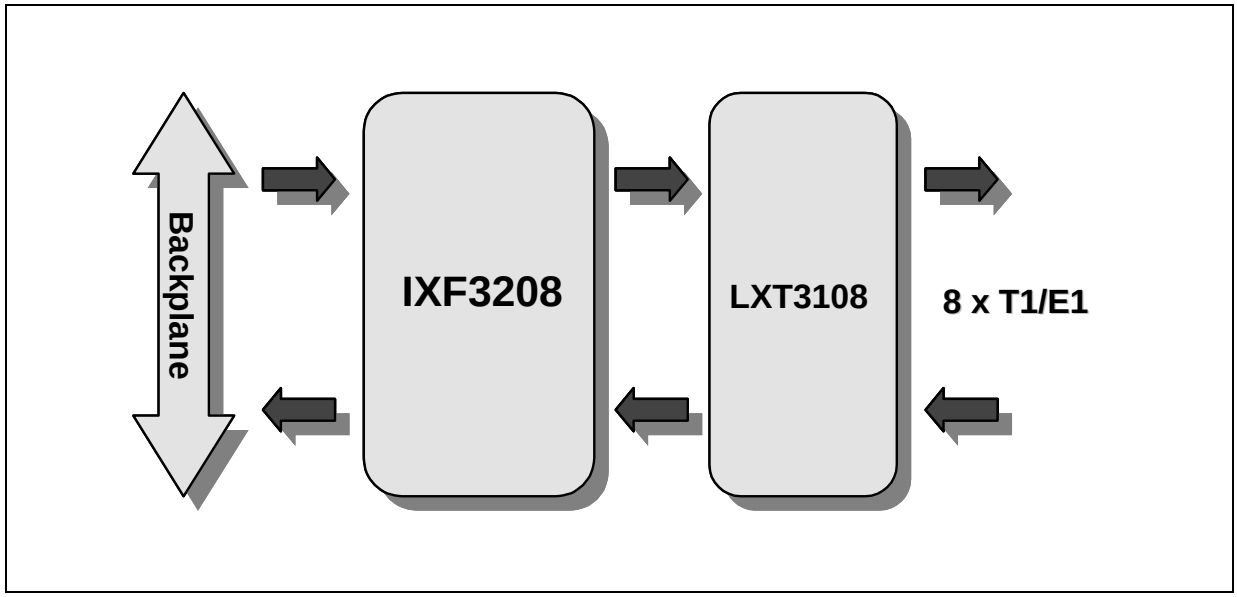
1.0 General Description

The Intel® LXT3108 octal Line Interface Unit (LIU) is the highest density T1/E1 Long Haul (LH), Short Haul (SH) solution currently available on the market. The LXT3108 is a full-featured T1/E1 LIU with crystal-less jitter attenuator.

In many applications, this LIU will interface with multi-port framers. The Intel® IXF3208 octal T1/E1/J1 framer is a natural choice, given its rich feature set and high density packages.

This application note shows that the Intel IXF3208 octal T1/E1/J1 framer can easily interface with the LXT3108 LIU. The following sections provide some guidelines regarding the connection of these devices in a typical T1/E1/J1 applications.

For related documents and current revision, see http://developer.intel.com/design/network/products/wan.



2.0 Digital Interface

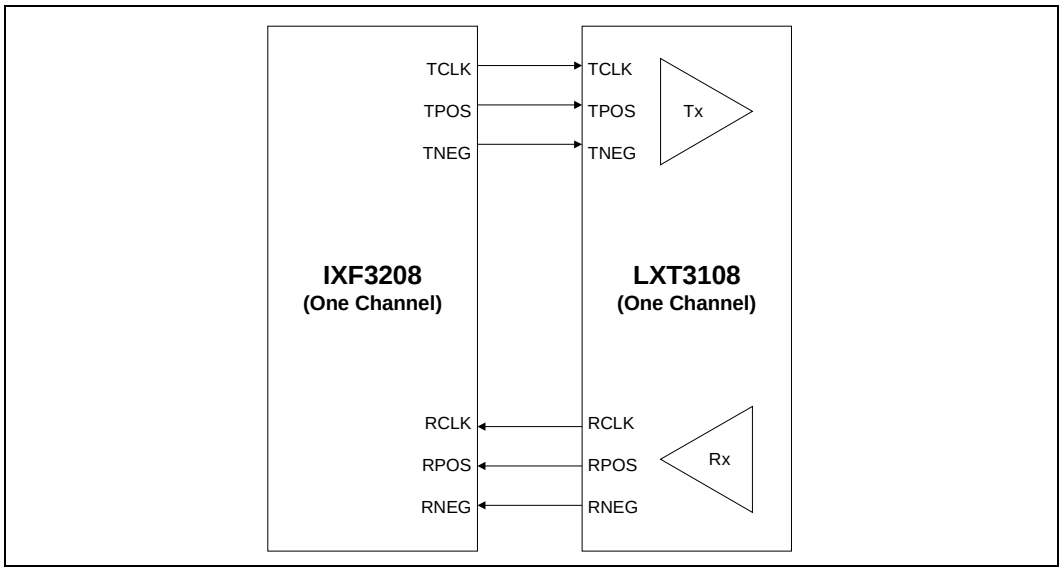
2.1 Unipolar/Bipolar Interface

The LXT3108 and the IXF3208 interface at the digital level through independent sets of data and clock signals for the receive and transmit paths. This interface can be either unipolar or bipolar. Given the bipolar interface's simplicity, it is recommended for most applications.

2.1.1 Bipolar Interface

In Bipolar mode, the LIU and the framer communicate using three signals in each direction: positive pulse (POS), negative pulse (NEG) and clock (CLK). See Figure 1.

Figure 1. Bipolar Interface



At the receive side, RPOS and RNEG indicate the LIU receiver has detected either a positive or negative pulse. RCLK is the clock extracted from the incoming signal and is used to latch the RPOS/RNEG data into the framer. Bipolar mode is sometimes called "dual rail mode," or "transparent mode" as the LIU simply reports the reception of negative or positive pulses to the framer. Note that the T1/E1/J1 input signal is a three-level signal with 0 V, positive or negative pulses. Therefore, in Bipolar mode, the framer must decode the sequence of positive and negative pulses into a data stream of 0s and 1s. As a result, the framer's HDB3 or AMI/B8ZS decoders must be enabled.

At the transmit side, the LIU outputs either positive or negative pulses according to the TPOS/TNEG data. When TPOS is High, a positive pulse is transmitted. When TNEG is High, a negative pulse is transmitted. When both TPOS and TNEG are Low, no pulse is transmitted onto the line. TCLK is used to latch the TPOS/TNEG data into the LIU. Note that since the sequence of positive and negative pulses (encoding) is not determined by the LIU, the HDB3 or B8ZS/AMI encoder must be enabled in the framer. Table 1 summarizes the settings in both the LXT3108 and the IXF3208 for Bipolar interface mode.

Table 1. Bipolar Interface Settings

LXT3108	IXF3208
RPOS/RNEG valid on falling edge of RCLK.	RPOS/RNEG can be valid on the falling or rising edge of RCLK. Register LIPOL (addr X+0h) controls clock edge.
TPOS/TNEG valid on falling edge of TCLK.	TPOS/TNEG can be valid on the falling or rising edge of TCLK. Register LIPOL (addr X+0h) controls clock edge.
Set bits 0 and 1 in register 1C to 0(selects Bipolar Mode).	Register LIMODE (addr X+2h) controls Bipolar/Unipolar mode selection. Select Bipolar Mode.
Set bits 2, and 3 in register 1C to 0(selects AMI code).	Register LIMODE (addr X+2h) controls AMI/B8ZS/HDB3 code selection.

2.1.2 Unipolar Interface

In Unipolar mode, the LIU and the framer exchange data using only two signals in each direction: one for data (DATA) and another for clock (CLK). See Figure 2. Unipolar mode is sometimes referred to as “single rail” or “NRZ” mode.

At the receive side, RDATA indicates the data content in the receive signal. RCLK is used to latch the RDATA information into the framer. Unipolar mode assumes that the data content of the LIU receive signal has already been decoded into a stream of 1s and 0s. Therefore, the HDB3 or B8ZS/AMI decoder should be enabled in the LIU.

At the transmit side, the TPOS/TCLK outputs from the framer connect directly to the TDATA/TCLK inputs of the LIU. The LIU is responsible for encoding the data stream into HDB3 or B8ZS/AMI line code.

Table 2 summarizes the settings in both the LXT3108 and the IXF3208 for Unipolar interface mode.

Figure 2. Unipolar Interface

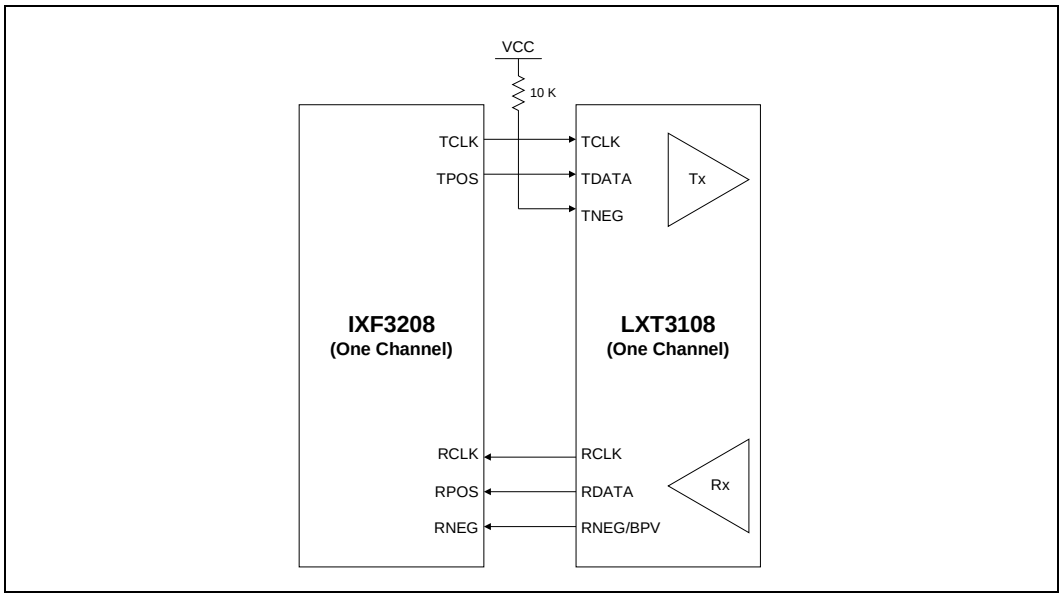


Table 2. Unipolar Interface Settings

LXT3108	IXF3208
RDATA valid on falling edge of RCLK. TDATA valid on falling edge of TCLK.	Register LIPOL (addr. X+0h) controls which clock edge validates the received data on RPOS input and transmit data on TPOS framer output.
Bits 0 and 1 in register 1C=1, Sets Unipolar Mode.	Register LIMODE (addr X+2h) and Register LINEGU (addr. X+1h) control Unipolar/Bipolar mode selection. Select Unipolar Mode.
Bits 2 and 3 in register 1C=1, enable B8ZS/HDB3 encoder decoders. Note: In Unipolar mode, the LXT3108 enables HDB3 codecs by default.	Register LIMODE (addr. X+2h) controls encoder/ decoder selection. Select AMI encoder/ decoder.

2.2 Timing Considerations

The timing characteristics of the LXT3108 and the IXF3208 are compatible. There is sufficient setup and hold time margin at both the receive and transmit interfaces.

2.3 Loss of Signal Detection

2.3.1 Bipolar Mode

Loss Of Signal (LOS) can be detected at either the framer or at the LIU. The IXF3208 LOS detection is based on the content of the RPOS/RNEG outputs from the LIU. When LOS is detected, the appropriate bit in the port status register is set and a microprocessor interrupt is generated (unless masked).

Alternatively, the LXT3108 can be used to detect LOS. The LOS register will indicate a LOS condition in any of the eight channels. The LOS condition is also reported on the LOS output.

2.3.2 Unipolar Mode

In Unipolar mode, the LIU is responsible for LOS detection. The LOS status is reported in the LXT3108 LOS register. LOS status can also be communicated to the framer via the LOS pins.

If the LOS condition is to be reported to the framer, then the LOS output pin for each channel should be connected to the corresponding LOS inputs on the IXF3208 framer. With the above configuration, the LOS status will be reflected in the framer Line Status Registers.

2.4 BPV Detection

2.4.1 Bipolar Mode

In Bipolar mode, code violations are detected by the framer and reported in the corresponding performance counters.

2.4.2 Unipolar Mode

In Unipolar mode, code violations are detected by the LIU and reported at the RNEG/BPV output pins. If the code violations need to be monitored by the framer, the RNEG/BPV pin should be connected to the corresponding RNEG inputs of the IXF3208. See Figure 2 and Table 2. Configure RNEG input of the IXF3208 as BPV input; register LINEGU controls this function.

An Alarm Indication Signal (AIS) can be detected by the framer. The AIS alarm is reported in the corresponding status register.

The LXT3108 can also detect AIS. The LIU will generate an interrupt (if enabled) when AIS is detected.

3.0 Jitter Attenuator

For T1/E1/J1 applications, the LXT3108 offers two per each port, advanced, digital CTR12 compliant jitter attenuators. Jitter attenuators can be placed in either the receive or the transmit path. If needed, the DJA can be enabled in both the transmit and receive path.

4.0 5V I/O Tolerance

Both the IXF3208 and the LXT3108 are 3.3V devices. When either of them interfaces with a 5V I/O device (a microprocessor for example), it is crucial to have 5V tolerant inputs.

All these devices can interface directly with 5V ICs. The IXF3208 and the LXT3108 accomplish this by offering 5V tolerant inputs.

5.0 Design Guidelines

Here's a list of general design guidelines:

- ***Avoid routing digital signals near analog signals.*** This is especially important near the receiver inputs as the cross-talk may induce bit errors.
- ***Provide ample power and ground planes.*** This practice will reduce emissions and assure signal integrity across the board.
- ***Reduce trace lengths connecting the devices, especially the clock signals.*** Although the T1/E1/J1 clock frequencies are relatively low, the rise and fall times in modern sub-micron CMOS technologies can be extremely fast. The LXT3108 has controlled slew rate output buffers that help minimize problems associated with fast transitions. However, the rise/fall time from the framer, or other digital devices (like CPU), may be considerably faster. This can create signal integrity problems when long traces connect the devices. As a rule of thumb, terminate clock signals between devices when the distance exceeds six inches.
- ***Use decoupling capacitors near the power supply pins.*** Decoupling capacitors will help reduce switching noise in the power supply. Follow the recommendations in the corresponding datasheets.

6.0 Glossary

Term Categories

Term	Term definition
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
BPV	BiPolar Violation
B8ZS	Bipolar 8 Zero Substitution
DJA	Digital Jitter Attenuator
HDB3	High Density Bipolar 3
LH	Long Haul
LIU	Line Interface Unit
LOS	Loss Of Signal
LH/SH	Long Haul/Short Haul
NRT	Non-Return to Zero
SH	Short Haul