IXYS

IXDD415SI
Dual 15 Ampere Low-Side Ultrafast MOSFET Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- High Peak Output Current: Dual 15A Peak
- Wide Operating Range: 8V to 30V
- Rise And Fall Times of <3ns
- Minimum Pulse Width Of 6ns
- Ability to Disable Output under Faults
- High Capacitive Load Drive Capability: 4nF in <5ns
- Matched Rise And Fall Times
- 32ns Input To Output Delay Time
- Low Output Impedance
- Low Supply Current

Applications

- Driving RF MOSFETs
- Class D or E Switching Amplifier Drivers
- Multi MHz Switch Mode Power Supplies (SMPS)
- Pulse Generators
- Acoustic Transducer Drivers
- Pulsed Laser Diode Drivers
- DC to DC Converters
- Pulse Transformer Driver

General Description

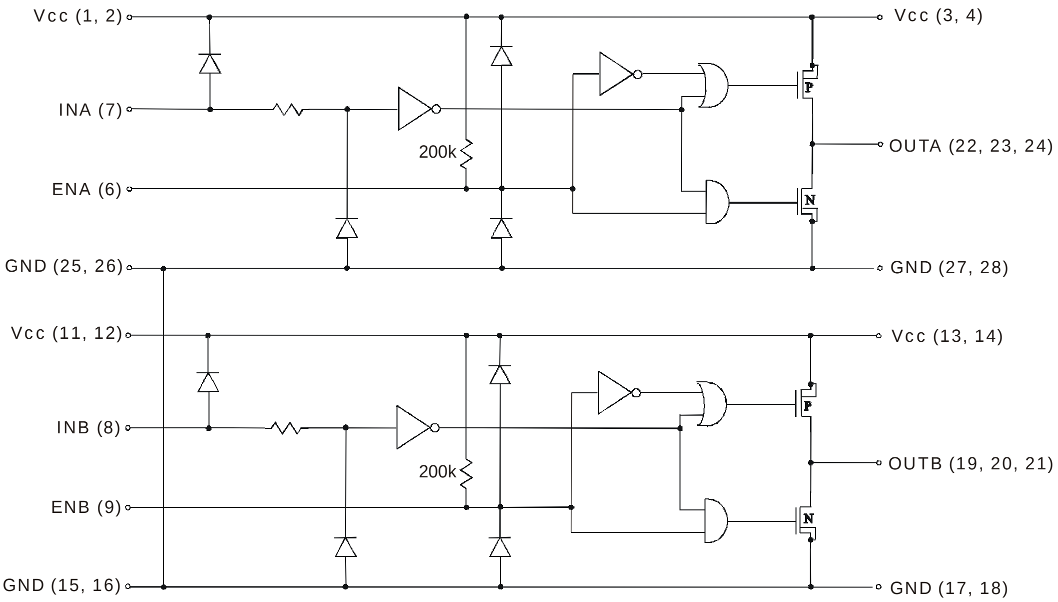
The IXDD415 is a dual CMOS high speed high current gate driver specifically designed to drive MOSFETs in Class D and E HF RF applications, as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. Each output of the IXDD415 can source and sink 15A of peak current while producing voltage rise and fall times of less than 3ns. The outputs of the IXDD415 may be paralleled, producing a single output of up to 30A with comparable rise and fall times. The input of the driver is compatible with TTL or CMOS and is fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the IXDD415. Its features and wide safety margin in operating voltage and power make the IXDD415 unmatched in performance and value.

The IXDD415 has two enable inputs, ENA and ENB. These enable inputs can be used to independently disable either of the outputs, OUTA or OUTB, for added flexibility. Additionally, the IXDD415 incorporates a unique ability to disable the output under fault conditions. When a logical low is forced into the Enable inputs, both final output stage MOSFETs (NMOS and PMOS) are turned off. As a result, the output of the IXDD415 enters a tristate mode and achieves a Soft Turn-Off of the MOSFET when a short circuit is detected. This helps prevent damage that could occur to the MOSFET if it were to be switched off abruptly due to a dv/dt over-voltage transient.

The IXDD415 is available in a 28 pin SO package (IXDD415SI), incorporating DEI's patented (1) RF layout techniques to minimize stray lead inductances for optimum switching performance.

(1) DEI U.S. Patent #4,891,686

Figure 1 - Functional Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	30V
All Other Pins	-0.3V to V_{CC} + 0.3V
Power Dissipation $T_{AMBIENT} \leq 25\ ^{o}C$ $T_{CASE} \leq 25\ ^{o}C$	 1W 12W
Derating Factors (to Ambient) 28-Pin SOIC	 $0.1W/^{o}C$
Storage Temperature	$-65^{o}C$ to $150^{o}C$
Soldering Lead Temperature (10 seconds maximum)	$300^{o}C$

Operating Ratings

Parameter	Value
Maximum Junction Temperature	$150^{o}C$
Operating Temperature Range	$-40^{o}C$ to $85^{o}C$
Thermal Impedance (Junction To Case) 28 Pin SOIC (SI) (θ_{JC})	 $0.75^{o}C/W$

Electrical Characteristics

Unless otherwise noted, $T_A = 25\ ^{o}C$, $4.5V \leq V_{CC} \leq 25V$.

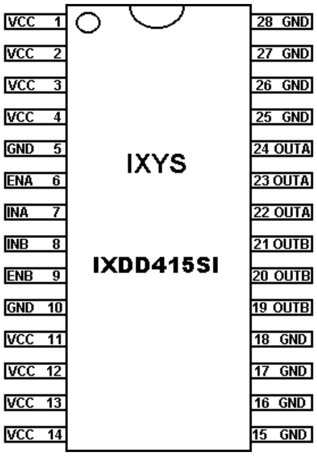
All voltage measurements with respect to GND. IXDD415 configured as described in *Test Conditions*.

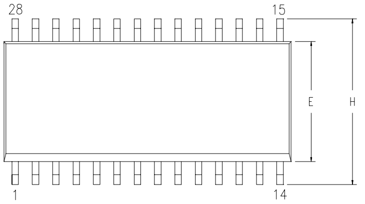
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		3.5			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	$0V \leq V_{IN} \leq V_{CC}$	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output High	I_{OUT} = 10mA, V_{CC} = 15V		0.8	1.2	Ω
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, V_{CC} = 15V		0.8	1.2	Ω
I_{PEAK}	Peak output current	V_{CC} = 15V, each output		15		A
I_{DC}	Continuous output current				2	A
V_{EN}	Enable voltage range		-0.3		Vcc + 0.3	V
V_{ENH}	High En input voltage		2/3 Vcc			V
V_{ENL}	Low En input voltage				1/3 Vcc	V
f_{MAX}	Maximum frequency	C_L=1.0nF Vcc=15V, max CW frequency limited by package power dissipation			45	MHz
t_R	Rise time [(1)]	C_L=1nF Vcc=15V V_{OH}=2V to 12V C_L=4nF Vcc=15V V_{OH}=2V to 12V		2.5 4.5		ns ns
t_F	Fall time [(1)]	C_L=1nF Vcc=15V V_{OH}=2V to 12V C_L=4nF Vcc=15V V_{OH}=2V to 12V		2.0 3.5		ns ns
t_{ONDLY}	On-time propagation delay [(1)]	C_L=4nF Vcc=15V		32	38	ns
t_{OFFDLY}	Off-time propagation delay [(1)]	C_L=4nF Vcc=15V		29	35	ns
P_{Wmin}	Minimum pulse width	FWHM C_L=1nF +3V to +3V C_L=1nF		5.0 7.0		ns ns
t_{ENOL}	Enable to output low delay time	Vcc=15V			80	ns
t_{ENOH}	Enable to output high delay time	Vcc=15V			170	ns
t_{DOLD}	Disable to output low Disable delay time	Vcc=15V			30	ns
t_{DOHD}	Disable to output high Disable delay time	Vcc=15V			30	ns
V_{CC}	Power supply voltage		8	15	30	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0 	3 10 10	mA µA µA

(1) Refer to Figures 2a and 2b

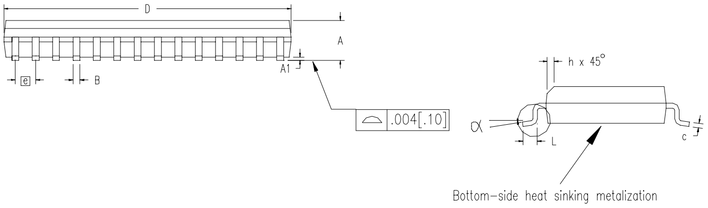
Specifications Subject To Change Without Notice

Pin Configurations And Package Outline





SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
B	.013	.020	.33	.51
C	.009	.013	.23	.32
D	.697	.713	17.70	18.10
E	.291	.299	7.40	7.60
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
h	.010	.029	.25	.75
L	.016	.050	.40	1.27
α	0°	8°	0°	8°



NOTE: Bottom-side heat sinking metalization is connected to ground

Pin Description

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1-4 11-14	VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 8V to 30V.
7	INA	Input	Input signal-TTL or CMOS compatible.
6	ENA	Enable	The system enable pin. This pin, when driven low, disables the chip, forcing high impedance state to the output.
22-24	OUTA	Output	Driver Output. For application purposes, this pin is connected to the Gate of a MOSFET. In some applications, a low-impedance series resistor may be required between this output and the MOSFET Gate.
8	INB	Input	Input signal-TTL or CMOS compatible.
9	ENB	Enable	The system enable pin. This pin, when driven low, disables the chip, forcing high impedance state to the output.
19-21	OUTB	Output	Driver Output. For application purposes, this pin is connected to the Gate of a MOSFET. In some applications, a low-impedance series resistor may be required between this output and the MOSFET Gate.
5,10 15-18 25-28	GND	Ground	The system ground pins. Internally connected to all circuitry, these pins provide ground reference for the entire chip. All of these pins should be connected to a low noise analog ground plane for optimum performance.

Note 1: Operating the device beyond parameters with listed "Absolute Maximum Ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Ordering Information			
Part Number	**Package Type**	**Temp. Range**	**Grade**
IXDD415SI	28-Pin SOIC	-40°C to +85°C	Industrial

Typical Performance Characteristics

Figure 2a - Characteristics Test Diagram

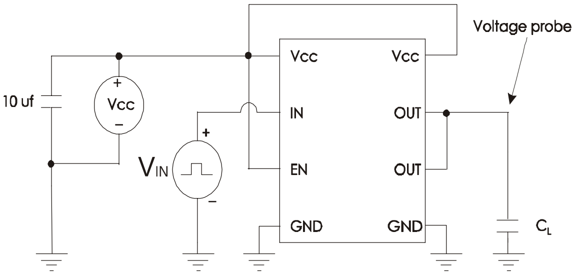


Figure 2b - Timing Diagram

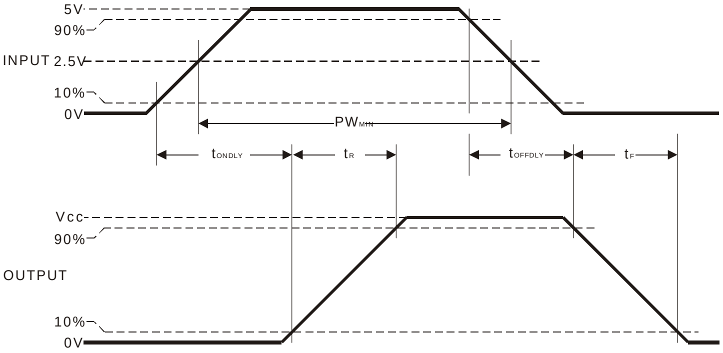


Fig. 3 Rise Time vs. Load Capacitance $V_{CC} = 15V, V_{OH} = 2V$ To $12V$

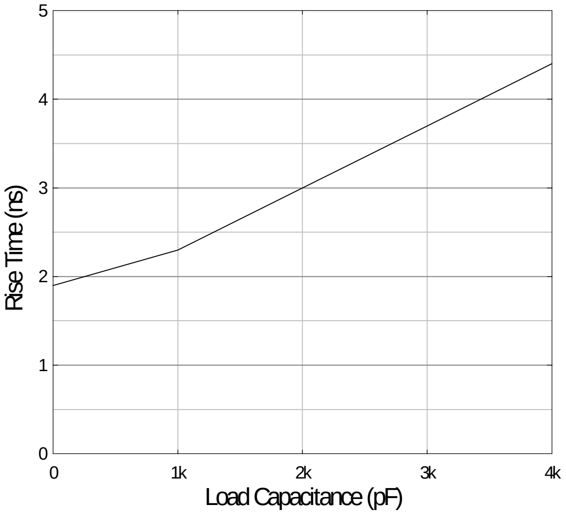


Fig. 4 Fall Time vs. Load Capacitance $V_{CC} = 15V, V_{OH} = 12V$ To $2V$

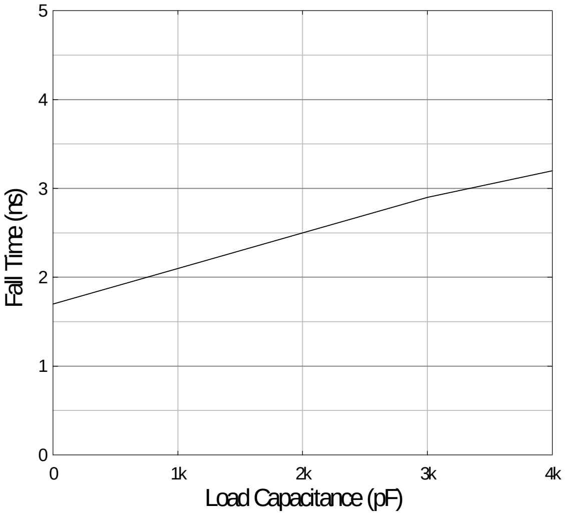


Fig. 5 Supply Current vs. Frequency Vcc=15V

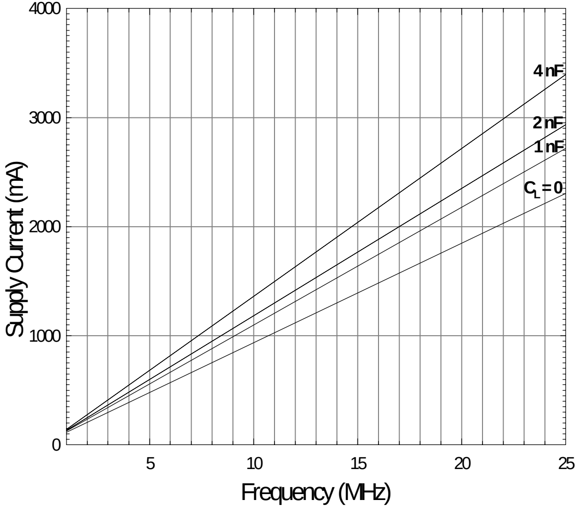


Fig. 6 Supply Current vs. Load Capacitance Vcc=15V

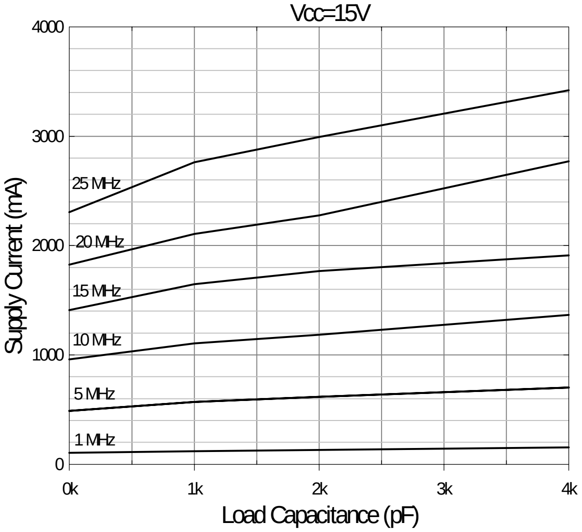


Fig. 7

Propagation Delay vs. Supply Voltage
C_L=4nF V_{IN}=5V@100kHz

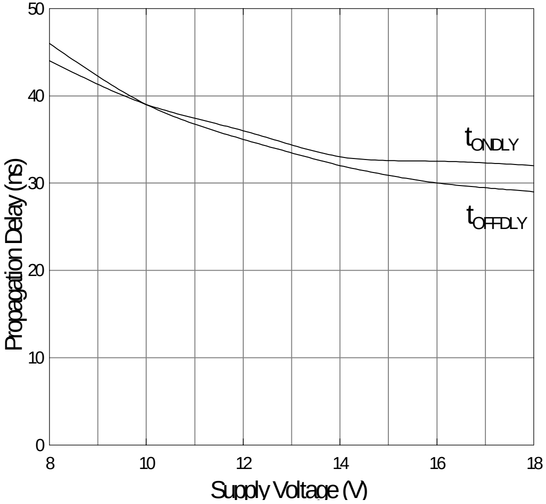


Fig. 8

Propagation Delay vs. Input Voltage
C_L=4nF V_{CC}=15V

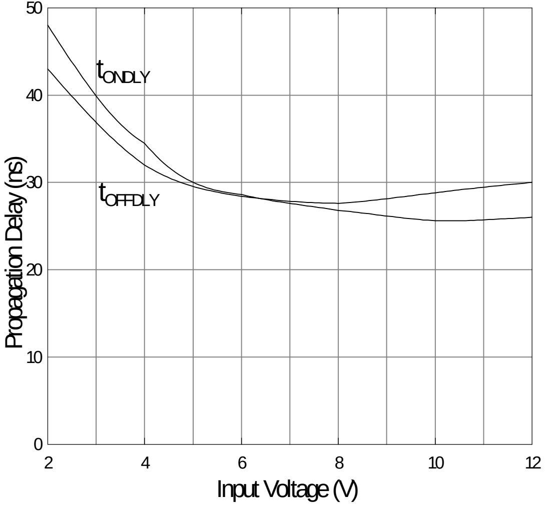
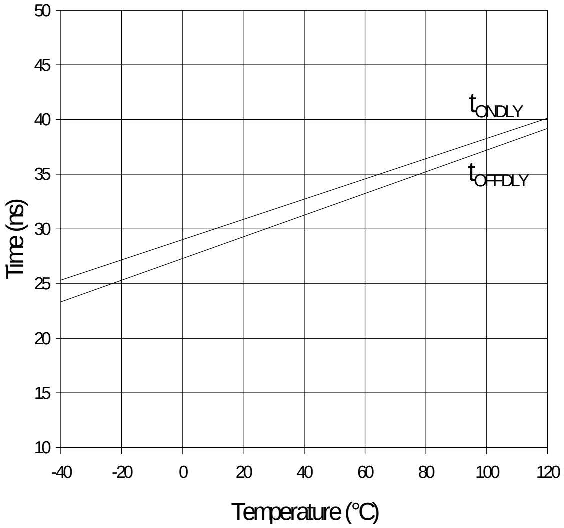


Fig. 9

Propagation Delay vs. Junction Temperature
C_L=4nF, V_{CC}=15V



Typical Output Waveforms

Unless otherwise noted, all waveforms are taken driving a 1nF load, 1MHz repetition frequency, V_{CC}=15V, Case Temperature = 25°C

Figure 10 2.2ns Rise Time

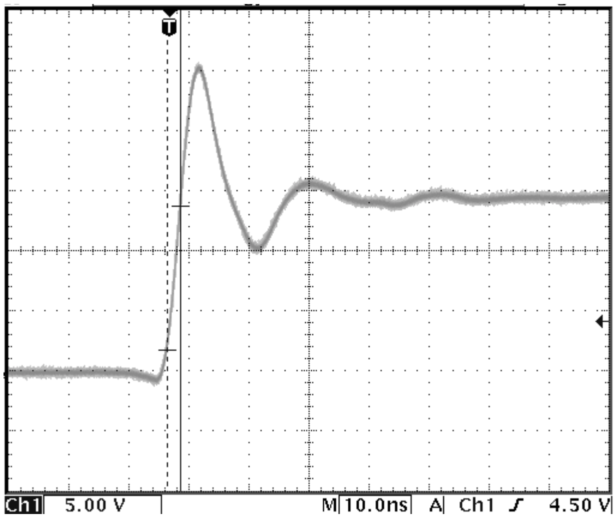


Figure 11 <6ns Minimum Pulse Width

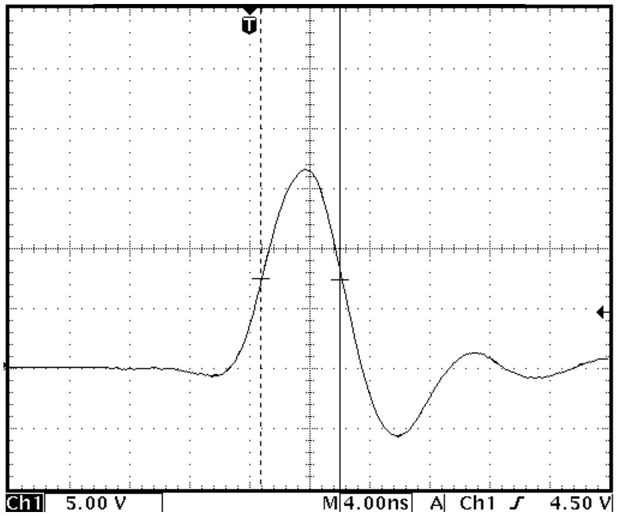


Figure 12 500KHz CW Repetition Frequency

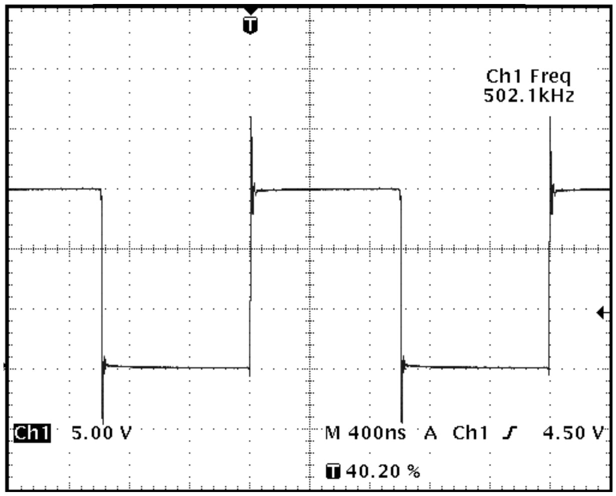


Figure 13 50MHz Burst Repetition Frequency

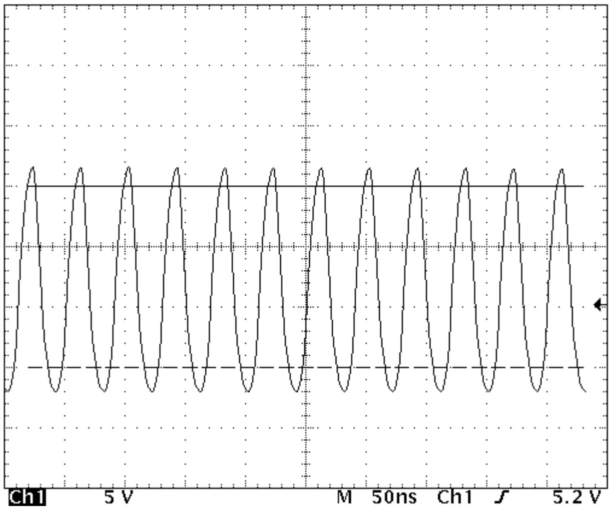
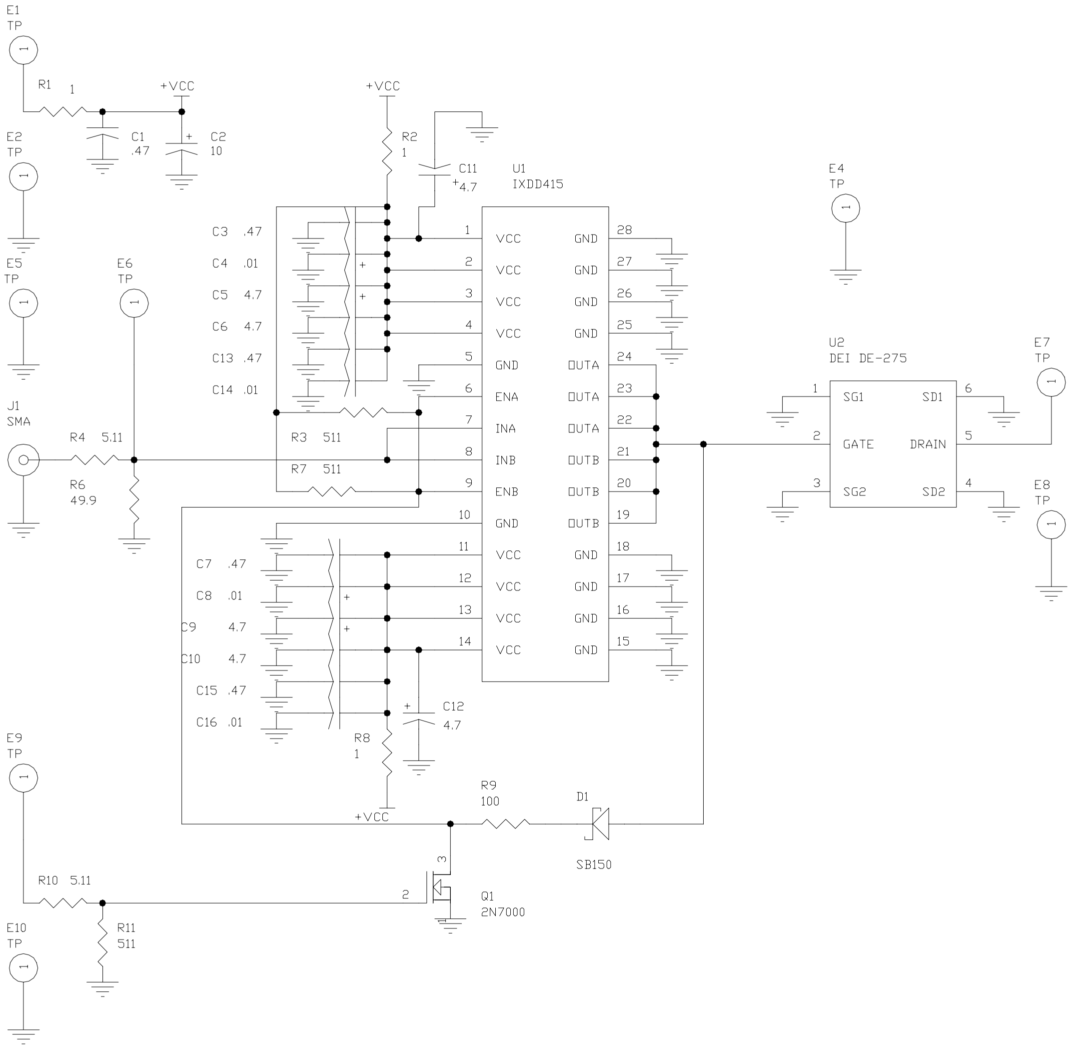


Figure 14 - High Frequency Gate Drive Circuit



APPLICATIONS INFORMATION

High Frequency Gate Drive Circuit

The circuit diagram in figure 14 is a circuit diagram for a very high switching speed, high frequency gate driver circuit using the IXDD415SI. This is the circuit used in the EVDD415 Evaluation Board,and is capable of driving a MOSFET at up to the maximum operating limits of the IXDD415. The circuit's very high switching speed and high frequency operation dictates the close attention to several important issues with respect to circuit design. The three key elements are circuit loop inductance, Vcc bypassing and grounding.

Circuit Loop Inductance
Referring to Figure 14, the Vcc to Vcc ground current path defines the loop which will generate the inductive term. This loop must be kept as short as possible. The output leads (pins 24, 23, 22, 21, 20, and 19) must be no further than 0.375 inches (9.5mm) from the gate of the MOSFET. Furthermore the output ground leads (pins 25, 26, 27 and 28 on one end of the IC and pins 15, 16, 17, and 18 on the other end of the IC) must provide a balanced symmetric coplanar ground return for optimum operation.

Vcc Bypassing
In order for the circuit to turn the MOSFET on properly, the IXDD415 must be able to draw up to 15A of current per output channel from the Vcc power supply in 2-6ns (depending upon the input capacitance of the MOSFET being driven). This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is at least two orders of magnitude larger than the load capacitance. Usually, this is achieved by placing two or three different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDD415 to an absolute minimum.

The bypassing should be comprised of several values of chip capacitors symmetrically placed on ether side of the IC. Recommended values are .01uF, .47uF chips and at least two 4.7uF tantalums.

Grounding
In order for the design to turn the load off properly, the IXDD415 must be able to drain this 15A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDD415 and its load. Path #2 is between the IXDD415 and its power supply. Path #3 is between the IXDD415 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical.

Output Lead Inductance
Of equal importance to supply bypassing and grounding are issues related to the output lead inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible, and treated as coplanar transmission lines.

In configurations where the optimum configuration of circuit layout and bypassing cannot be used, a series resistance of a few Ohms in the gate lead may be necessary to prevent ringing.

Heat Sinking

For high power operation, the bottom side metalized heat sink pad should be epoxied to the circuit board ground plane, or attached to an appropriate heat sink, using thermally conductive epoxy. The heat sink tab is connected to ground.

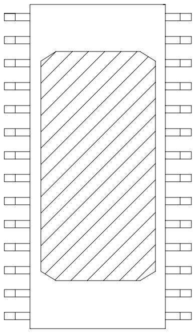


Figure 15: IXDD415SI Bottom Side Heat Sinking Metalization

TTL to High Voltage CMOS Level Translation

The enable (EN) input to the IXDD415 is a high voltage CMOS logic level input where the EN input threshold is ½ V_{CC}, and may not be compatible with 5V CMOS or TTL input levels. The IXDD415 EN input was intentionally designed for enhanced noise immunity with the high voltage CMOS logic levels. In a typical gate driver application, V_{CC} =15V and the EN input threshold at 7.5V, a 5V CMOS logical high input applied to this typical IXDD415 application's EN input will be misinterpreted as a logical low, and may cause undesirable or unexpected results. The note below is for optional adaptation of TTL or 5V CMOS levels.

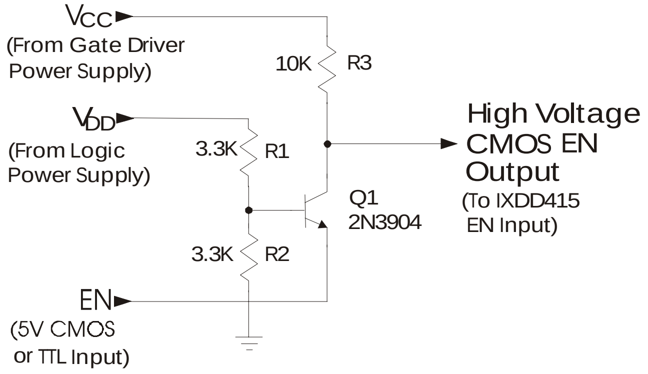
The circuit in Figure 16 alleviates this potential logic level misinterpretation by translating a TTL or 5V CMOS logic input to high voltage CMOS logic levels needed by the IXDD415 EN input. From the figure, V_{CC} is the gate driver power supply, typically set between 8V to 20V, and V_{DD} is the logic power supply, typically between 3.3V to 5.5V. Resistors R1 and R2 form a voltage divider network so that the Q1 base is positioned at the midpoint of the expected TTL logic transition levels.

A TTL or 5V CMOS logic low, V_{TTLLOW}=~<0.8V, input applied to the Q1 emitter will drive it on. This causes the level translator output, the Q1 collector output to settle to $V_{CESATQ1}$ + V_{TTLLOW}=<~2V, which is sufficiently low to be correctly interpreted as a high voltage CMOS logic low (<1/3V_{CC}=5V for V_{CC} =15V given in the IXDD415 data sheet.)

A TTL high, $V_{TTLHIGH}$=>~2.4V, or a 5V CMOS high, $V_{5VCMOSHIGH}$=~>3.5V, applied to the EN input of the circuit in Figure 16 will cause Q1 to be biased off. This results in Q1 collector being pulled up by R3 to V_{CC}=15V, and provides a high voltage CMOS logic high output. The high voltage CMOS logical EN output applied to the IXDD415 EN input will enable it, allowing the gate driver to fully function as a 15 Ampere output driver.

The total component cost of the circuit in Figure 16 is less than $0.10 if purchased in quantities >1K pieces. It is recommended that the physical placement of the level translator circuit be placed close to the source of the TTL or CMOS logic circuits to maximize noise rejection.

Figure 16 - TTL to High Voltage CMOS Level Translator



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