OBSOLETE PRODUCT
No Recommended Replacement

August 1998 File Number 3209.2

Power Control IC Single Chip Power Supply

The HIP5063 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC.

This IC allows the user maximum flexibility in implementing high frequency current controlled power supplies and other power sources.

Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Over-temperature detection circuitry is incorporated within the IC to monitor the chip temperature.

As a result of the power DMOS transistor's current and voltage capability (10A and 60V), power supplies with output power capability up to 100 watts are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5063DY	0^oC to $+85^oC$	21 Pad Chip
HIP5063DW	0^oC to $+85^oC$	Wafer

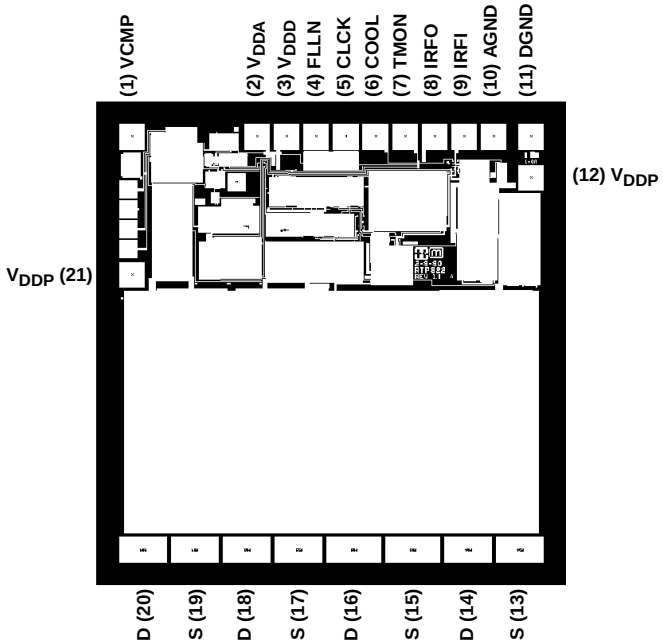
Features

- Single Chip Current Mode Control IC
- 60V, 10A On-chip DMOS Transistor
- Thermal Protection
- 1MHz Operation - External Clock
- Output Rise and Fall Times ~ 3ns
- Simple Implementation of High-Speed Current Mode Controlled Regulators and Power Amplifiers
- Designed for 10V to 45V Operation

Applications

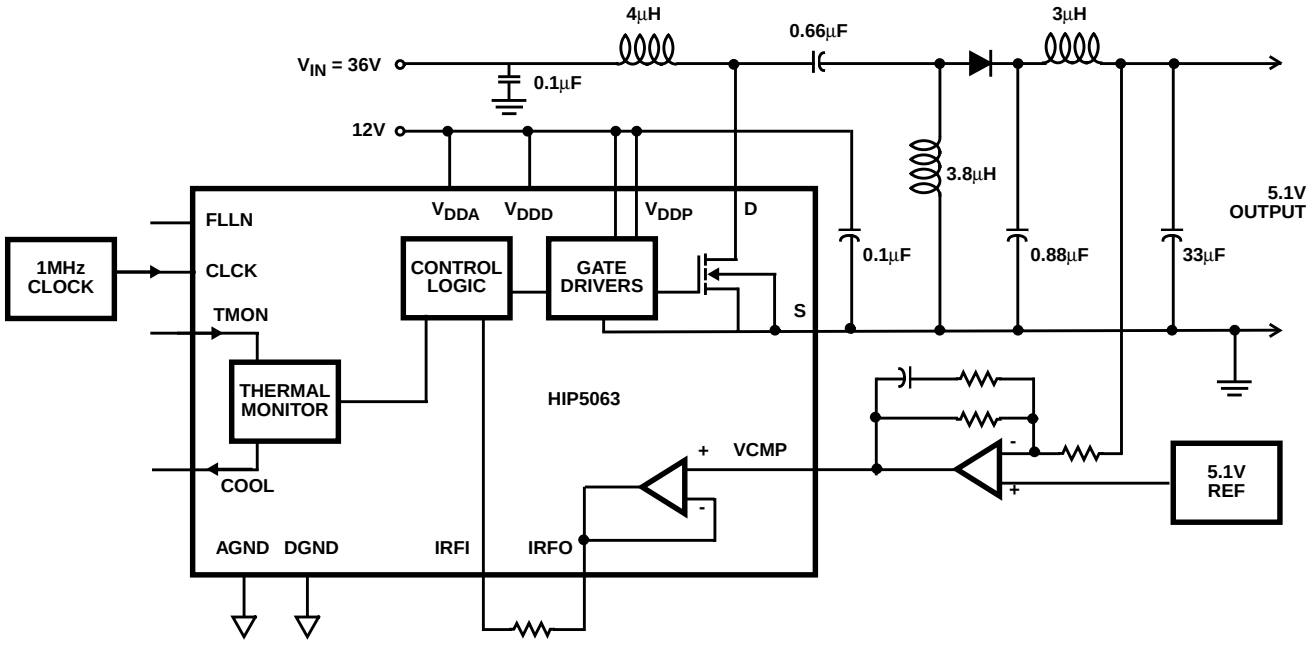
- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters
- Wideband Power Amplifiers for Motor Control

Chip



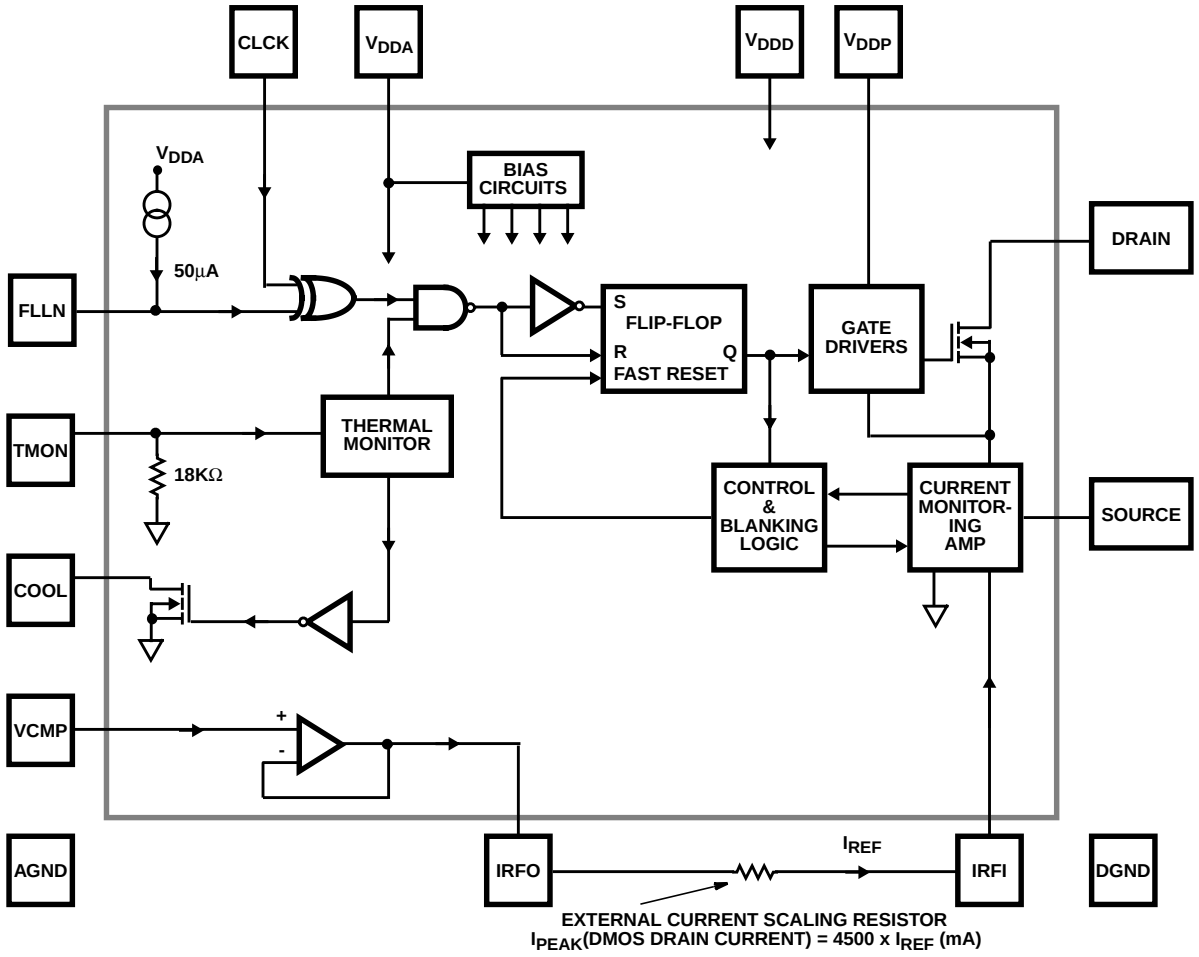
NOTE: Unused pads are for trim and test.
122 mils x 126 mils (3.1mm x 3.2mm)

Simplified Block Diagram



TYPICAL SEPIC APPLICATION CONFIGURATION

Functional Block Diagram



Absolute Maximum Ratings

DMOS Drain Voltage . . . . . -0.3V to 60V
DMOS Drain Current 20A
DC Logic Supply. . . . . -0.3V to 16V
Output Voltage, Logic Outputs . . . . . -0.3V to 16V
Input Voltage, Analog and Logic. . . . . -0.3V to 16V
Operating Junction Temperature Range. . . . . 0^oC to $+110^oC$
Storage Temperature Range . . . . . -55^oC to $+150^oC$

Thermal Information

Thermal Resistance θ_{JC}
(Solder Mounted to . . . . . $3^oC/W$ Max
0.050" Thick Copper Heat Sink)
Maximum Junction Temperature . . . . . $+110^oC$
(Controlled By Thermal Shutdown Circuit)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{DDA} = V_{DDD} = V_{DDP} = 12V$, $T_J = 0^oC$ to $+110^oC$; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	External Clock Input = 1MHz	-	14	-	mA
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 5A, $T_J = +25^oC$	-	-	0.13	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA
CURRENT CONTROLLED PWM						
$\|V_{IO}\|$ VCMP	Buffer Offset Voltage (VCMP - V_{IRFO})	IRFO = 0mA to -5mA, VCMP = 0.2V to 7.6V	-	-	125	mV
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	3.8	-	4.9	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{RFI} = 2mA	150	-	360	Ω
t_{RS}	Current Comparator Response Time (Note 1)	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/ms	-	30	-	ns
MCPW	Minimum Controllable Pulse Width (Note 1)		25	50	100	ns
MCPI	Minimum Controllable DMOS Peak Current (Note 1)		200	400	800	mA
CLOCK						
V_{TH} CLCK	CLCK Input Threshold Voltage		4	-	8	V
V_{TH} FLLN	FLLN Input Threshold Voltage		4	-	8	V
I_{FLLN}	FLLN Pull-Up Current	VFLLN = 0V	-70	-50	-30	µA
THERMAL MONITOR						
TEMP	Substrate Temperature for Thermal Monitor to Trip (Note 1)	TMON pin open	105	-	135	^oC
I_{LEAK} COOL	COOL Leakage Current	V_{COOL} = 12V	-	-	1	µA
V_{COOL}	COOL Low-State Voltage	I_{COOL} = 2mA, $T_J > +125^oC$	-	-	0.4	V

NOTE:

1. Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1	VCMP	This is the input terminal from an external error amplifier. A MOS input voltage follower buffers this terminal. The buffer output is the IRFO terminal. The external error amplifier may be either an operational amplifier or a transconductance amplifier like the CA3080. This node may be used for both gain and frequency compensation of the control loop.
2	V_{DDA}	This is the analog supply input. An external 12V supply is required.
3	V_{DDD}	Voltage input for the chip's digital circuits.
4	FLLN	One pad of two clocking terminals. This terminal has an external 50µA pull-up current that allows the terminal to be floated or be left open. With FLLN high, (open or tied to V_{DDD}), the ON cycle will start wiith the falling edge of the CLCK input. With FLLN low or grounded, the DMOS ON cycle will start on the rising edge of the CLCK input.
5	CLCK	The other clock input pad. An external clock is applied to this terminal. This terminal has no pull-up current or resistance. See FLLN above for phasing information.
6	COOL	Over-temperature indication is provided at this pad. When the chip temperature is below the thermal threshold, the open drain DMOS transistor is in the high impedance state. When the thermal threshold is exceeded, COOL is held low.
7	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to V_{DDA} or 12V the function is disabled. Returning this pad to ground will enable the thermal monitor function. Thermal threshold occurs at a nominal junction temperature of $+125^{o}C$.
8	IRFO	A resistor placed between this pad and IRFI converts the VCMP signal to a reference current for the current sense comparator. The cycle by cycle peak current is set by the value to this resistor according the the equation: I_{PEAK} = 4500 x VCMP/R. Where I_{PEAK} is in amperes and R is the value of the external resistor in ohms. A maximum VCMP of 8V and a resistor of 1800Ω will keep the drain current below the absolute maximum specification of 20A.
9	IRFI	See IRFO.
10	AGND	Analog ground.
11	DGND	Digital ground.
12 & 21	V_{DDP}	These pads are used to decouple the high current pulses to the output driver transistors. The capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
13, 15, 17, 19	S	Source pads of the DMOS power transistor.
14, 16, 18, 20	D	Drain pads of the DMOS power transistor.