DATA SHEET

NEC

MOS INTEGRATED CIRCUITS

μPD789166(A1),167(A1),176(A1),177(A1), 166(A2),167(A2),176(A2),177(A2)

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD789166(A1), 789167(A1), 789166(A2), and 789167(A2) (hereafter, represented as μPD78916x(A1) and μPD78916x(A2)) are members of the μPD789167 Subseries in the 78K/0S Series. The μPD789176(A1), 789177(A1), 789176(A2), and 789177(A2) (hereafter, represented as μPD78917x(A1) and μPD78917x(A2) are members of the μPD789177 Subseries in the 78K/0S Series.

In addition to an 8-bit CPU, these microcontrollers incorporate various hardware such as I/O ports, timers, a serial interface, an A/D converter, and interrupt control.

A stricter quality assurance program (called special grade in NEC's grade classification) is applied to the (A1) products and (A2) products, compared to the μPD78916x and 78917x, which are classified as standard grade.

In addition, a flash memory version (μPD78F9177) that can operate within the same power supply voltage range as the mask ROM version, and a range of development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual: U14186E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

Item / Part Number	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)	A/D Converter Resolution	Operating Ambient Temperature
μPD789166(A1)	16 KB	512 bytes	8 bits	T_A = –40 to +110°C
μPD789167(A1)	24 KB			
μPD789176(A1)	16 KB		10 bits	
μPD789177(A1)	24 KB			
μPD789166(A2)	16 KB		8 bits	T_A = –40 to +125°C
μPD789167(A2)	24 KB			
μPD789176(A2)	16 KB		10 bits	
μPD789177(A2)	24 KB			

- Minimum instruction execution time can be changed from high-speed (0.4 μs @5.0 MHz operation with main system clock) to ultra-low-speed (122 μs @ 32.768 kHz operation with subsystem clock)
- A/D converter: 8 channels
- On chip 16-bit multiplier
- I/O ports: 31
- Power supply voltage: V_{DD} = 4.5 to 5.5 V
- Serial interface: 1 channel
  Switchable between 3-wire serial I/O mode and UART mode
- Timers: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel

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APPLICATIONS

Power windows, keyless entry, battery management unit, side-impact air bags, etc

ORDERING INFORMATION

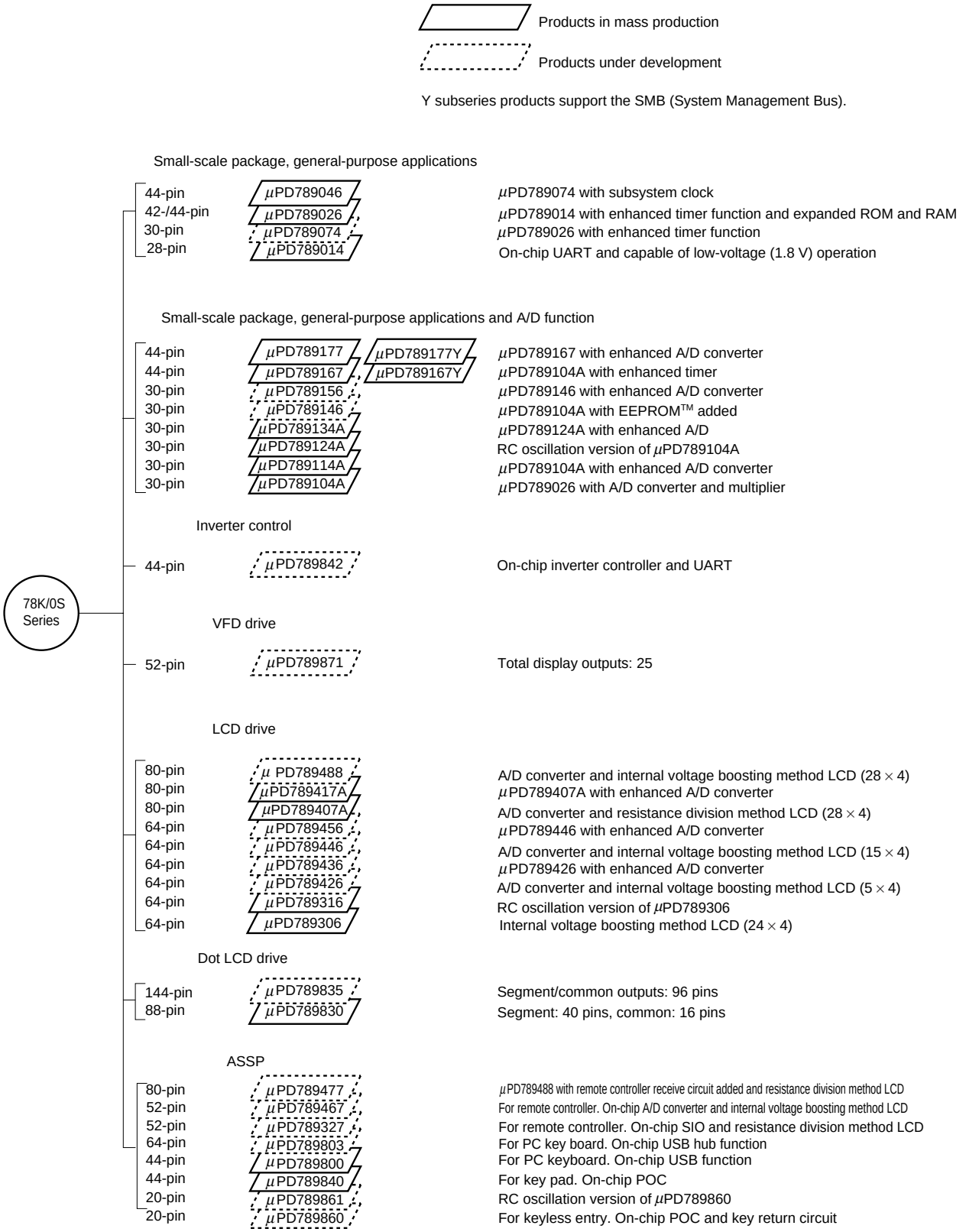
Part Number	Package	Quality Grade
μPD789166GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789167GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789176GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789177GB(A1)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789166GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789167GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789176GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)
μPD789177GB(A2)-×××-8ES	44-pin plastic LQFP (10 × 10)	Special (for high reliability electrical equipment)

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major differences between subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
			8-Bit	16-Bit	Watch	WDT						
Small-scale, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789074	2 K to 8 K								24		
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale, general-purpose applications + A/D function	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		Internal EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K						4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789417A	12 K to 24 K						7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789477	24 K	3 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch (UART: 1 ch)	45	1.8 V	Internal LCD
	μPD789467	4 K to 24 K	2 ch	–			1 ch		–	18		
	μPD789327						–		1 ch	21		
	μPD789800	8 K			–				2 ch (USB: 1 ch)	31	4.0 V	–
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC oscillation version, Internal EEPROM
	μPD789860											Internal EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

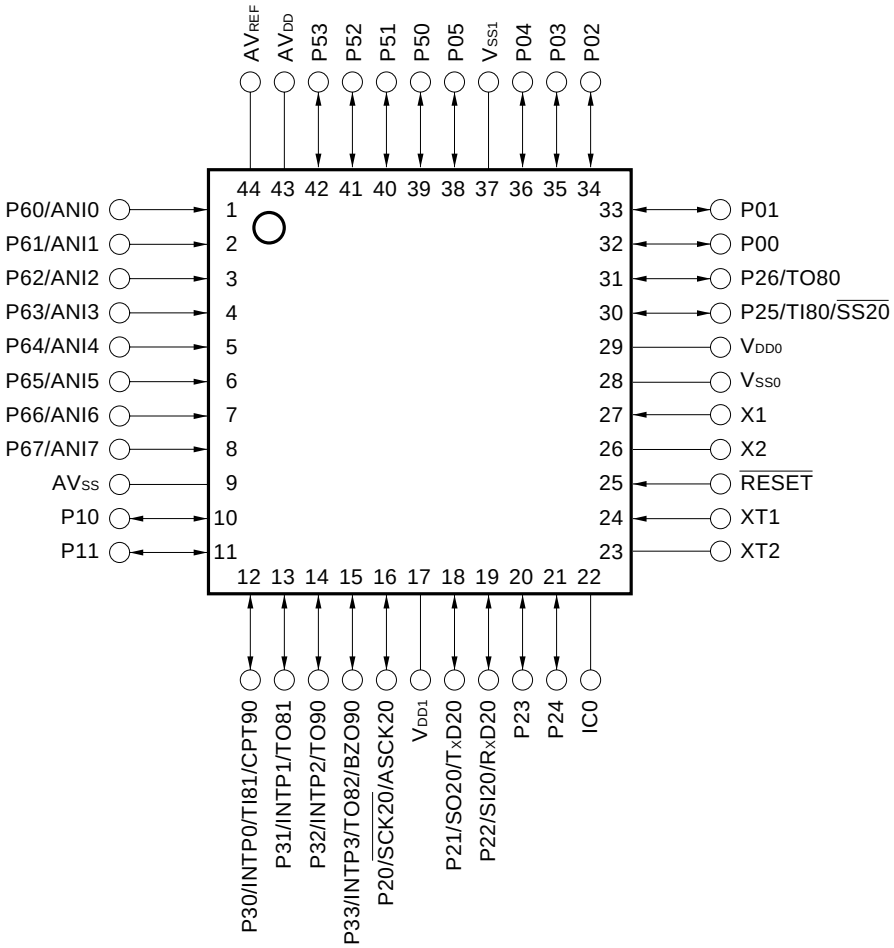
Item		μPD789166(A1), 789176(A1) μPD789166(A2), 789176(A2)	μPD789167(A1), 789177(A1) μPD789167(A2), 789177(A2)
Internal memory	ROM	16 KB	24 KB
	High-speed RAM	512 bytes	
Minimum instruction execution time		• 0.4μs/1.6 μs (@ 5.0 MHz operation with main system clock) • 122 μs (@ 32.768 kHz operation with subsystem clock)	
General-purpose registers		8 bits × 8 registers	
Instruction set		• 16-bit operations • Bit manipulations (set, reset, and test)	
Multiplier		8 bits × 8 bits = 16 bits	
I/O ports		Total: 31 • CMOS input: 8 • CMOS I/O: 17 • N-ch open-drain (12 V tolerance): 6	
A/D converter		• 8-bit resolution × 8 channels (μPD78916x(A1), 78916x(A2)) • 10-bit resolution × 8 channels (μPD78917x(A1), 78917x(A2))	
Serial interface		3-wire serial I/O/UART: 1 channel	
Timers		• 16-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • 8-bit timer: 1 channel • Watch timer: 1 channel • Watchdog timer: 1 channel	
Timer outputs		4	
Vectored interrupt sources	Maskable	Internal: 10, External: 4	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 4.5 to 5.5 V	
Operating ambient temperature		T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1))	
		T_A = –40 to +125°C (μPD78916x(A2), 78917x(A2))	
Package		44-pin plastic LQFP (10 × 10)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- 44-pin plastic LQFP (10 × 10)

  μPD789166GB(A1)-×××-8ES μPD789166GB(A2)-×××-8ES
  μPD789167GB(A1)-×××-8ES μPD789167GB(A2)-×××-8ES
  μPD789176GB(A1)-×××-8ES μPD789176GB(A2)-×××-8ES
  μPD789177GB(A1)-×××-8ES μPD789177GB(A2)-×××-8ES



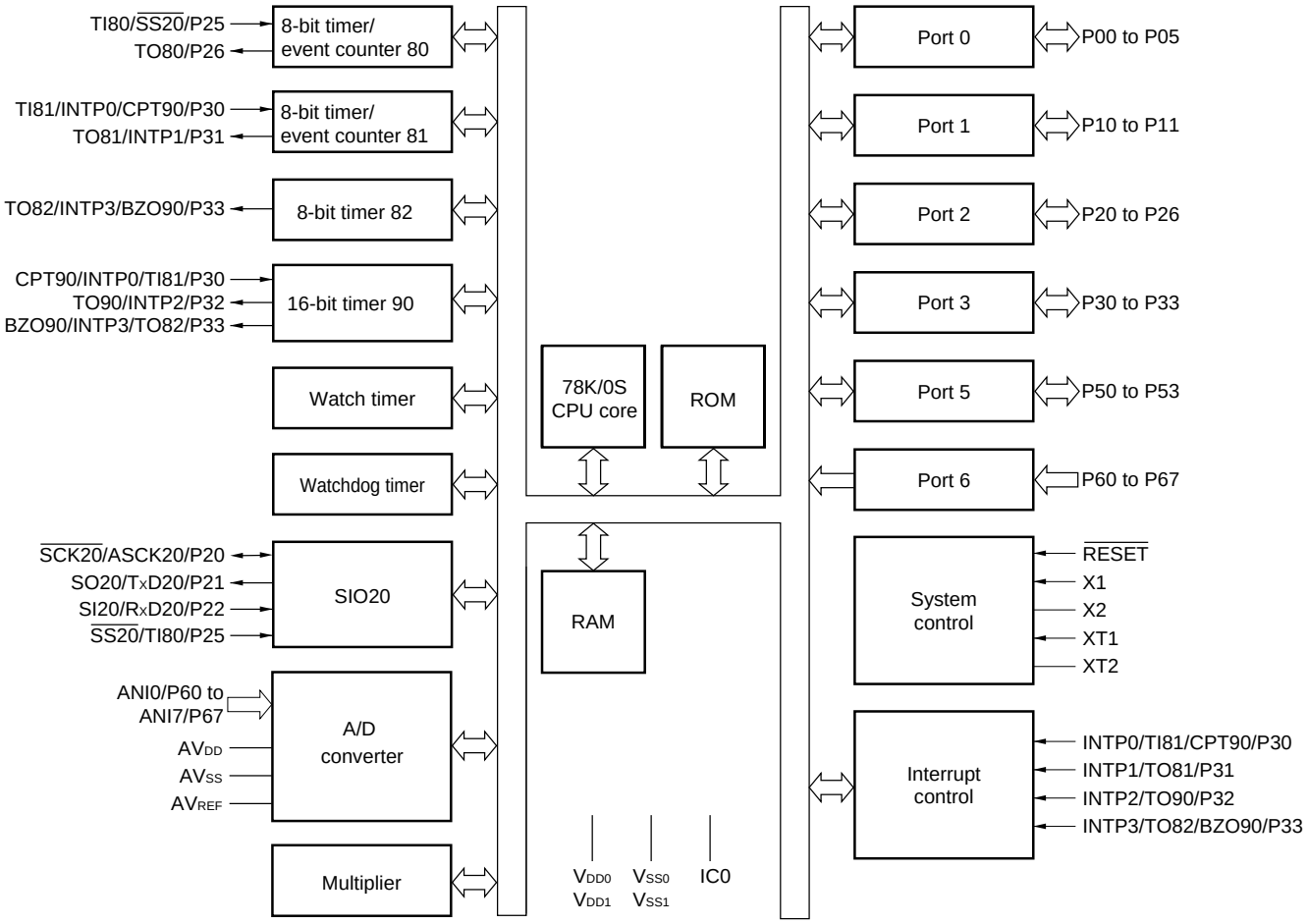
Cautions 1. Connect the IC0 (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{DD} pin to V_{DD0}.

3. Connect the AV_{SS} pin to V_{SS0}.

ANI0 to ANI7:	Analog input	P60 to P67:	Port 6
ASCK20:	Asynchronous serial input	$\overline{\text{RESET}}$:	Reset
AV_{DD}:	Analog power supply	RxD20:	Receive data
AV_{REF}:	Analog reference voltage	$\overline{\text{SCK20}}$:	Serial clock (for SIO20)
AV_{SS}:	Analog ground	SI20:	Serial input
BZO90:	Buzzer output	SO20:	Serial output
CPT90:	Capture trigger input	$\overline{\text{SS20}}$:	Chip select input
IC0:	Internally connected	TI80, TI81:	Timer input
INTP0 to INTP3:	Interrupt from peripherals	TO80 to TO82, TO90:	Timer output
P00 to P05:	Port 0	TxD20:	Transmit data
P10, P11:	Port 1	V_{DD0}, V_{DD1}:	Power supply
P20 to P26:	Port 2	V_{SS0}, V_{SS1}:	Ground
P30 to P33:	Port 3	X1, X2:	Crystal (main system clock)
P50 to P53:	Port 5	XT1, XT2:	Crystal (subsystem clock)

2. BLOCK DIAGRAM



Remark The internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit I/O port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P10, P11	I/O	Port 1 2-bit I/O port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P20	I/O	Port 2 7-bit I/O port Input/output can be specified in 1-bit units For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by software. Only P23 and P24 can be used as N-ch open-drain I/O port pins.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				–
P24				–
P25				TI80/$\overline{\text{SS20}}$
P26				TO80
P30	I/O	Port 3 4-bit I/O port Input/output can be specified in 1-bit units An on-chip pull-up resistor can be specified by software.	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain I/O port Input/output can be specified in 1-bit units An on-chip pull-up resistor can be specified by a mask option.	Input	–
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0 to ANI7

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
SCK20	I/O	Serial clock input/output for serial interface	Input	P20/ASCK20
SS20	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{\text{SCK20}}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer 80	Input	P25/$\overline{\text{SS20}}$
TI81	Input	External count clock input to 8-bit timer 81	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer 80 output	Input	P26
TO81	Output	8-bit timer 81 output	Input	P31/INTP1
TO82	Output	8-bit timer 82 output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer 90 output	Input	P32/INTP2
BZO90	Output	16-bit timer 90 buzzer output	Input	P33/INTP3/TO82
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
ANI0 to ANI7	Input	A/D converter analog input	Input	P60 to P67
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
V_{DD0}	–	Positive power supply	–	–
V_{DD1}	–	Positive power supply (other than ports)	–	–
V_{SS0}	–	Ground potential	–	–
V_{SS1}	–	Ground potential (other than ports)	–	–
RESET	Input	System reset input	Input	–
IC0	–	Internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–

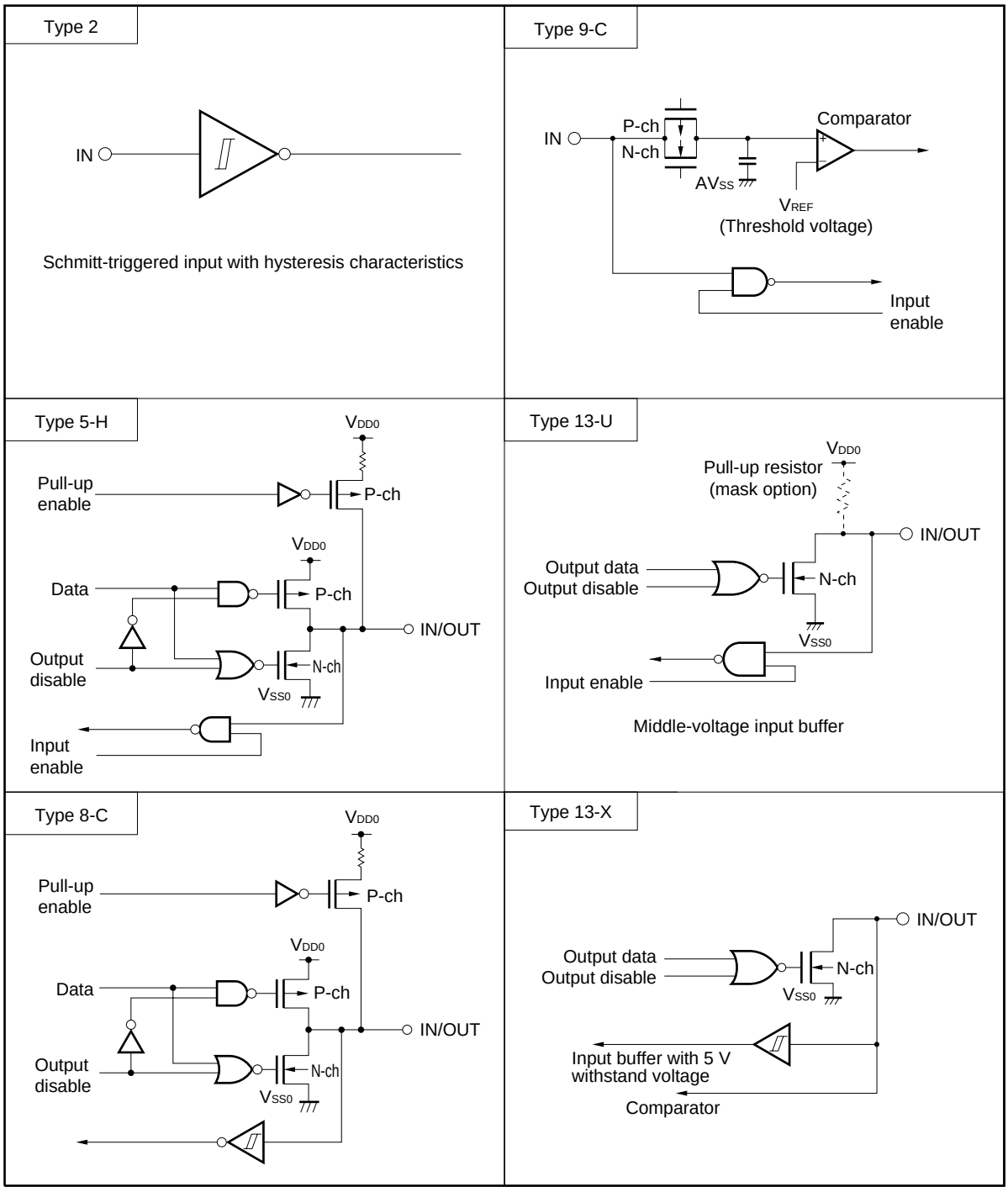
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins is shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P05	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23	13-X		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P24			
P25/TI80/$\overline{SS20}$	8-C		Input: Independently connect to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor. Output: Leave open.
P26/TO80			
P30/INTP0/TI81/CPT90			Input: Independently connect to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P31/INTP1/TO81			
P32/INTP2/TO90			
P33/INTP3/TO82/BZO90			
P50 to P53	13-U		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P60/ANI0 to P67/ANI7	9-C	Input	Connect directly to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1}.
XT1	–	Input	Connect to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC0	–	–	Connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. I/O Circuit Type

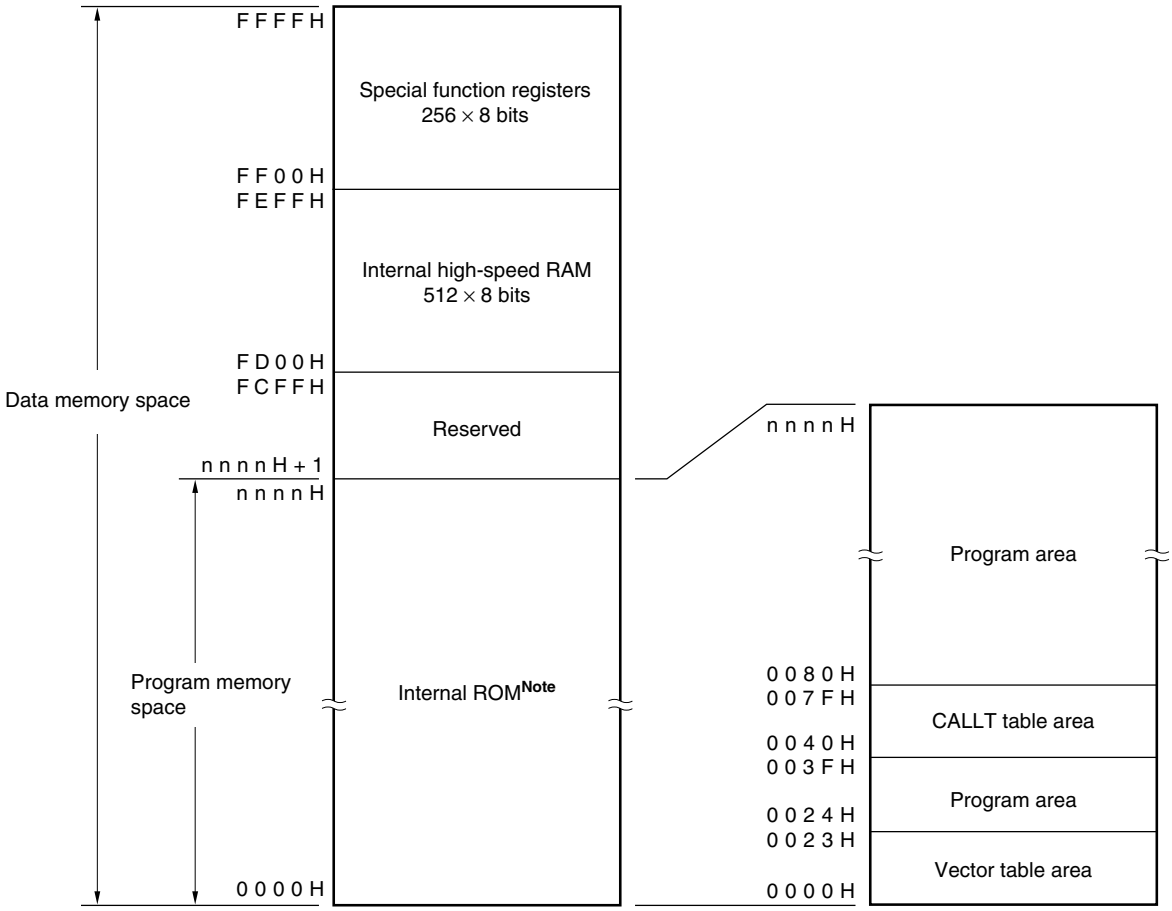


4. MEMORY SPACE

Products in the μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2) can access up to 64 KB of memory space.

Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH
μPD789166(A1), 789176(A1), 789166(A2), 789176(A2)	3FFFH
μPD789167(A1), 789177(A1), 789167(A2), 789177(A2)	5FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following three types of I/O ports are available:

- CMOS input: 8
- CMOS I/O: 17
- N-ch open-drain I/O: 6

Total: 31

Table 5-1. Port Functions

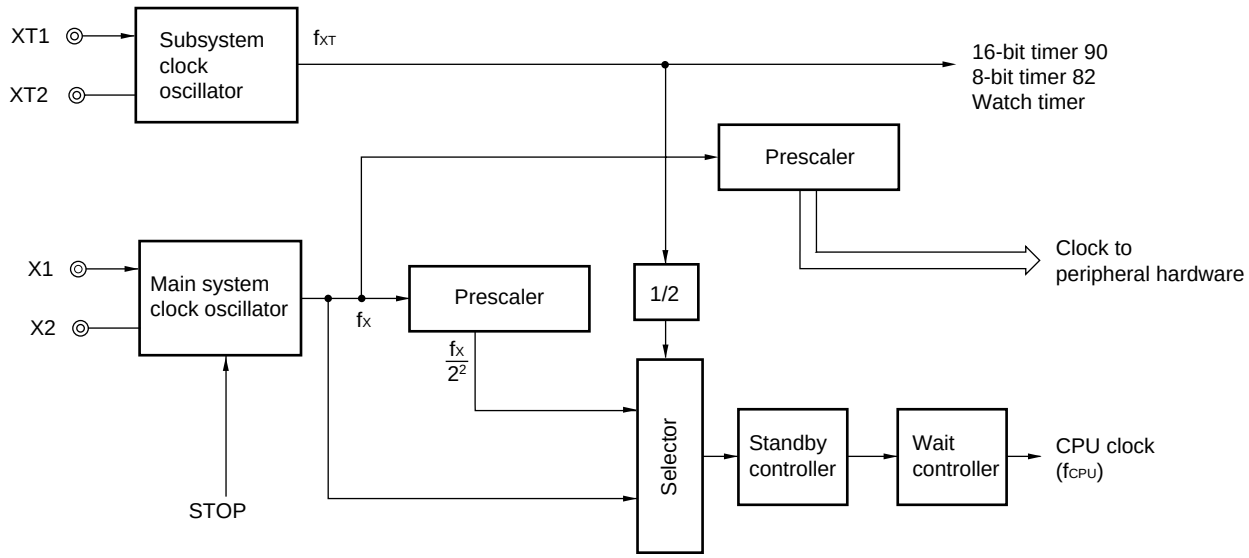
Port Name	Pin Name	Function
Port 0	P00 to P05	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 1	P10, P11	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by software.
Port 2	P20 to P26	I/O port. Input/output can be specified in 1-bit units. For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by means of software. (P23 and P24 are N-ch open-drain I/O ports (with 5 V tolerance).)
Port 3	P30 to P33	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by software.
Port 5	P50 to P53	N-channel open-drain I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a mask option.
Port 6	P60 to P67	Input-only port

5.2 Clock Generator

An on-chip system clock generator is provided.
The minimum instruction execution time can be changed.

- 0.4 μs/1.6 μs (@ 5.0 MHz operation with main system clock)
- 122 μs (@ 32.768 kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Six on-chip timers are provided.

- 16-bit timer 90 (TM90): 1 channel
- 8-bit timer/event counter 80, 81 (TM80, TM81): 2 channels
- 8-bit timer 82 (TM82): 1 channel
- Watch timer (WT): 1 channel
- Watchdog timer (WDT): 1 channel

Table 5-2. Timer Operation

		TM90	TM80	TM81	TM82	WT	WTM
Operation mode	Interval timer	–	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	–	1 channel	1 channel	–	–	–
Function	Timer output	1	1	1	1	–	–
	Square-wave output	–	1	1	1	–	–
	PWM output	–	1	1	1	–	–
	Buzzer output	1	–	–	–	–	–
	Capture	1 input	–	–	–	–	–
	Interrupt request	1	1	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer

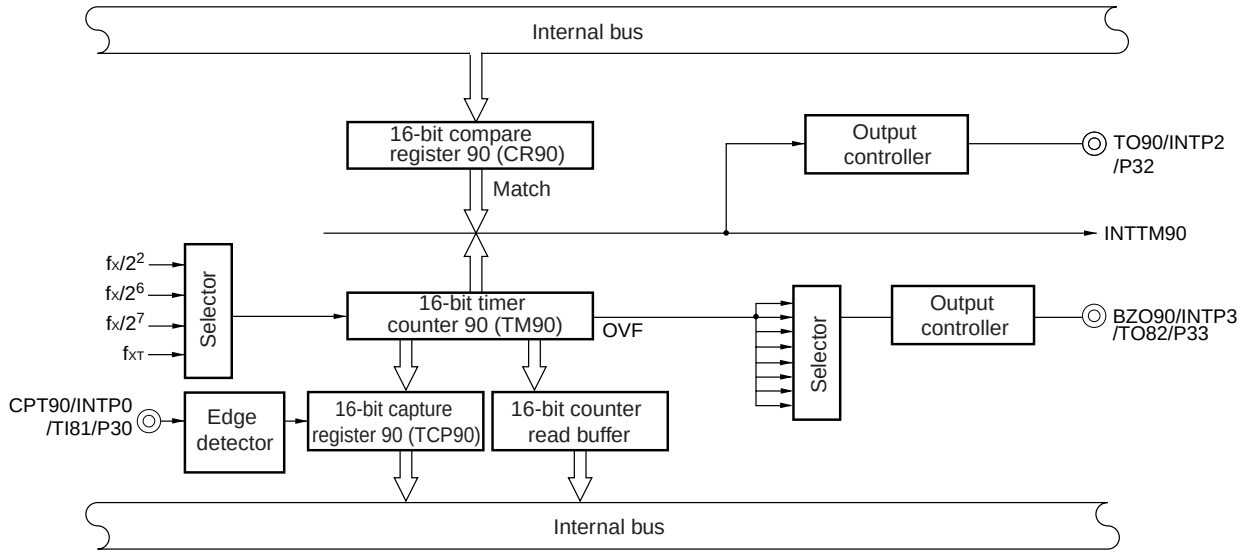


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 80

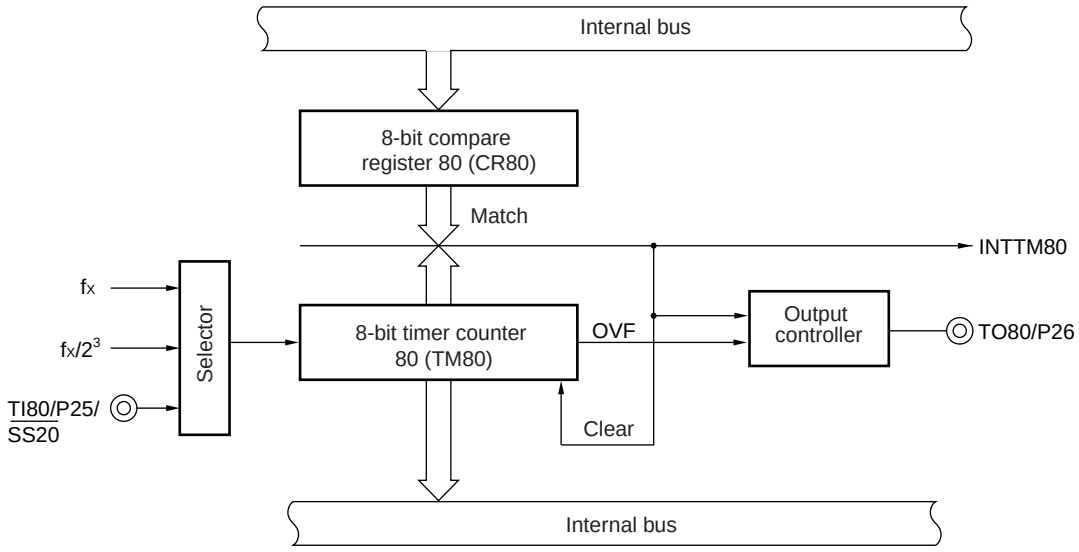


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 81 (TM81)

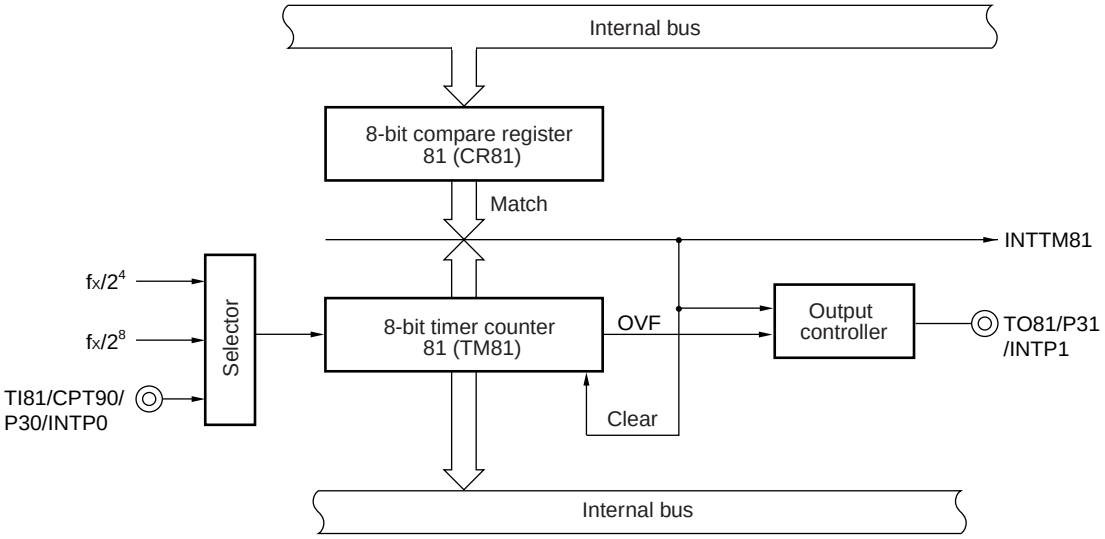


Figure 5-5. Block Diagram of 8-Bit Timer 82 (TM82)

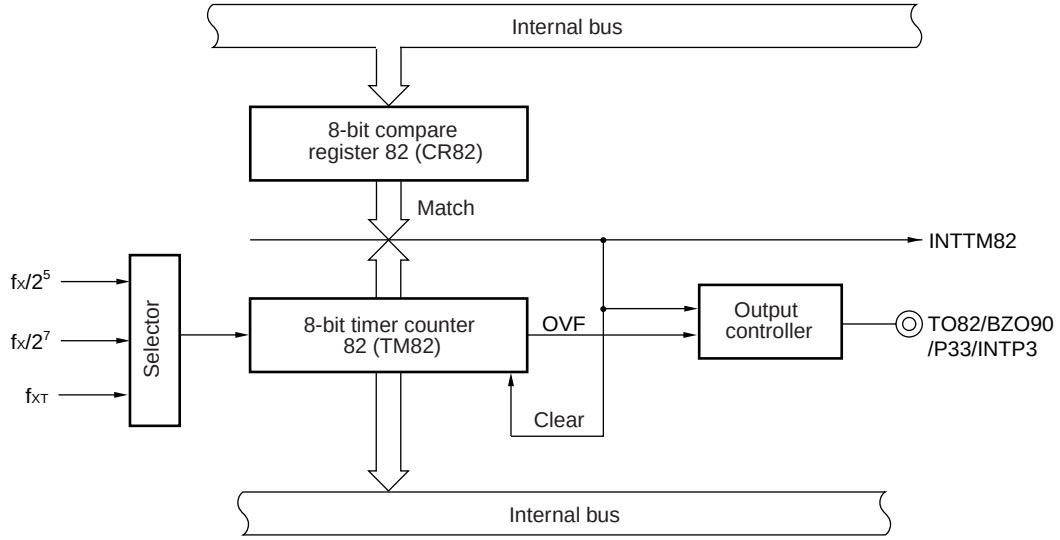
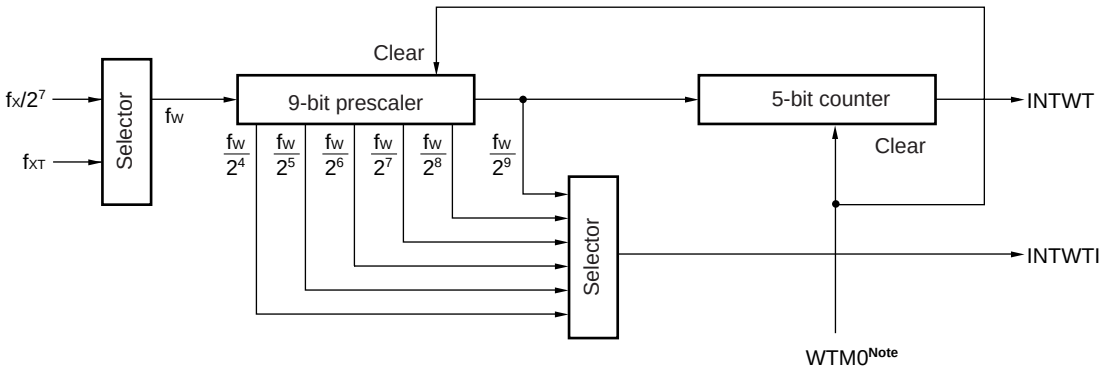
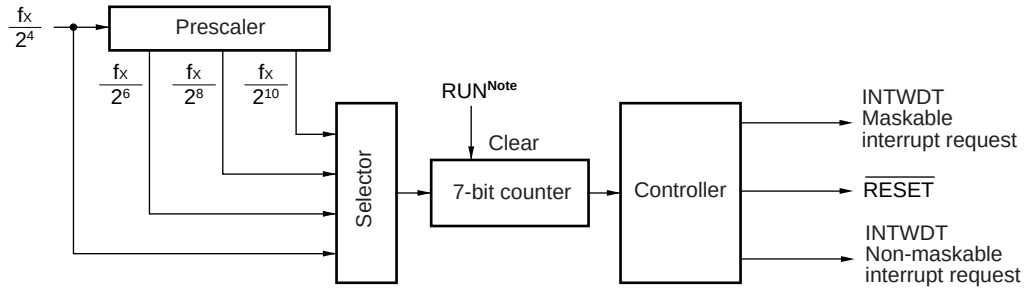


Figure 5-6. Block Diagram of Watch timer



Note Bit 0 of the watch timer mode control register (WTM)

Figure 5-7. Watchdog Timer Block Diagram



Note Bit 7 of the watchdog timer mode control register (WDTM)

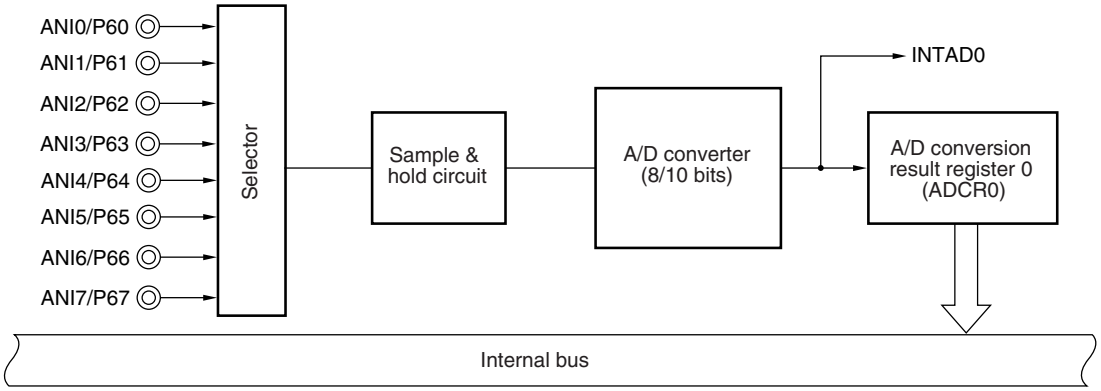
5.4 A/D Converter

The conversion resolution of the A/D converter differs depending on the product as shown below.

- 8-bit A/D converter × 8 channels.... μPD78916x(A1), 78916x(A2)
- 10-bit A/D converter × 8 channels.. μPD78917x(A1), 78917x(A2)

A/D conversion can be only started by software.

Figure 5-8. A/D Converter Block Diagram

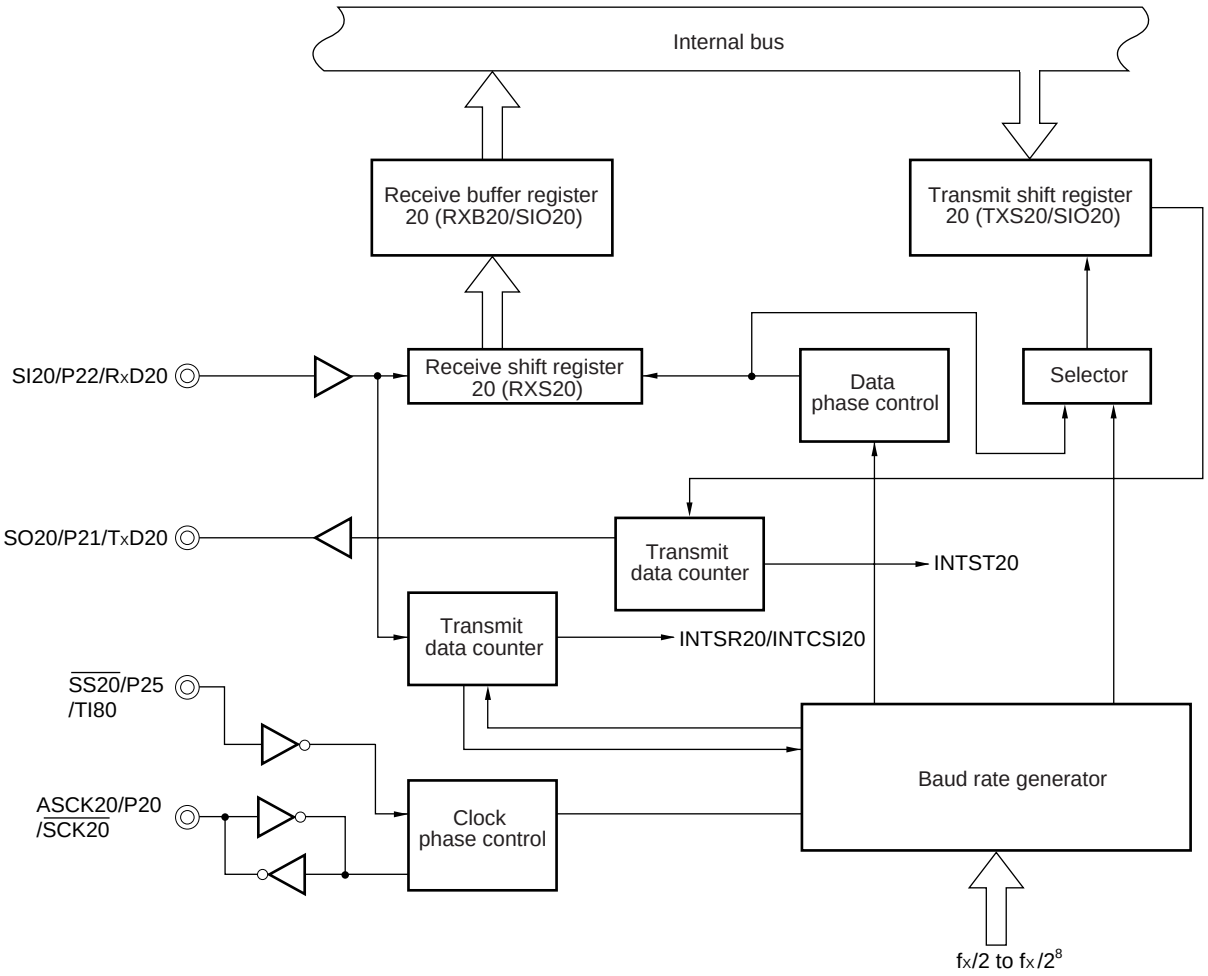


5.5 Serial Interface 20

Serial interface 20 has following three modes:

- Operation stopped mode: Power consumption can be reduced.
- 3-wire serial I/O mode: Switchable between MSB/LSB first
- Asynchronous serial interface (UART) mode: A dedicated baud rate generator is incorporated.

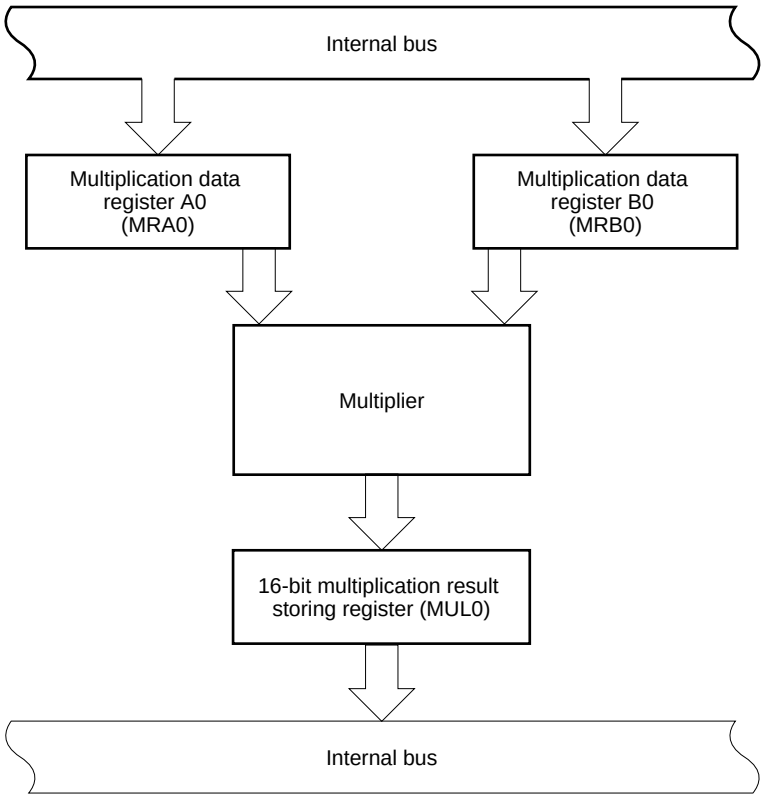
Figure 5-9. Block Diagram of Serial Interface 20



5.6 Multiplier

The calculation of 8 bits × 8 bits = 16 bits can be performed.

Figure 5-10. Multiplier Block Diagram



6. INTERRUPT FUNCTION

A total of 15 interrupt sources are provided, divided into the following two types.

- Non-maskable interrupts: 1
- Maskable interrupts: 14

Table 6-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with the interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR20	End of serial interface 20 UART reception	Internal	000EH	(B)
		INTCSI20	End of serial interface 20 3-wire SIO transfer reception			
	6	INTST20	End of serial interface 20 UART transmission		0010H	
	7	INTWT	Watch timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM80	Generation of match signal of 8-bit timer/event counter 80		0016H	
	10	INTTM81	Generation of match signal of 8-bit timer/event counter 81		0018H	
	11	INTTM82	Generation of match signal of 8-bit timer 82		001AH	
	12	INTTM90	Generation of match signal of 16-bit timer 90		001CH	
	13	INTAD0	A/D conversion completion signal		0022H	

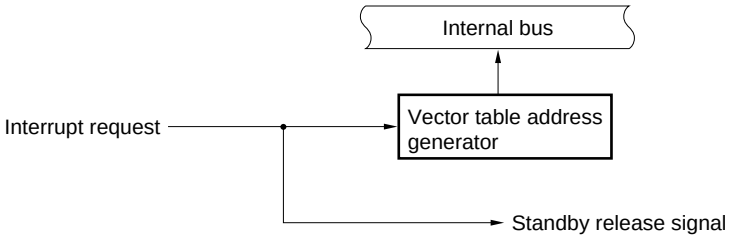
Notes 1. Priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest and 13 is the lowest.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 6-1.

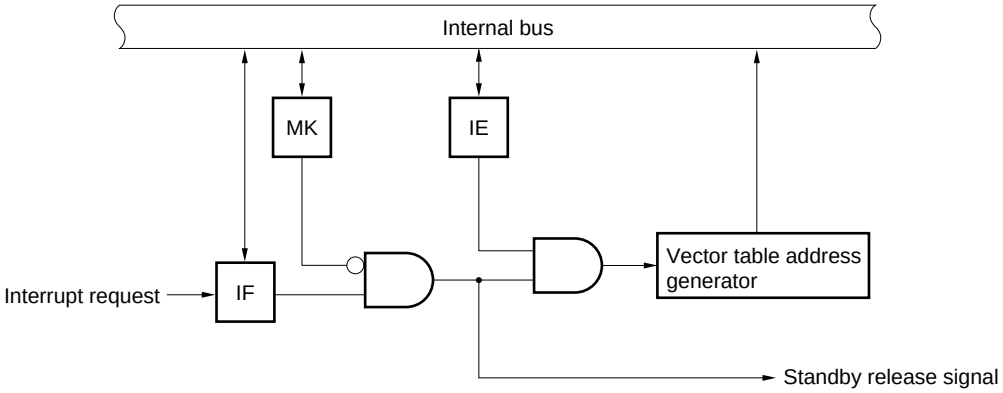
Remark Either a non-maskable interrupt or a maskable interrupt (internal) can be selected as the interrupt source of the watchdog timer (INTWDT).

Figure 6-1. Basic Configuration of Interrupt Function

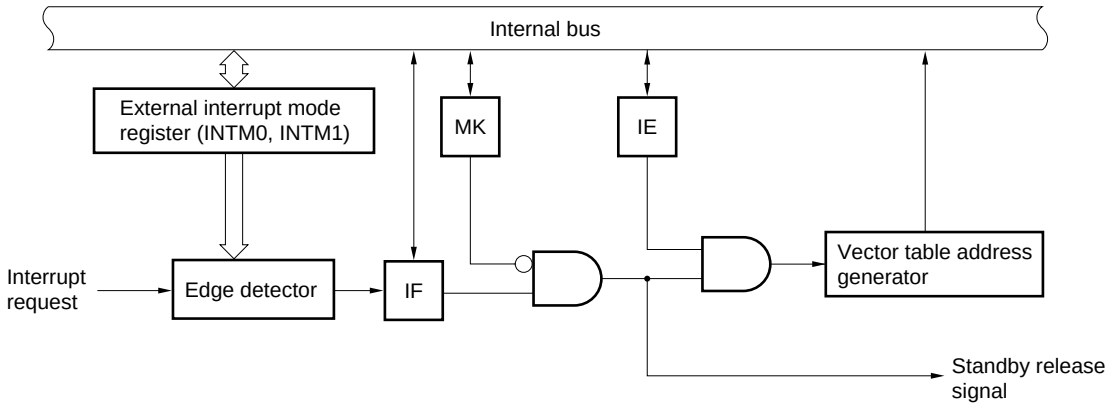
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



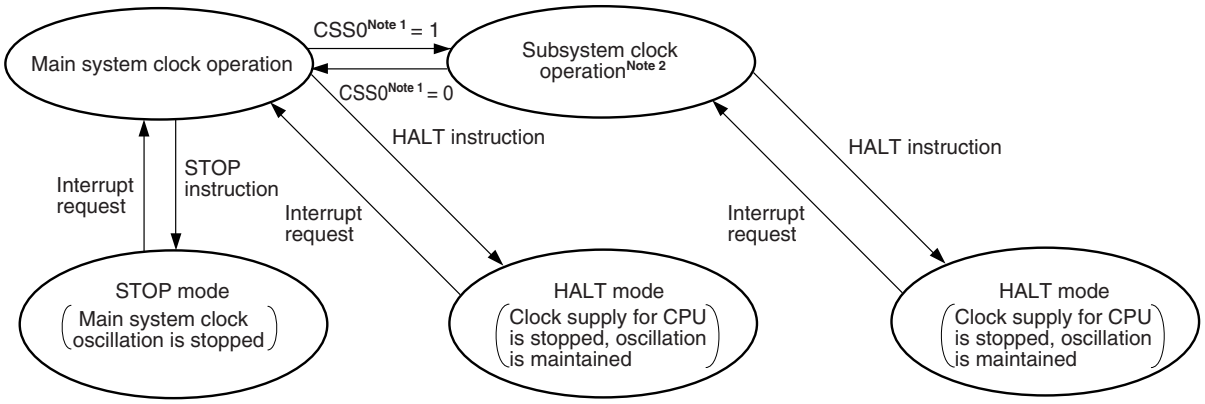
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Figure 7-1. Standby Function



Notes 1. Bit 4 of the sub-clock control register (CSS)

2. The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

8. RESET FUNCTION

The following two reset methods are available.

(1) External reset by $\overline{\text{RESET}}$ signal input
(2) Internal reset by watchdog timer inadvertent program loop time detection.

9. MASK OPTION

The μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2) have the following mask options.

- P50 to P53 mask options
  On-chip pull-up resistors can be selected in bit units
<1> Specifies on-chip pull-up resistors
<2> Does not specify on-chip pull-up resistors

10. INSTRUCTION SET OVERVIEW

This section lists the μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2) instruction set.

10.1 Conventions

10.1.1 Operand identifiers and description methods

Operands are described in the "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 10-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7), AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH immediate data or label FE20H to FF1FH immediate data or label (even address only)
addr16 addr5	0000H to FFFFH immediate data or label (Only even addresses for 16-bit data transfer instructions) 0040H to 007FH immediate data or label (even address only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

10.1.2 Descriptions of the operation field

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Non-maskable interrupt servicing flag
( ):	Memory contents indicated by address or register contents in parentheses
X_H, X_L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
∀:	Exclusive OR
$\overline{\quad}$:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

10.1.3 Description of the flag operation field

(Blank):	Not affected
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is restored

10.2 Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	Flags AC	Flags CY
MOV	r. #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ←→ X			
	A, r Note 2	2	6	A ←→ r			
	A, saddr	2	6	A ←→ (saddr)			
	A, sfr	2	6	A ←→ (sfr)			
	A, [DE]	1	8	A ←→ (DE)			
	A, [HL]	1	8	A ←→ (HL)			
	A, [HL + byte]	2	8	A ←→ (HL+byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except r = A

2. Except r = A, X

3. Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp[Note]	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A+ (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A+ (addr16) +CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A+ (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×

Note Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r– 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ←SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC_H ← (00000000, addr5 + 1) PC_L ← (00000000, addr5) SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP –– 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags
					Z AC CY
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC_H ← A, PC_L ← X	
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr.bit, $saddr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A.bit, $saddr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW.bit $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set Stop Mode	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

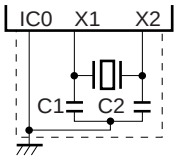
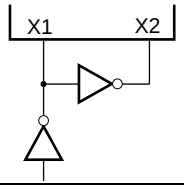
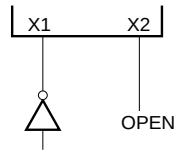
Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$		−0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le AV_{DD} + 0.3\ V$			V
	AV_{REF}	$AV_{REF} \le V_{DD} + 0.3\ V$			V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24		−0.3 to +5.5	V
	V_{I3}	P50 to P53	N-ch open drain	−0.3 to +13	V
			On-chip pull-up resistor	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78916x(A1), 78917x(A1)	−4	mA
		Total for all pins		−14	mA
		Per pin	μPD78916x(A2), 78917x(A2)	−2	mA
		Total for all pins		−6	mA
Output current, low	I_{OL}	Per pin	μPD78916x(A1), 78917x(A1)	5	mA
		Total for all pins		80	mA
		Per pin	μPD78916x(A2), 78917x(A2)	2	mA
		Total for all pins		40	mA
Operating ambient temperature	T_A	μPD78916x(A1), 78917x(A1)		−40 to +110	°C
		μPD78916x(A2), 78917x(A2)		−40 to +125	°C
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

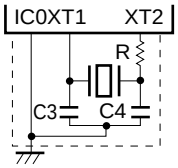
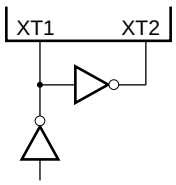
3. For ceramic resonator, use the part number for which the resonator manufacturer guarantees operation under the following conditions.

μPD78916x(A1), 78917x(A1): T_A = 110°C
μPD78916x(A2), 78917x(A2): T_A = 125°C

Remark For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]			1.2	2	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, users are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2))) (1/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78916x(A1), 78917x(A1)			–1	mA
		Total for all pins				–7	mA
		Per pin	μPD78916x(A2), 78917x(A2)			–1	mA
		Total for all pins				–3	mA
Output current, low	I_{OL}	Per pin	μPD78916x(A1), 78917x(A1)			1.6	mA
		Total for all pins				40	mA
		Per pin	μPD78916x(A2), 78917x(A2)			1.6	mA
		Total for all pins				20	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11, P60 to P67		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	N-ch open drain	0.7V_{DD}		10	V
			On-chip pull-up resistor	0.7V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P26, P30 to P33		0.8V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67		0		0.3V_{DD}	V
	V_{IL2}	P50 to P53		0		0.3V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P26, P30 to P33		0		0.2V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2		0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	I_{OH} = –1 mA	V_{DD} – 2.0			V
			I_{OH} = –100 μA	V_{DD} – 1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA			2.0	V
			I_{OL} = 400 μA			1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA			1.0	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2))) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_I = V_{DD}$	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			10	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 10 V Note1	P50 to P53 (N-ch open drain)			80	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			–10	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–10 Note 2	μA
Output leakage current, high	I_{LOH}	$V_O = V_{DD}$				10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	300	kΩ
Mask option pull-up resistor	R_2	V_I = 0 V, P50 to P53		10	30	100	kΩ

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by mask option).

2. A low-level input leakage current of –60 μA (MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 when on-chip pull-up resistors are not connected to P50 to P53 (specified by mask option) and P50 to P53 are set to input mode. At times other than this, a –3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2))) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.0	8.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.0	5.0	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	1200	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	1100	μA
	I_{DD5} Note 1	32.768 kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	1000	μA
	I_{DD6} Note 2	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		3.0	10.0	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and port current (including the current flowing through the internal pull-up resistors) is not included.

2. The AV_{REF}ON (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) is not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

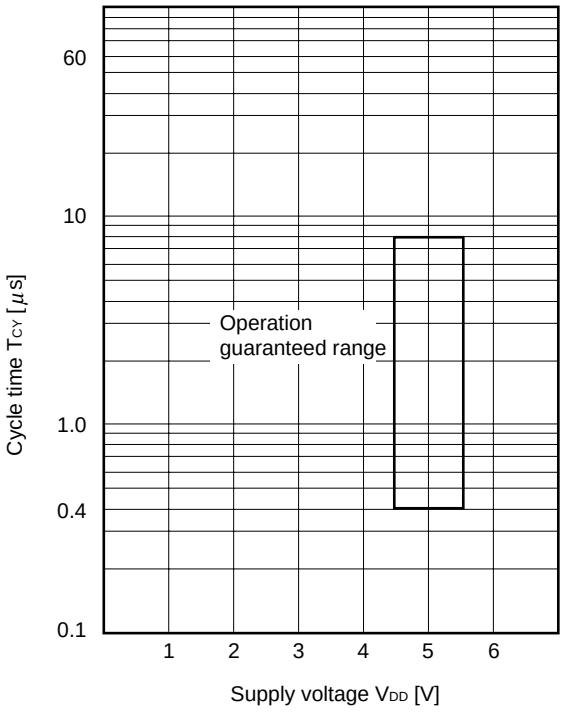
AC Characteristics

(1) Basic operation

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	0.4		8	μs
		Operation based on the subsystem clock	114	122	125	μs
TI80 and TI81 input frequency	f_{TI}		0		4	MHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3	10			μs
$\overline{RESET}$ input low-level width	t_{RSL}		10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD} (main system clock)



(2) Serial interface 20

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		900			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}				120	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}				240	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

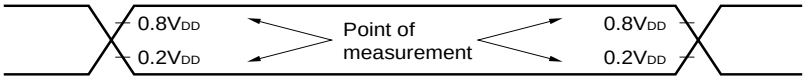
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

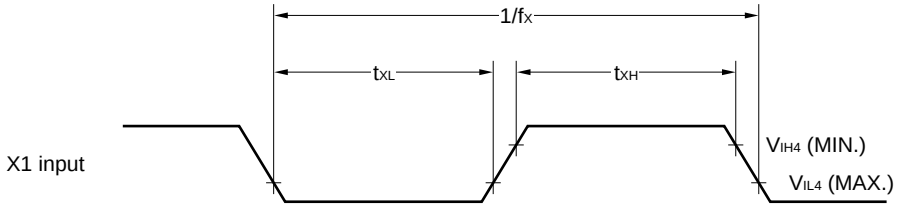
(d) UART mode (external clock input)

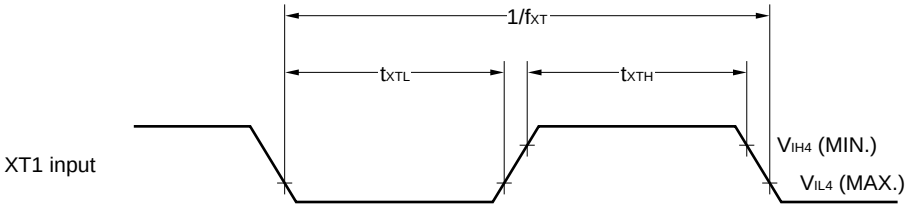
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		900			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

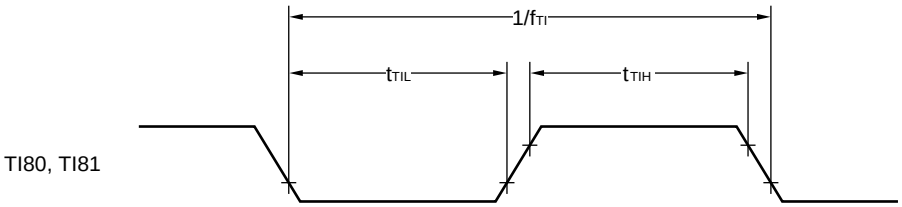


Clock Timing

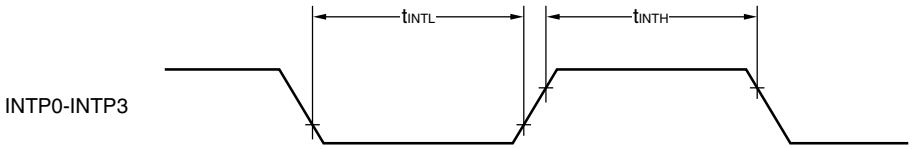




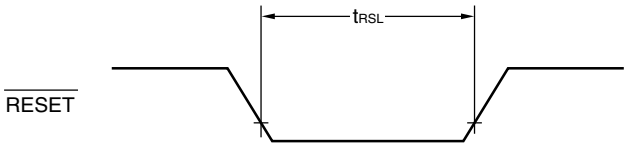
TI Timing



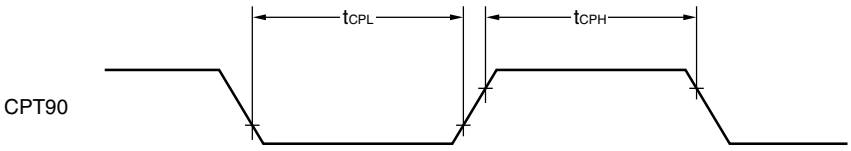
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

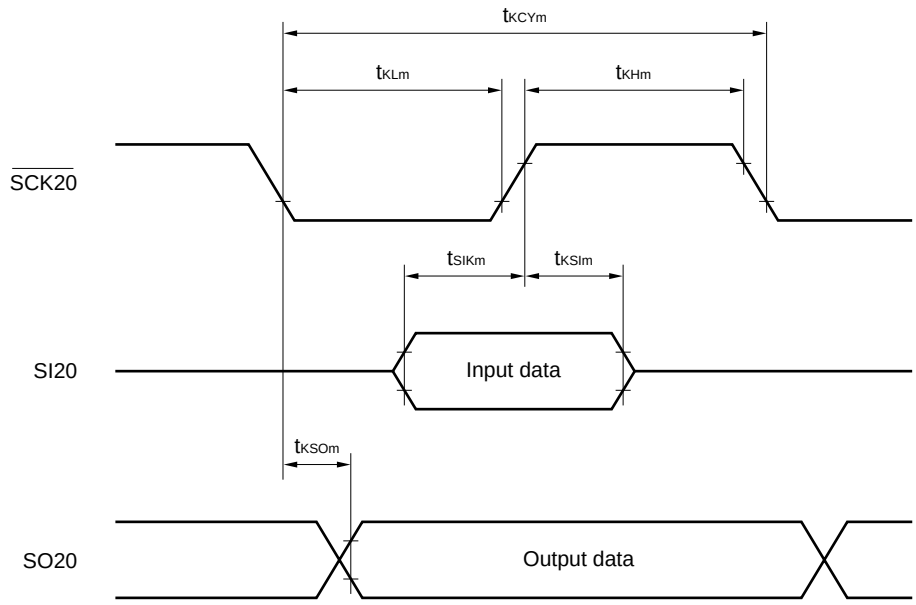


CPT90 Input Timing



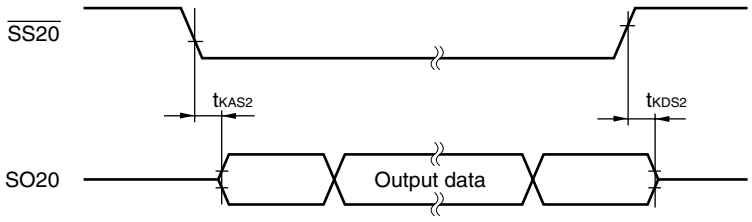
Serial Transfer Timing

3-wire serial I/O mode:

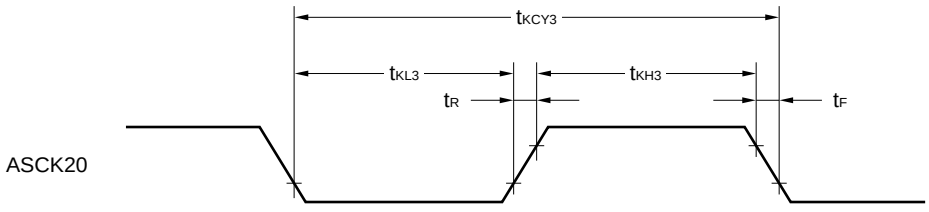


Remark m = 1, 2

3-wire serial I/O mode (when using $\overline{\text{SS20}}$):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78916x(A1), 78916x(A2))

(T_A = –40 to +110°C (μPD78916x(A1)), –40 to +125°C (μPD78916x(A2))

4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]				±0.4	±1.0	%FSR
Conversion time	t_{CONV}		14		28	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full scale range

10-Bit A/D Converter Characteristics (μPD78917x(A1), 78917x(A2))

(T_A = –40 to +110°C (μPD78917x(A1)), –40 to +125°C (μPD78917x(A2))

4.5 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]				±0.4	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Note]					±0.6	%FSR
Full-scale error[Note]					±0.6	%FSR
Integral linearity error[Note]	INL				±4.5	LSB
Differential linearity error[Note]	DNL				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{AIREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Data Memory Stop Mode Low Power Supply Voltage Data Retention Characteristics
(T_A = –40 to +110°C (μPD78916x(A1), 78917x(A1)),
= –40 to +125°C (μPD78916x(A2), 78917x(A2)))

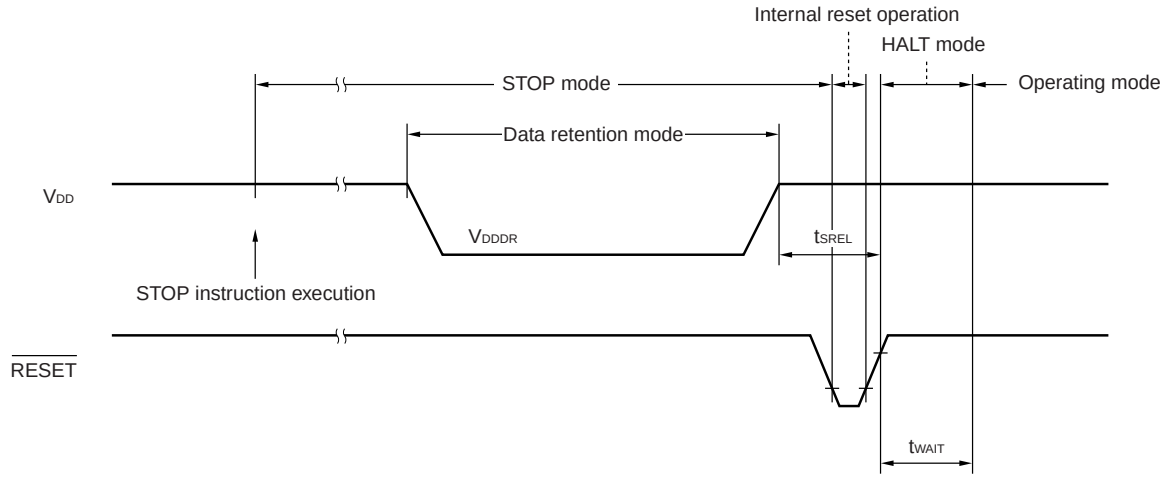
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		4.5		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

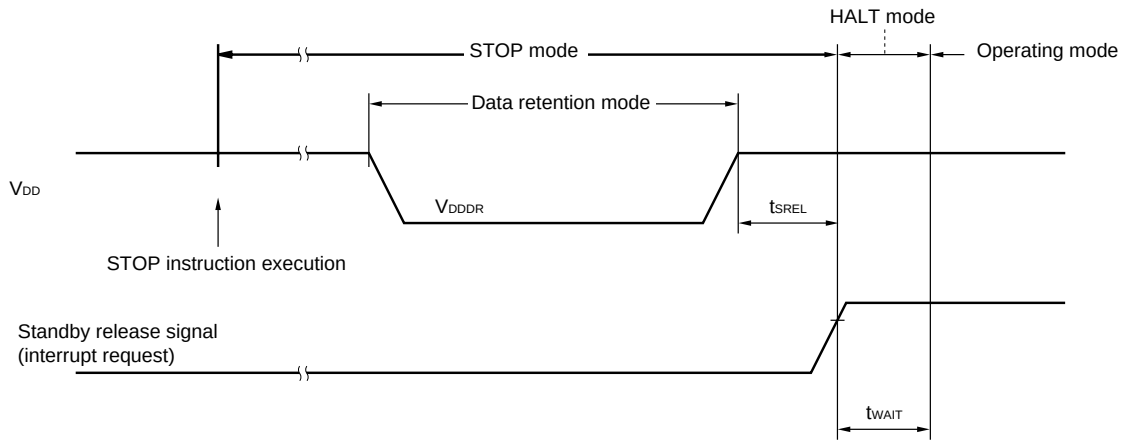
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected by using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



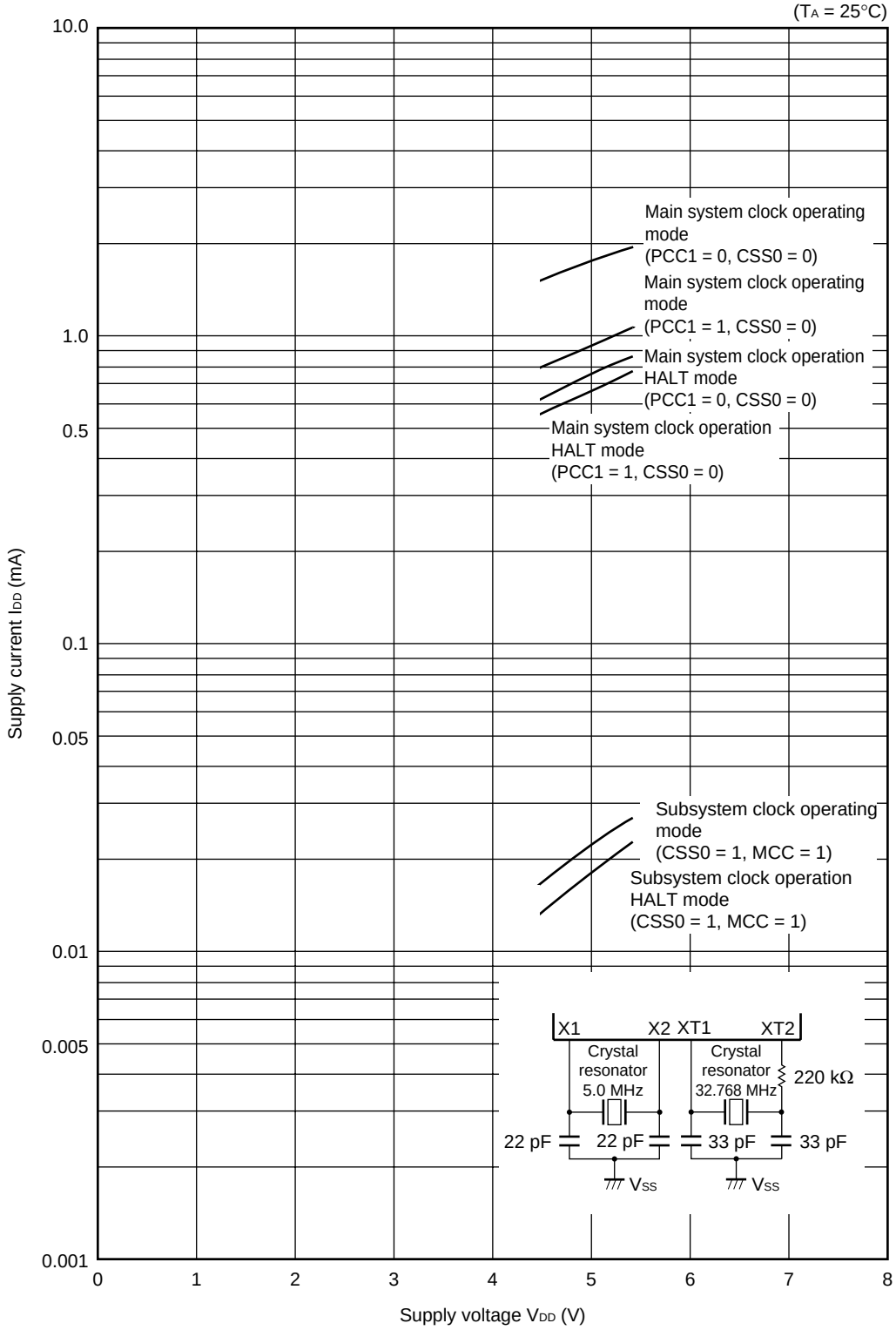
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



12. CHARACTERISTICS CURVES

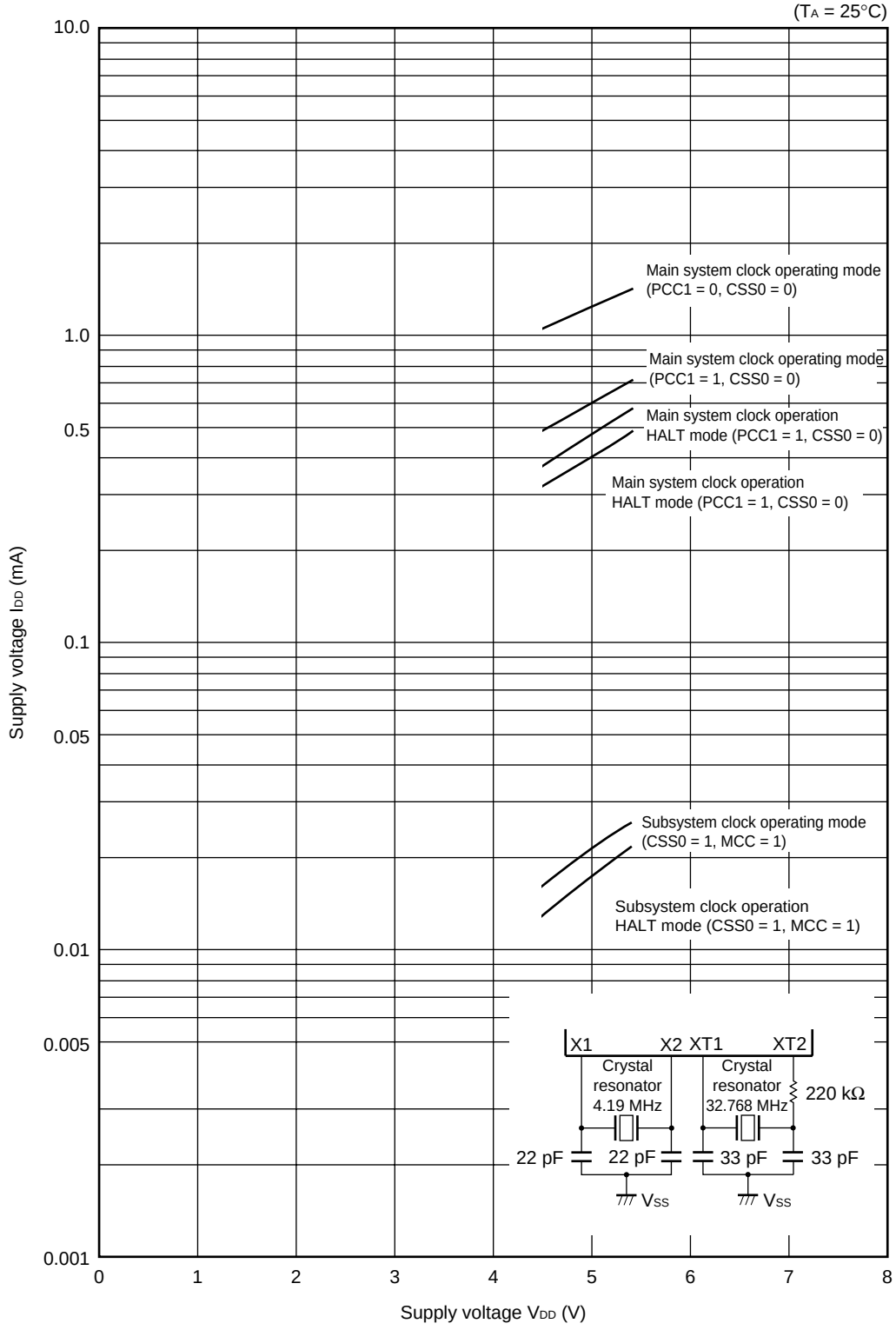
I_{DD} vs. V_{DD} (f_X = 5.0 MHz, f_{XT} = 32.768 kHz)

(T_A = 25°C)



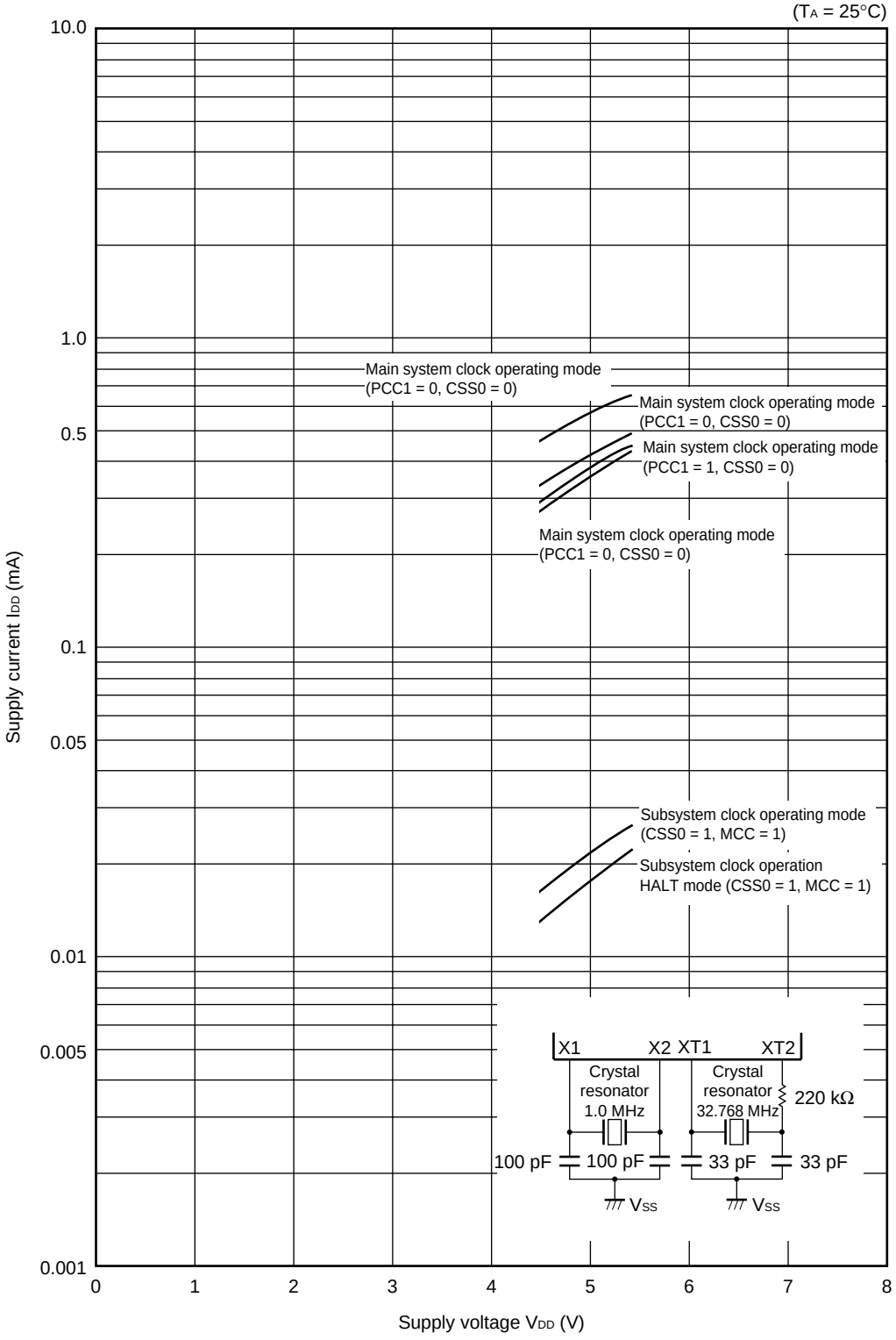
I_{DD} vs. V_{DD} (f_X = 4.19 MHz, f_{XT} = 32.768 kHz)

(T_A = 25°C)



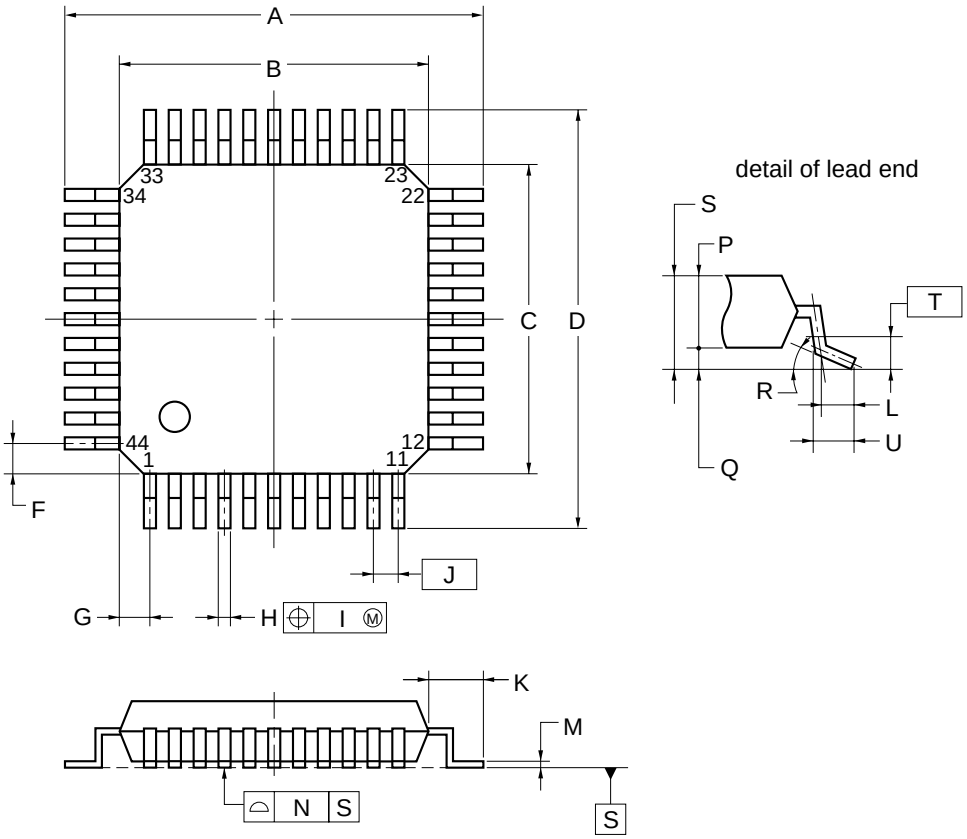
I_{DD} vs. V_{DD} (f_X = 1.0 MHz, f_{XT} = 32.768 kHz)

(T_A = 25°C)



13. PACKAGE DRAWING

44 PIN PLASTIC QFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2) should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD789166GB(A1)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167GB(A1)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176GB(A1)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177GB(A1)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789166GB(A2)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789167GB(A2)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789176GB(A2)-xxx-8ES: 44-pin plastic LQFP (10 × 10)
μPD789177GB(A2)-xxx-8ES: 44-pin plastic LQFP (10 × 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2).

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789177[Notes 1, 2, 3]	Device file for μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2)
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No.: FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated for on-chip flash memory microcontrollers
FA-44GB-8ES[Note 4]	Flash memory programming adapter for 44-pin plastic LQFP (GB-8ES type)

Debugging Tools

IE-78K0S-NS In-circuit emulator		In-circuit emulator used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter		Adapter used to supply power from a 100 to 240 V AC outlet
IE-70000-98-IF-C Interface adapter		Adapter required when using the PC-9800 series (excluding notebook PCs) as the host machine for the IE-78K0S-NS (C bus supported)
IE-70000-CD-IF-A PC card interface		PC card and interface cable required when using a notebook PC as the host machine for the IE-78K0S-NS (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter		Adapter required when using an IBM PC/AT™ or compatible as the host machine for the IE-78K0S-NS (ISA bus supported)
IE-70000-PCI-IF Interface adapter		Adapter required when using a PC equipped with a PCI bus as the host machine for the IE-78K0S-NS
IE-789177-NS-EM1 Emulation board		Emulation board used to emulate the peripheral hardware specific to the device. This is used in combination with the in-circuit emulator.
NP-44GB[Note 4] Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the EV-9200G-44.
	EV-9200G-44 conversion socket	Conversion socket to connect the target system board on which a 44-pin plastic LQFP can be mounted and the NP-44GB
NP-44GB-TQ[Note 4] Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the TGB-044SAP.
	TGB-044SAP[Note 5] conversion socket	Conversion socket to connect the target system board on which a 44-pin plastic LQFP can be mounted and the NP-44GB-TQ
SM78K0S[Notes 1, 2]		System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]		Integrated debugger common to 78K/0S Series
DF789177[Notes 1, 2]		Device file for μPD78916x(A1), 78917x(A1), 78916x(A2), and 78917x(A2)

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on the PC-9800 series (Japanese Windows™)

2. Based on IBM PC/AT and compatibles (Japanese Windows/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Soraris™), and NEWS™ (NEWS-OS™)

4. Product made by and available from Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).

5. Product made by TOKYO ELETECH CORPORATION.
Refer to: Daimaru Kogyo, Ltd.
Tokyo Electronic Division (+81-3-3820-7112)
Osaka Electronic Division (+81-6-6244-6672)

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789177.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.
μPD789166, 167, 176, 177, 166Y, 167Y, 176Y, 177Y, 166(A), 167(A), 176(A), 177(A), 166Y(A), 167Y(A), 176Y(A), 177Y(A) Data Sheet	U14017E
μPD789166(A1), 167(A1), 176(A1), 177(A1), 166(A2), 167(A2), 176(A2), 177(A2) Data Sheet	This manual
μPD78F9177, 78F9177Y Data Sheet	U14022E
μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual	U14186E
78K/0S Series Instructions User's Manual	U11047E

Document Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S System Simulator Windows based	Reference	U11489E
SM78K0S, SM78K0 System Simulator Ver.2.10 or later Windows based	Operation	U14611E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092E
ID78K0S-NS Integrated Debugger Windows based	Reference	U12901E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or later Windows based	Operation	U14910E
IE-789177-NS-EM1 Emulation Board		U14621E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
OS for 78K/0S Series MX78K0S	Fundamental	U12938E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Device	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 02-2719-5951

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Tel: 55-11-6462-6810
Fax: 55-11-6462-6829

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