PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD789841, 789842

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD789841 and μPD789842 are μPD789842 subseries products of the 78K/0S series.

These microcontrollers incorporate an inverter control timer being suitable for controlling general-purpose inverters.

The μPD78F9842, a product with on-chip flash memory which can operate on the same supply voltage as for masked ROM products and various development tools are also under development.

Detailed descriptions of their functions, etc., are given in the following user's manuals. Be sure to read them for design purposes.

μPD789842 Subseries User's Manual : To be prepared
78K/0S Series User's Manual, Instruction : U11047E

FEATURES

- On-chip ROM and RAM

Item / Product name	Program memory (ROM)	Data memory (Internal high-speed RAM)	Package
μPD789841	8K bytes	256 bytes	44-pin plastic QFP (10 × 10 mm)
μPD789842	16K bytes		

- Minimum instruction execution time can be switched between high speed (0.24 μs) and low speed (0.96 μs) (when the system clock operates at 8.38 MHz).
- I/O port: 30
- Timer: 6 channels
  - 10-bit inverter control timer: 1 channel
  - 8-bit timer/event counter : 2 channels
  - 8-bit timer counter : 1 channel
  - Watch timer : 1 channel
  - Watchdog timer : 1 channel
- 8-bit resolution A/D converter: 8 channels
- Serial interface (UART00): 1 channel
- Multiplier: 10 bits × 10 bits = 20 bits
- SWAP: The contents of the high-order four bits of an 8-bit register can be exchanged with the low-order four bits.
- Vectored interrupt source: 14
- Supply voltage: V_{DD} = 4.0 to 5.5 V

APPLICATIONS

Inverter-driven air conditioners, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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Date Published November 1998 J CP(K)
Printed in Japan

ORDERING INFORMATION

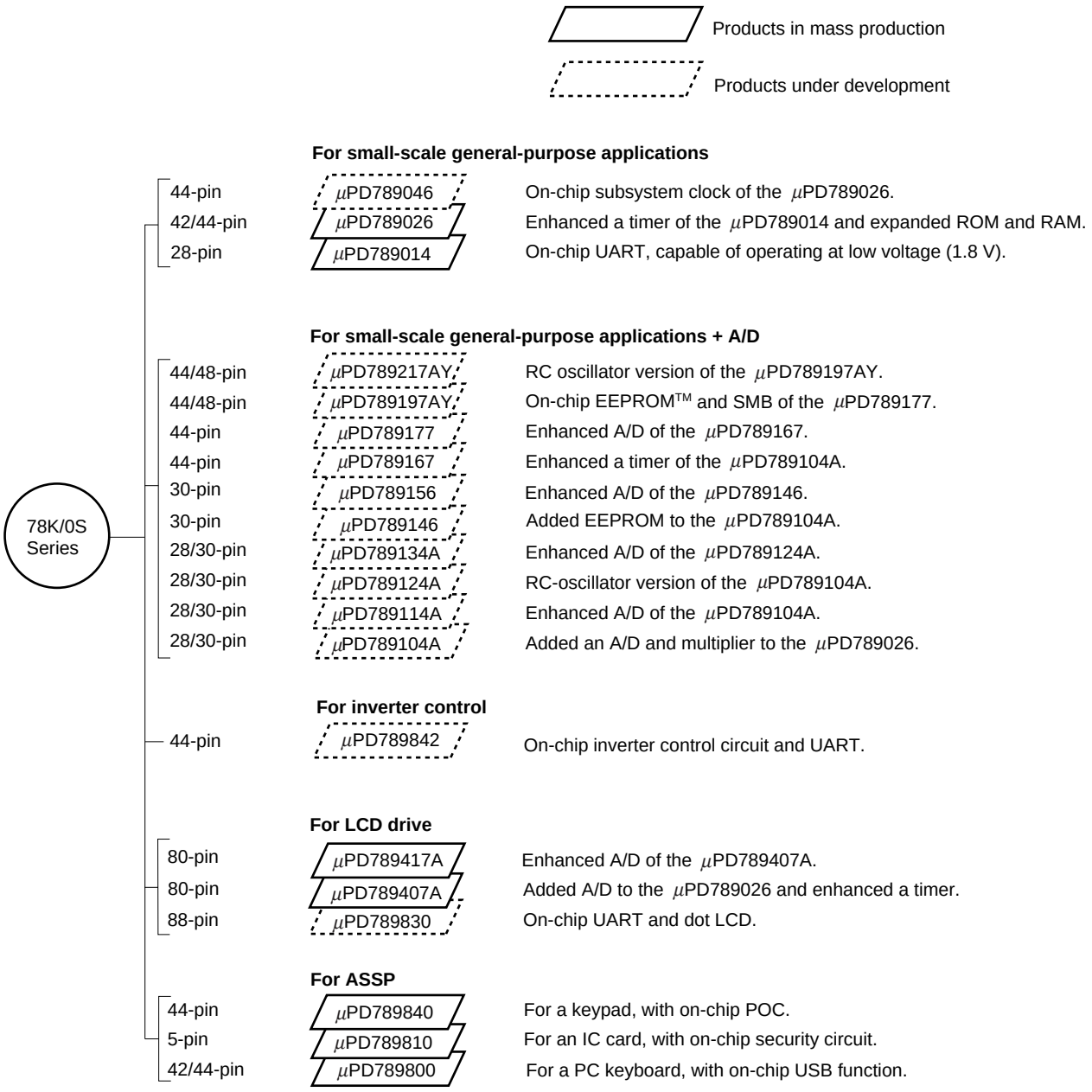
Part number	Package
μPD789841GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, package height: 2.7 mm)
μPD789841GB-×××-8ES	44-pin plastic QFP (10 × 10 mm, package height: 1.4 mm)
μPD789842GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, package height: 2.7 mm)
μPD789842GB-×××-8ES	44-pin plastic QFP (10 × 10 mm, package height: 1.4 mm)

Remark ××× indicates ROM code suffix.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

78K/0S SERIES DEVELOPMENT

The 78K/0S series products are shown below. The subseries names are indicated in frames.



The following table lists the major differences in functions between the subseries.

Subseries \ Function		ROM size	Timer				8-bit A/D	10-bit A/D	Serial interface	I/O	Remarks
			8-bit	16-bit	Clock	WDT					
Small-scale, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	-	-	1 ch (UART: 1 ch)	34 pins	-
	μPD789026	4 K-16 K			-						
	μPD789014	2 K-4 K	2 ch	-						22 pins	
Small-scale, general-purpose applications and A/D function	μPD789217AY	16 K-24 K	3 ch	1 ch	1 ch	1 ch	-	8 ch	2 ch [UART: 1 ch, SMB : 1 ch]	31 pins	RC-oscillator version, with built-in EEPROM
	μPD789197AY										With built-in EEPROM
	μPD789177								1 ch (UART: 1 ch)		-
	μPD789167						8 ch	-			
	μPD789156	8 K-16 K	1 ch		-		-	4 ch		20 pins	With built-in EEPROM
	μPD789146						4 ch	-			
	μPD789134A	2 K-8 K					-	4 ch			RC-oscillator version
	μPD789124A						4 ch	-			
	μPD789114A						-	4 ch			-
	μPD789104A						4 ch	-			
Inverter control	μPD789842	8 K - 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	-	1 ch (UART: 1 ch)	30 pins	-
LCD driving	μPD789417A	12 K-24 K	3 ch	1 ch	1 ch	1 ch	-	7 ch	1 ch (UART: 1 ch)	43 pins	-
	μPD789407A						7 ch	-			
	μPD789830	24 K	1 ch				-			30 pins	
ASSP	μPD789840	8 K	2 ch	-	-	1 ch	4 ch	-	1 ch	29 pins	-
	μPD789810	6 K	-				-		-	1 pin	With built-in EEPROM
	μPD789800	8 K	2 ch						2 ch (USB: 1 ch)	31 pins	-

Note 10-bit timer: 1 channel

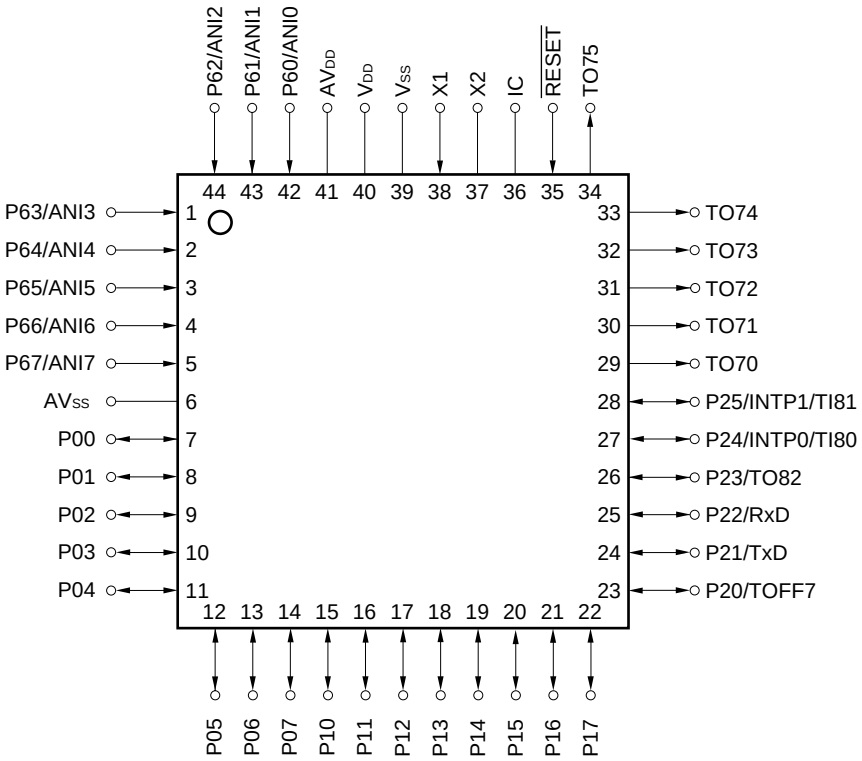
FUNCTIONS

Item		μPD789841	μPD789842
Internal memory	ROM	8K bytes	16K bytes
	High-speed RAM	256 bytes	
Minimum instruction execution time		0.24 μs/0.96 μs (when the system clock operates at 8.38 MHz)	
General-purpose register		8 bits × 8 registers	
Instruction set		• 16-bit operation • Bit manipulation (set, reset, and test) etc.	
I/O ports		Total of 30 port pins 22 CMOS input/output pins 8 CMOS input pins	
Timer		• 10-bit inverter control timer : 1 channel • 8-bit timer/event counter : 2 channels • 8-bit timer counter : 1 channel • Watch timer : 1 channel • Watchdog timer : 1 channel	
A/D converters		Eight channels with 8-bit resolution	
Serial interface		UART: 1 channel	
Multiplier		10 bits × 10 bits = 20 bits	
SWAP		The contents of the high-order four bits of an 8-bit register can be exchanged with the low-order four bits.	
Vector interrupt source	Maskable	Internal: 11, external: 2	
	Nonmaskable	Internal: 1	
Power supply voltage		V_{DD} = 4.0 to 5.5 V	
Operating ambient temperature		T_A = -40°C to +85°C	
Package		44-pin plastic QFP (10 × 10 mm)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

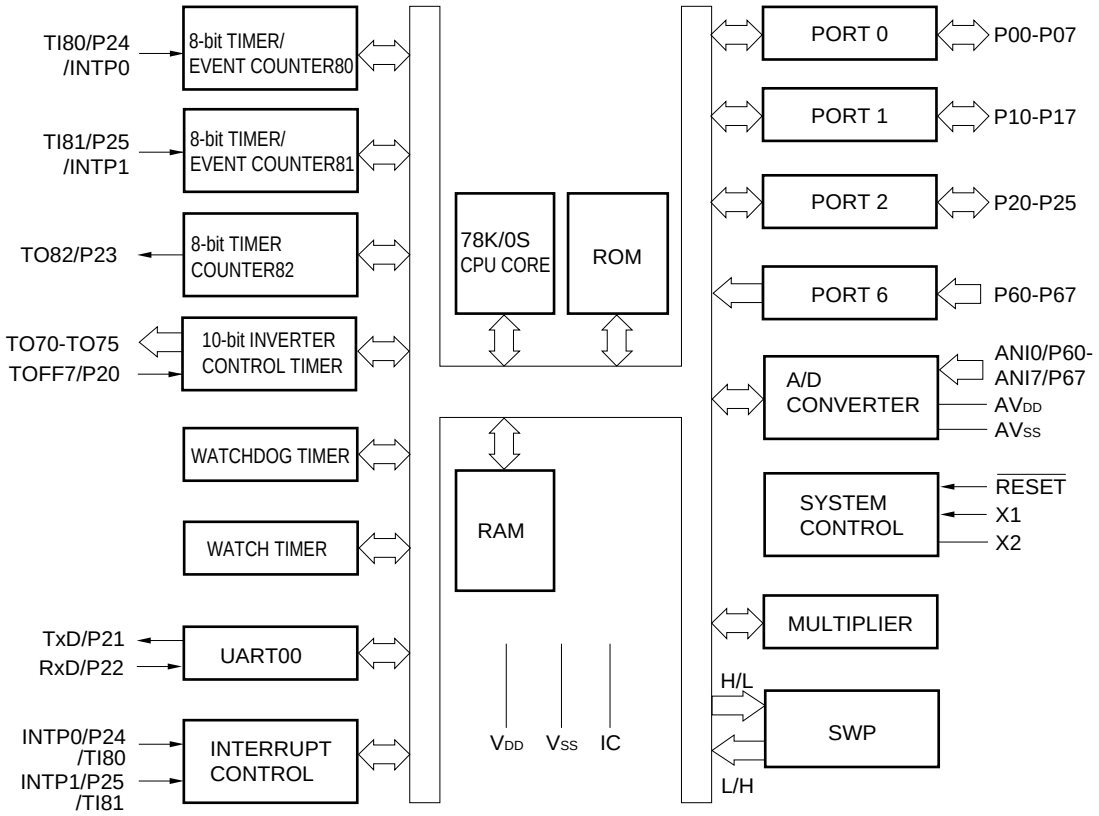
- 44-pin plastic QFP
  μPD789841GB-×××-3BS-MTX (10 × 10 mm, package height: 2.7 mm)
  μPD789841GB-×××-8ES (10 × 10 mm, package height: 1.4 mm)
  μPD789842GB-×××-3BS-MTX (10 × 10 mm, package height: 2.7 mm)
  μPD789842GB-×××-8ES (10 × 10 mm, package height: 1.4 mm)



Cautions 1. Connect the IC (Internally Connected) pin directly to the V_{SS} pin.
2. Connect the AV_{DD} pin to the V_{DD} pin.
3. Connect the AV_{SS} pin to the V_{SS} pin.

ANI0 to ANI7	: Analog input	$\overline{\text{RESET}}$	: Reset
AV_{DD}	: Analog power supply	RxD	: Receive data
AV_{SS}	: Analog ground	TI80, TI81	: Timer input
IC	: Internally connected	TO70 to TO75, TO82	: Timer output
INTP0, INTP1	: Interrupt from peripherals	TOFF7	: Timer output off
P00 to P07	: Port 0	TxD	: Transmit data
P10 to P17	: Port 1	V_{DD}	: Power supply
P20 to P25	: Port 2	V_{SS}	: Ground
P60 to P67	: Port 6	X1, X2	: Crystal

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin name	I/O	Function	When reset	Also used as
P00-P07	I/O	Port 0 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.	Input	-
P10-P17	I/O	Port 1 8-bit input/output port Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.	Input	-
P20	I/O	Port 2 6-bit input/output port Input or output is specifiable bit by bit. The use of on-chip pull-up resistors can be specified by software.	Input	TOFF7
P21				TxD
P22				RxD
P23				TO82
P24				INTP0/TI80
P25				INTP1/TI81
P60-P67	Input	Port 6 8-bit input-only port	Input	ANI0-ANI7

3.2 Non-Port Pins

Pin name	I/O	Function	When reset	Also used as
INTP0	Input	External interrupt input for which effective edges (rising and/or falling edges) can be specified	Input	P24/TI80
INTP1				P25/TI81
RxD	Input	Serial data input to asynchronous serial interface	Input	P22
TxD	Output	Serial data output from asynchronous serial interface	Input	P21
TO70-TO75	Output	10-bit inverter control timer output	Output	-
TOFF7	Input	External input to stop timer output (TO70 to TO75)	Input	P20
TI80	Input	External count clock input to TM80	Input	P24/INTP0
TI81		External count clock input to TM81		P25/INTP1
TO82	Output	TM82 timer output	Input	P23
ANI0-ANI7	Input	A/D converter analog input	Input	P60-P67
AV_{SS}	-	A/D converter ground potential	-	-
AV_{DD}		A/D converter analog power supply	-	-
X1	Input	Connected to crystal for system clock oscillation	-	-
X2	-		-	-
$\overline{RESET}$	Input	System reset input	Input	-
V_{DD}	-	Positive supply voltage for ports	-	-
V_{SS}	-	Ground potential for ports	-	-
IC	-	Internally connected. Connect this pin directly to V_{SS}.	-	-

3.3 Pin Input/Output Circuits and Handling of Unused Pins

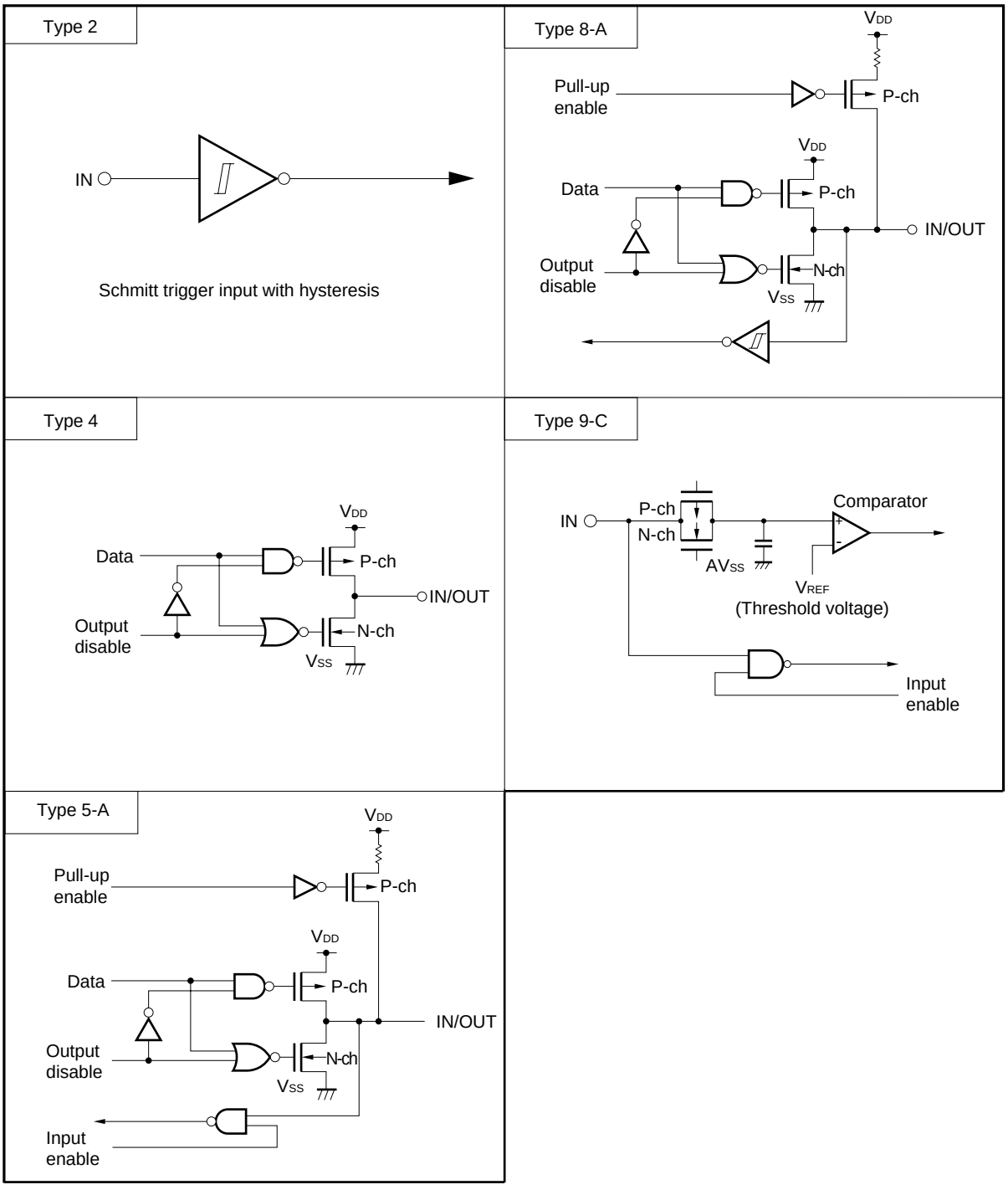
Table 3-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.

Figure 3-1 shows the configuration of each type of input/output circuit.

Table 3-1. Type of Input/Output Circuit for Each Pin

Pin name	I/O circuit type	I/O	Recommended connection of unused pins
P00-P07	5-A	I/O	Input : Connect these pins separately to V_{DD} or V_{SS} via respective resistors. Output : Leave these pins open.
P10-P17			
P20/TOFF7	8-A		
P21/TxD			
P22/RxD			
P23/TO82			
P24/INTP0/TI80			
P25/INTP1/TI81			
P60/ANI0-P67/ANI7	9-C	Input	Connect this pin directly to V_{DD} or V_{SS}.
TO70-TO75	4	Output	Connect this pin to V_{DD} or V_{SS} via respective resistors.
$\overline{\text{RESET}}$	2	Input	-
IC	-	-	Connect this pin directly to V_{SS}.

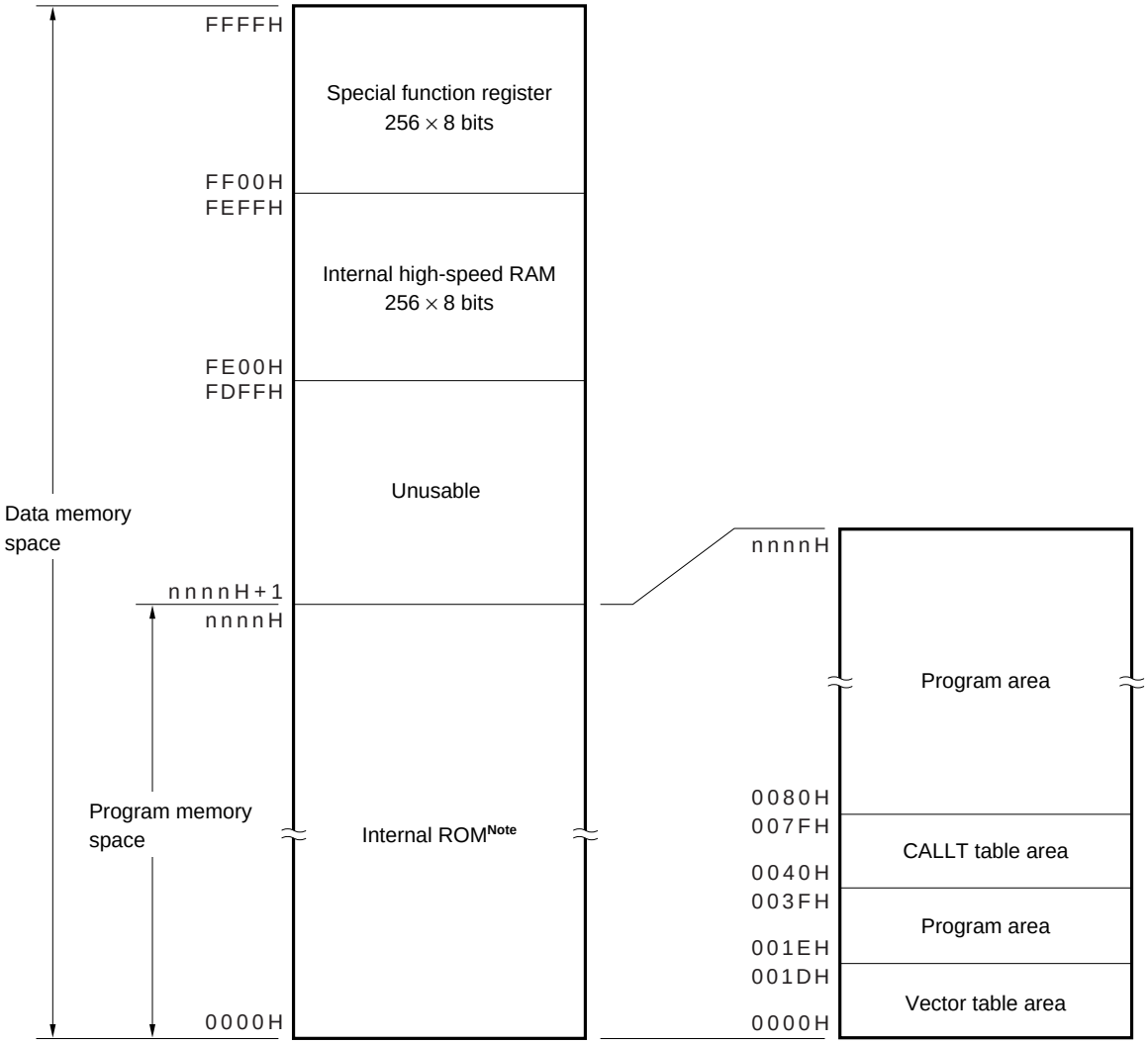
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The μPD789841 and μPD789842 can each access up to 64K bytes of memory space. Figure 4-1 shows the memory map of the μPD789841 and μPD789842.

Figure 4-1. Memory Map



Note The internal ROM size varies with products (as shown in the table below).

Product name	End address of internal ROM nnnnH
μPD789841	1FFFH
μPD789842	3FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

I/O ports are listed below.

- CMOS input/output ports (ports 0 to 2): 22 pins
- CMOS input port (port 6): 8 pins

Table 5-1. Port Functions

Name	Pin name	Function
Port 0	P00-P07	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.
Port 1	P10-P17	Input/output port. Input or output is specifiable bit by bit. When used as an input port, the use of on-chip pull-up resistors can be specified by software.
Port 2	P20-P25	Input/output port. Input or output is specifiable bit by bit. The use of on-chip pull-up resistors can be specified by software.
Port 6	P60-P67	Input-only port.

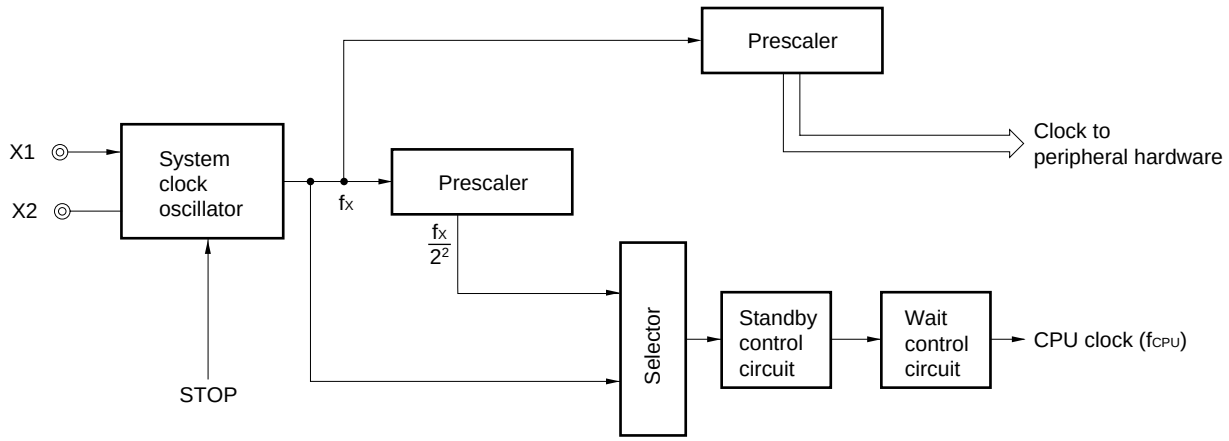
5.2 Clock Generator

The μPD789841 and μPD789842 have an on-chip system clock generator.

It is possible to change the minimum instruction execution time.

- 0.24 μs/0.96 μs (when the system clock operates at 8.38 MHz)

Figure 5-1. Block Diagram of Clock Generator



5.3 Timer

The μPD789841 and μPD789842 have six on-chip timers.

- 10-bit inverter control timer (TM7) : 1 channel
- 8-bit timer/event counters (TM80, TM81) : 2 channels
- 8-bit timer counter (TM82) : 1 channel
- Watch timer (WT) : 1 channel
- Watchdog timer (WDT) : 1 channel

Table 5-2. Timer Operation

		TM7	TM80	TM81	TM82	WT[Note 1]	WDT[Note 2]
Operation mode	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	-	1 channel	1 channel	-	-	-
Function	Timer output	1 output	-	-	1 output	-	-
	Square wave output	-	-	-	1 output	-	-
	Interrupt source	1	1	1	1	2	2

Notes 1. Watch timer can perform both watch timer and interval timer functions at the same time.

2. Since the watchdog timer provides the watchdog timer function and interval timer function, select the one out of two functions.

Figure 5-2. Block Diagram of 10-Bit Inverter Control Timer

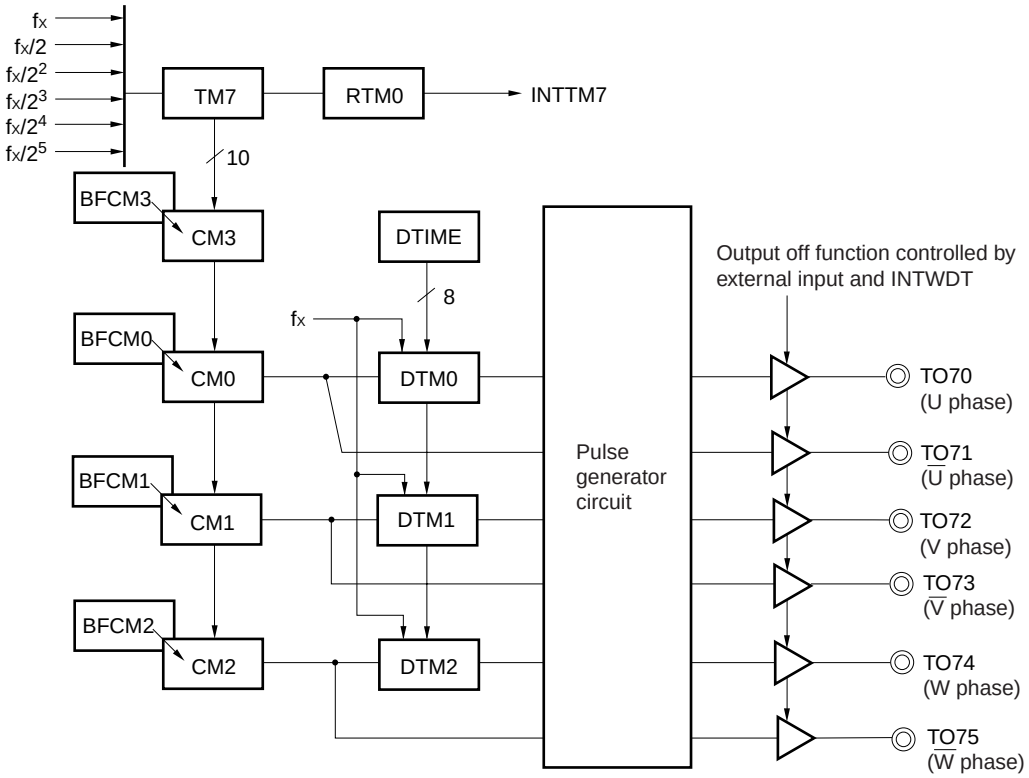


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 80

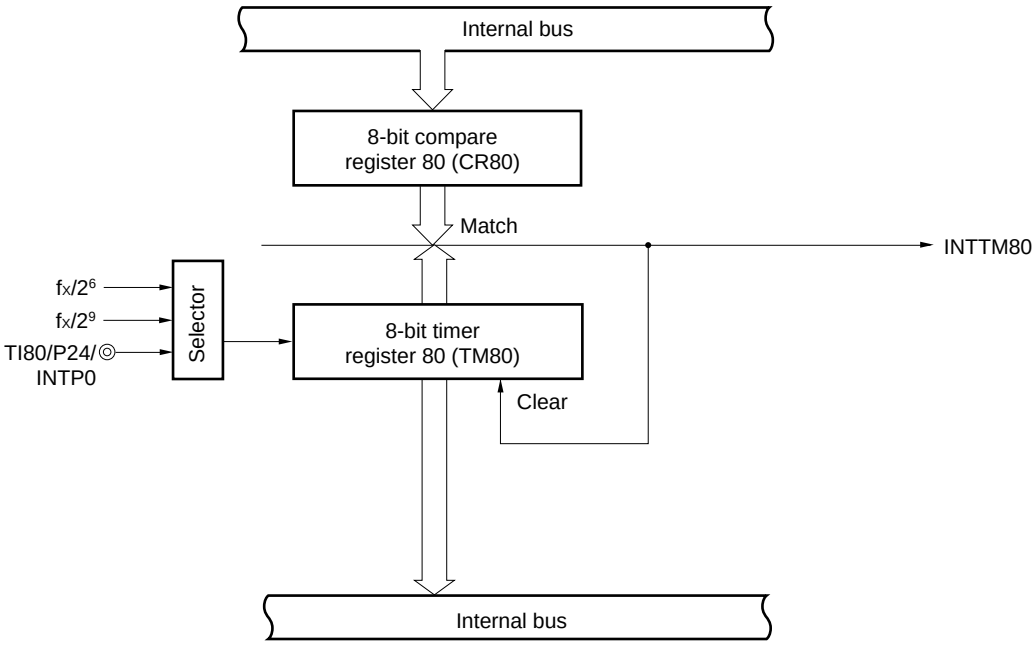


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 81

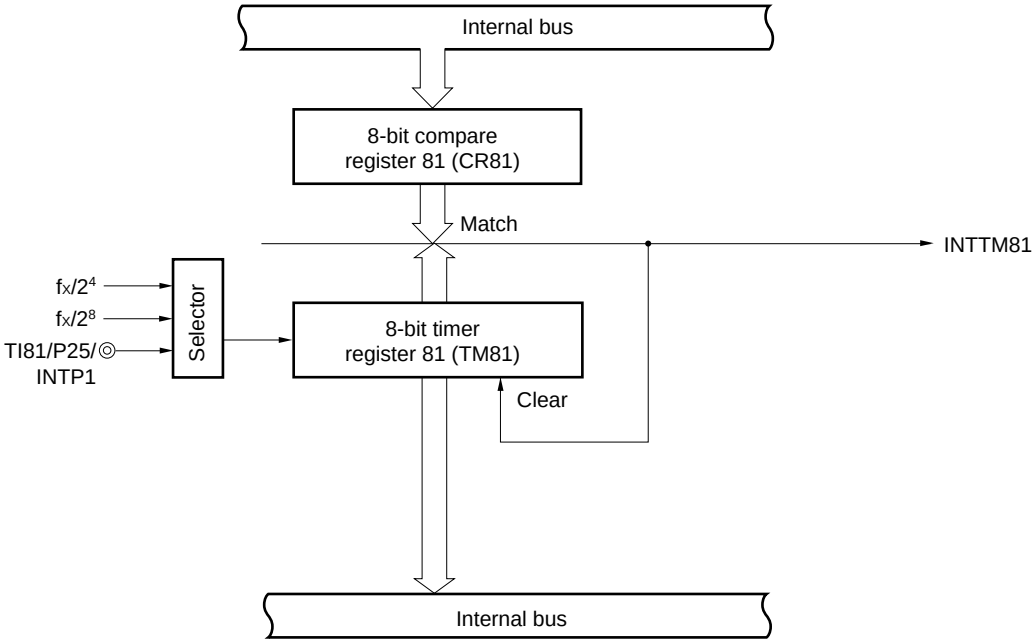


Figure 5-5. Block Diagram of 8-Bit Timer Counter 82

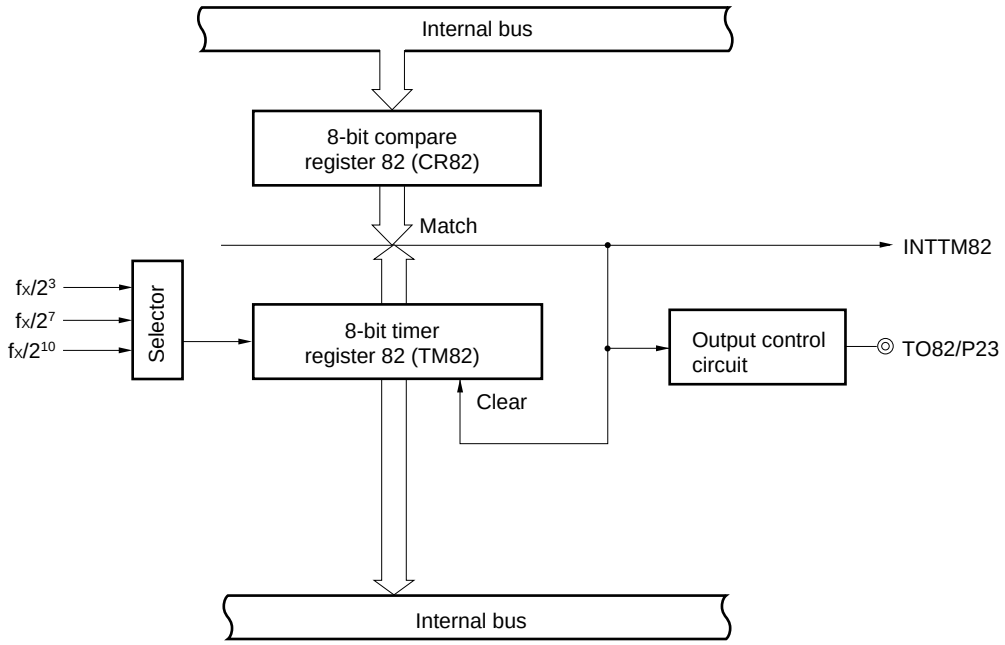


Figure 5-6. Block Diagram of Watch Timer

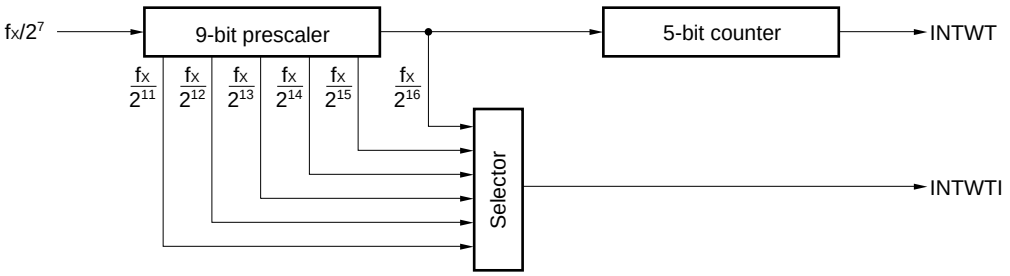
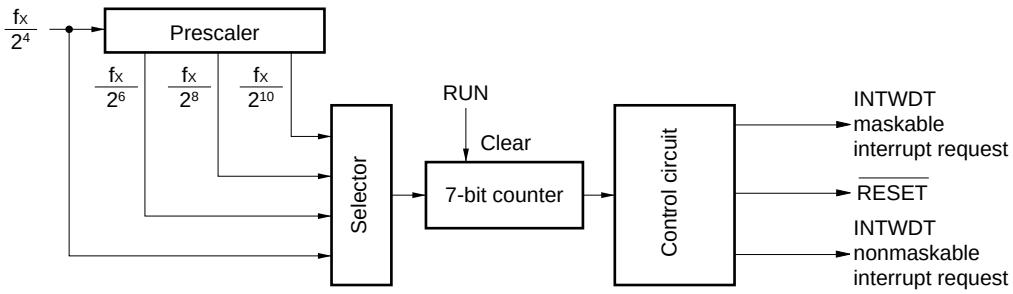


Figure 5-7. Block Diagram of Watchdog Timer

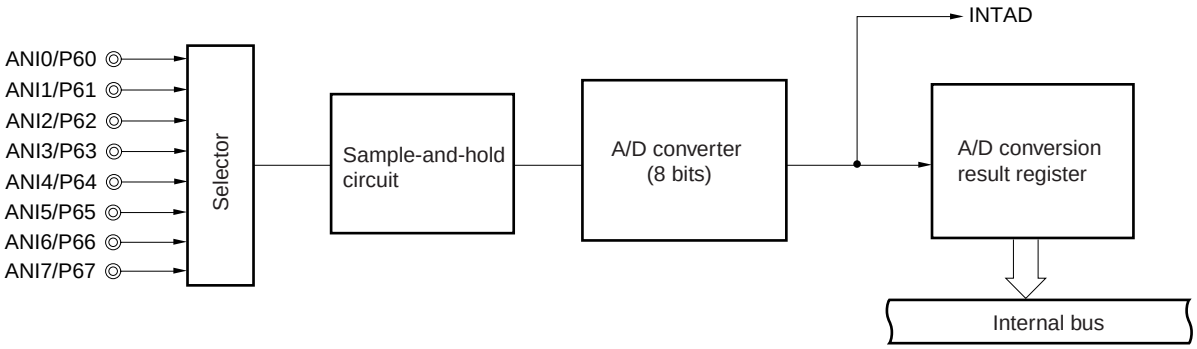


5.4 A/D Converter

The μPD789841 and μPD789842 have an on-chip 8-channel A/D converter with an 8-bit resolution.

A/D conversion can be started only by software.

Figure 5-8. Block Diagram of A/D Converter



5.5 Serial Interface

One channel of serial interface is on chip.

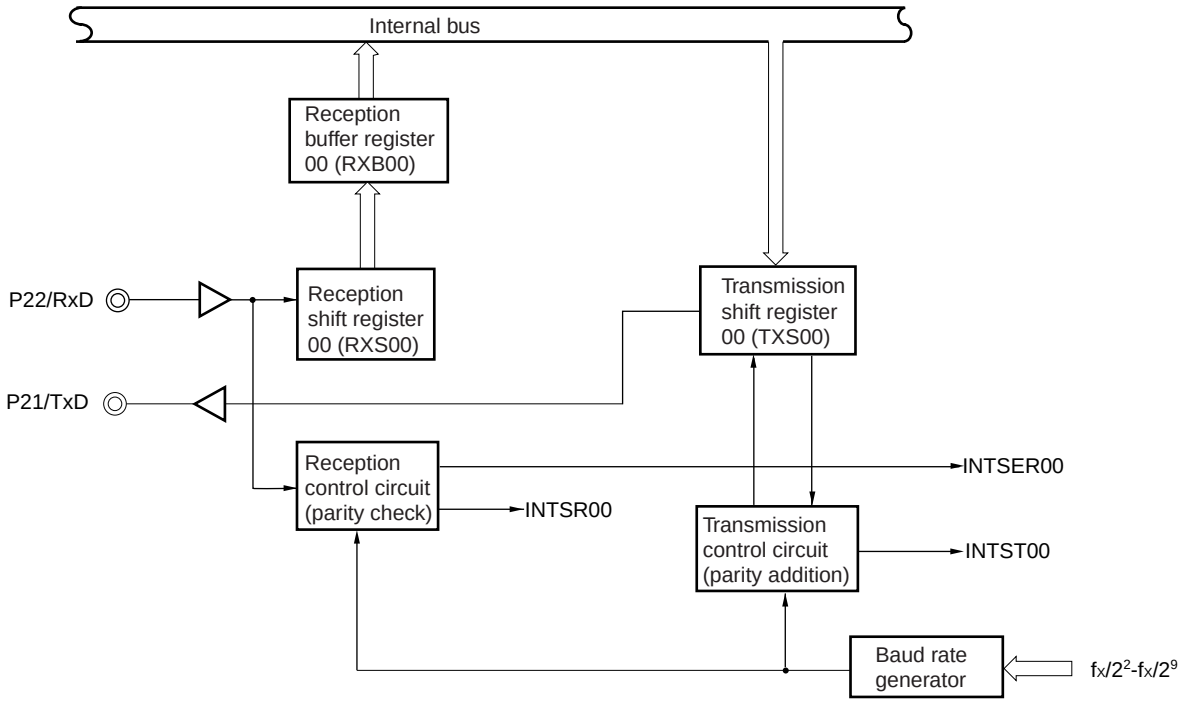
- Serial interface UART00

  This mode is used to send and receive the one byte of data that follows a start bit. It supports full-duplex communication.

  Serial interface UART00 contains a UART-dedicated baud rate generator, enabling communication over a wide range of baud rates.

  The UART-dedicated baud rate generator can output the 31.25-kbps baud rate that complies with the MIDI standard.

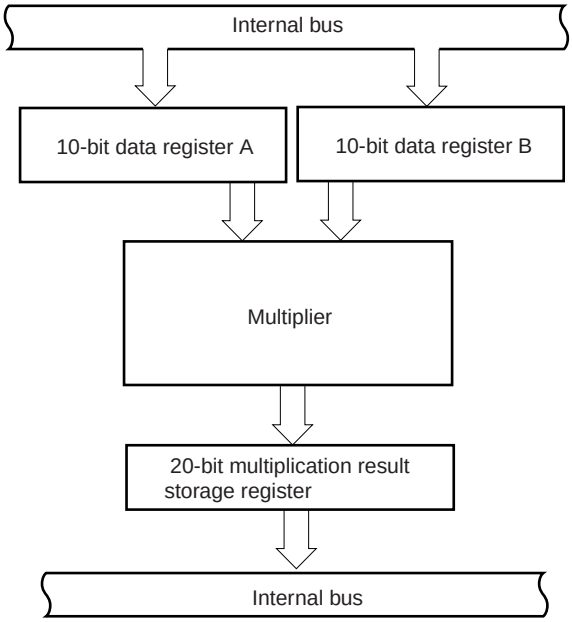
Figure 5-9. Block Diagram of Serial Interface UART00



5.6 Multiplier

The multiplier can execute calculation of 10 bits × 10 bits = 20 bits.

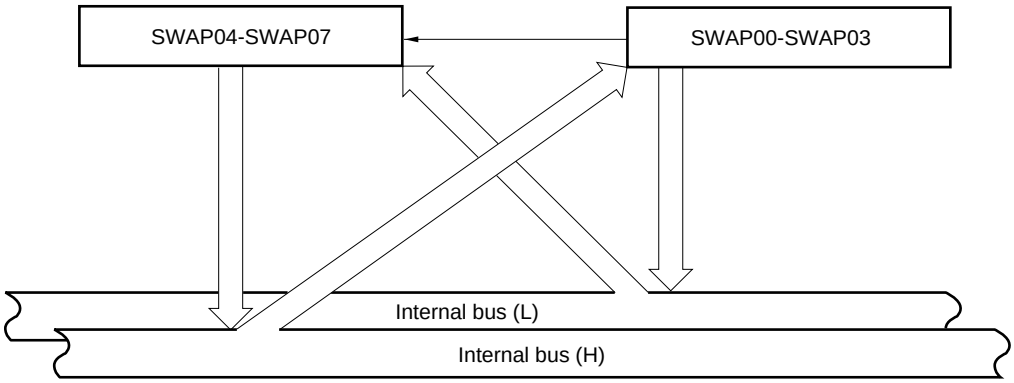
Figure 5-10. Block Diagram of Multiplier



5.7 Swapping (SWAP)

By performing four shift operations, it is possible to switch the contents of the high-order four bits of swapping function register 0 (SWAP0) with the low-order four bits. Figure 5-11 shows the block diagram of SWAP.

Figure 5-11. Block Diagram of SWAP



6. INTERRUPT FUNCTION

There are two types and 14 sources of interrupt function as shown below.

- Nonmaskable interrupt: 1 source
- Maskable interrupts : 13 sources

Table 6-1. Interrupt Source List

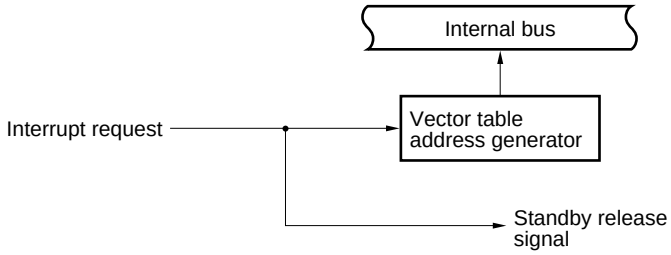
Type of interrupt	Priority[Note 1]	Interrupt source		Internal/ external	Vector table address	Basic configuration type[Note 2]
		Name	Trigger			
Nonmaskable	-	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTTM7	Generation of underflow signal for 10-bit inverter control timer	Internal	000AH	(B)
	4	INTSER00	Reception error on serial interface (UART00)		000CH	
	5	INTSR00	Completion of reception on serial interface (UART00)		000EH	
	6	INTST00	Completion of transmission on serial interface (UART00)		0010H	
	7	INTWT	Watch timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM80	Generation of match signal for 8-bit timer/event counter 80		0016H	
	10	INTTM81	Generation of match signal for 8-bit timer/event counter 81		0018H	
	11	INTTM82	Generation of match signal for 8-bit timer counter 82		001AH	
	12	INTAD	A/D conversion completion signal		001CH	

Notes 1. The priority is the order of priority when multiple maskable interrupts are generated simultaneously. 0 is the highest priority and 12 is the lowest priority.

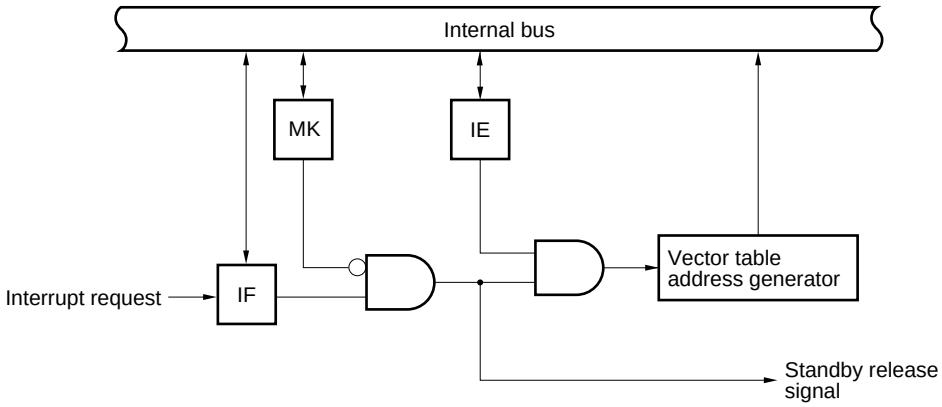
2. Types (A) to (C) in the basic configuration correspond to (A) to (C) in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Function

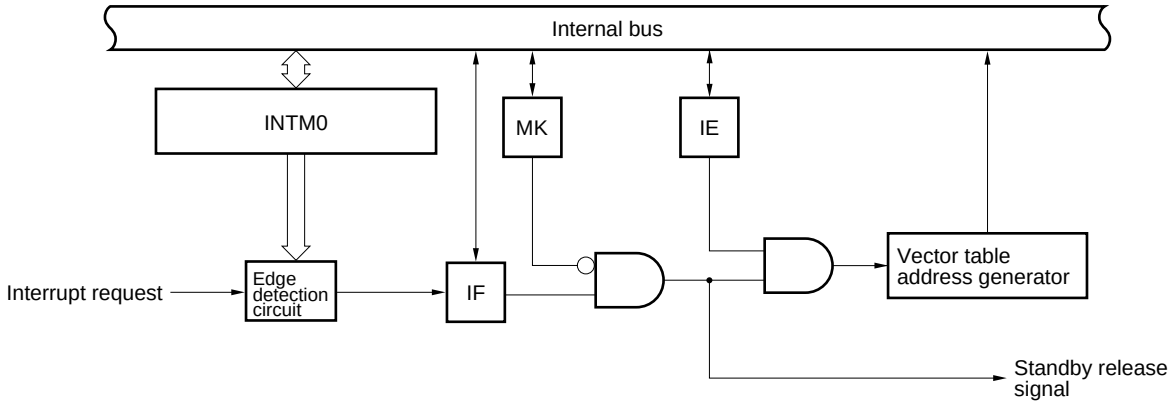
(A) Internal nonmaskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



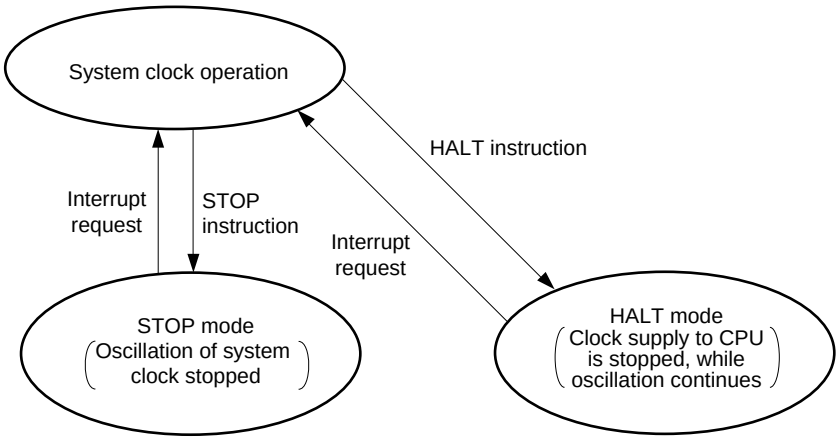
INTM0 : External interrupt mode register 0
IF : Interrupt request flag
IE : Interrupt enable flag
MK : Interrupt mask flag

7. STANDBY FUNCTION

The standby function is a function to reduce current consumption and there are two kinds of standby function as shown below.

- HALT mode : Stops the operating clock of the CPU. Intermittent operation together with normal operation can reduce average current consumption.
- STOP mode : Stops oscillation of the system clock. Stops the entire operation by the system clock and minimizes power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The system is reset in the following two ways.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by detection of inadvertent program loop time of watchdog timer

9. INSTRUCTION SET OVERVIEW

The instruction set for the μPD789841 and μPD789842 is listed later.

9.1 Legend

9.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform with the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and a pair of [and] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [and]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or a pair of [and].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 9-1).

Table 9-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

9.1.2 Descriptions of the operation field

A	:	A register (8-bit accumulator)
X	:	X register
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
AX	:	AX register pair (16-bit accumulator)
BC	:	BC register pair
DE	:	DE register pair
HL	:	HL register pair
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
IE	:	Interrupt request enable flag
NMIS	:	Flag to indicate that a nonmaskable interrupt is being handled
()	:	Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L	:	Upper and lower 8 bits of a 16-bit register
∧	:	Logical product (AND)
∨	:	Logical sum (OR)
$\veebar$	:	Exclusive OR
—	:	Inverted data
addr16	:	16-bit immediate data or label
jdisp8	:	Signed 8-bit data (displacement value)

9.1.3 Description of the flag operation field

(blank)	:	No change
0	:	To be cleared to 0
1	:	To be set to 1
×	:	To be set or cleared according to the result
R	:	To be restored to the previous value

9.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.
2. Except when r = A or X.
3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp Note	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1			×
ROL	A, 1	1	2	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, $A_{m-1} \leftarrow A_m$) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, $A_{m+1} \leftarrow A_m$) × 1			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP − 1) ← (PC + 3)$_H$, (SP − 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP − 2			
CALLT	[addr5]	1	8	(SP − 1) ← (PC + 1)$_H$, (SP − 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP − 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP − 1) ← PSW, SP ← SP − 1			
	rp	1	4	(SP − 1) ← rp$_H$, (SP − 2) ← rp$_L$, SP ← SP − 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock control register (PCC).

10. ELECTRICAL CHARACTERISTICS

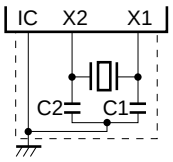
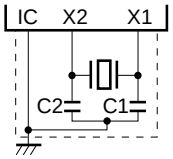
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Rated value	Unit
Supply voltage	V_{DD}		-0.3 to +6.5	V
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V
Output high current	I_{OH}	Each pin	-10	mA
		Total for all pins	-30	mA
Output low current	I_{OL}	Each pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

CHARACTERISTICS OF THE SYSTEM CLOCK OSCILLATION CIRCUIT
(T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	8.0	8.38	8.5	MHz
		Oscillation settling time[Note 2]	After V_{DD} reaches MIN. of the oscillation voltage range			4	ms
Crystal		Oscillator frequency (f_X)[Note 1]		8.0	8.38	8.5	MHz
		Oscillation settling time[Note 2]				10	ms

Notes 1. Only the characteristics of the oscillation circuit are indicated. See the description of the AC characteristics for the instruction execution time.

2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected. Use a resonator that can settle oscillation before the oscillation settling time expires.

Caution When using the system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

DC CHARACTERISTICS (T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output high current	I_{OH}	Each pin				-1	mA
		Total for all pins				-15	mA
Output low current	I_{OL}	Each pin				10	mA
		Total for all pins				80	mA
Input high voltage	V_{IH1}	P00-P07, P10-P17, P60-P67		0.7V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20-P25		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input low voltage	V_{IL1}	P00-P07, P10-P17, P60-P67		0		0.3V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P20-P25		0		0.2V_{DD}	V
	V_{IL3}	X1, X2		0		0.1	V
Output high voltage	V_{OH}	I_{OH} = -1 mA		V_{DD} – 1.0			V
Output low voltage	V_{OL}	I_{OL} = 10 mA				1.0	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1 and X2			3	μA
	I_{LIH2}		X1, X2			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Pins other than X1 and X2			-3	μA
	I_{LIL2}		X1, X2			-20	μA
High-level output leakage current	I_{LOH}	V_{OUT} = 0 V				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				-3	μA
Software pull-up resistor	R	V_{IN} = 0 V		50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	8.38-MHz crystal oscillation (operating mode)[Note 2]			5.5	16.5	mA
	I_{DD2}	8.38-MHz crystal oscillation (HALT mode)			1.2	3.6	mA
	I_{DD3}	STOP mode			0.1	30	μA
	I_{DD4}	8.38-MHz crystal oscillation (A/D operation mode)			6.0	18.0	mA

Notes 1. The power supply current does not include the current flowing through the on-chip pull-up resistor.

2. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H)

Remark The characteristics of a dual-function pin do not differ between the port function and the secondary function, unless otherwise stated.

AC CHARACTERISTICS

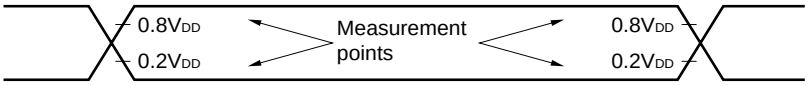
(1) Basic operations (T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	When PCC = 00H	0.24		0.25	μs
		When PCC = 02H	0.94		1.0	μs
TI input frequency	f_{TI}		0		4.0	MHz
TI input high/low level width	t_{TIH}, t_{TIL}		0.1			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INTP0, INTP1	10			μs
$\overline{\text{RESET}}$ input low level width	t_{RSL}		10			μs

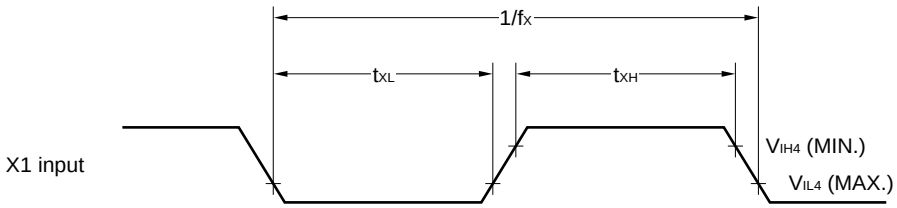
(2) Serial interface (UART) (T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		When the microcontroller operates at the system clock (f_X) of 8.38 MHz			115,200	bps

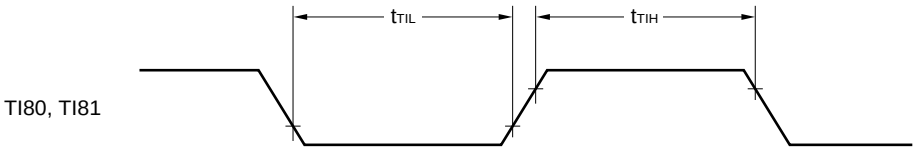
AC TIMING MEASUREMENT POINTS (except the X1 input)



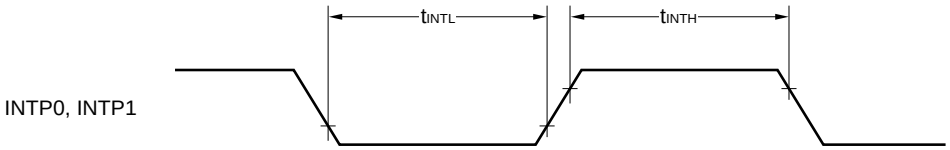
CLOCK TIMING



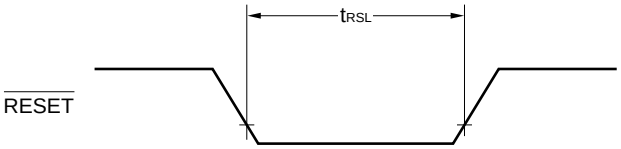
TI TIMING



INTERRUPT INPUT TIMING



$\overline{\text{RESET}}$ INPUT TIMING



A/D CONVERTER CHARACTERISTICS (T_A = -40°C to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]					1.5	LSB
Conversion time	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Note Quantization error (±1/2LSB) is excluded.

DATA HOLD CHARACTERISTICS OF DATA MEMORY AT LOW VOLTAGE IN STOP MODE (T_A = -40°C to +85°C)

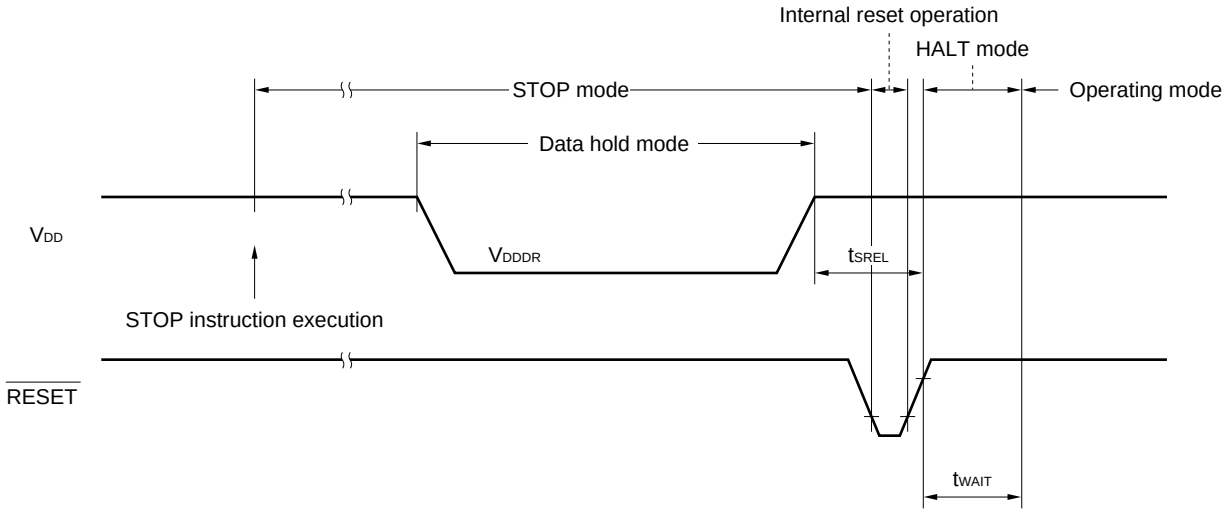
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V_{DDDR}		4.0		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation settling time[Note 1]	t_{WAIT}	Reset by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Reset by interrupt request		**Note 2**		ms

Notes 1. During the oscillation settling time, CPU operations are disabled to prevent them from becoming unstable upon the start of oscillation.

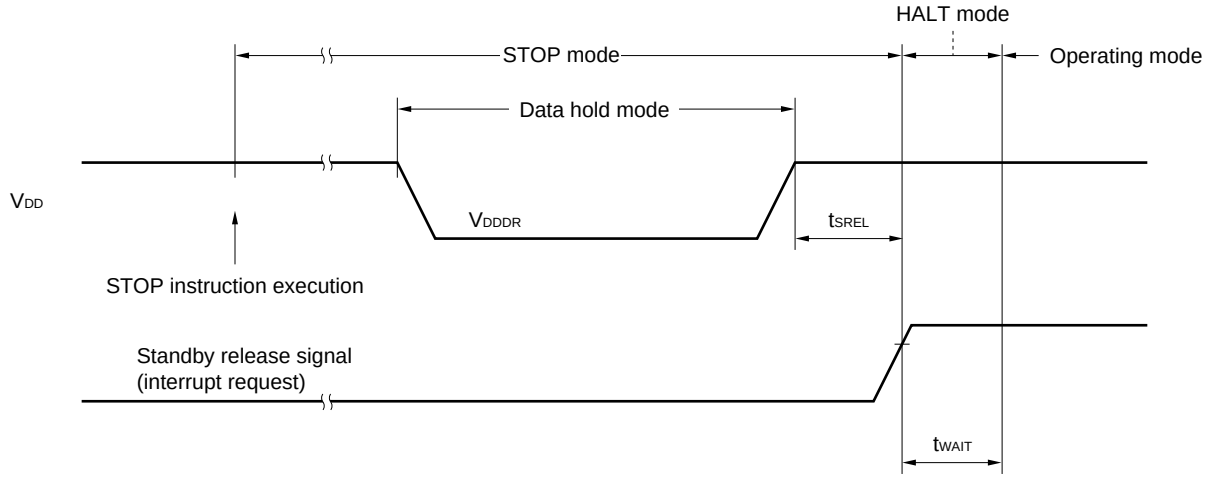
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register.

Remark f_X: System clock oscillation frequency

DATA HOLD TIMING (STOP mode release by $\overline{\text{RESET}}$)

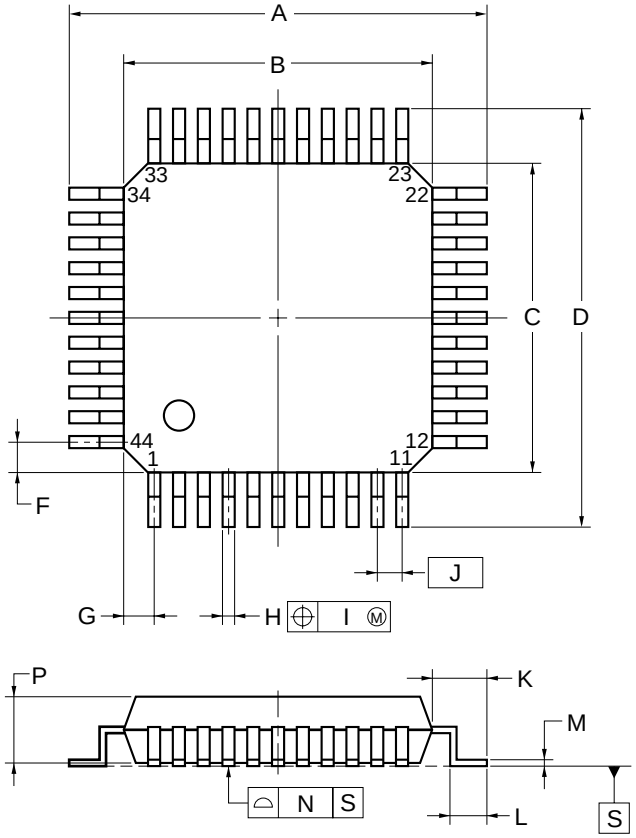


DATA HOLD TIMING (standby release signal: STOP mode release by interrupt signal)

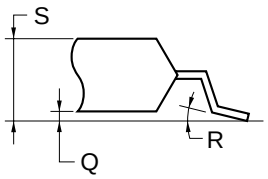


11. PACKAGE DRAWING

44 PIN PLASTIC QFP (□10)



detail of lead end



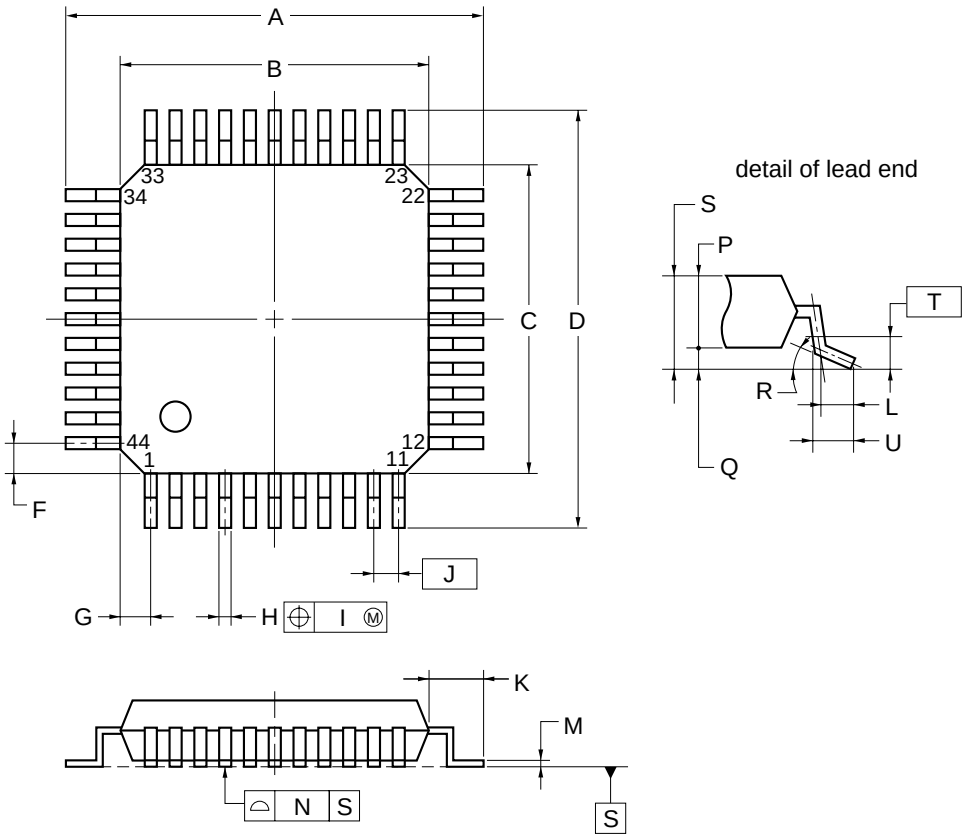
NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS-1

44 PIN PLASTIC QFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD789841 and μPD789842.

LANGUAGE PROCESSING SOFTWARE

RA78K0S[Notes 1, 2, 3]	Assembler package common to the 78K/0S series
CC78K0S[Notes 1, 2, 3]	C compiler package common to the 78K/0S series
DF789842[Notes 1, 2, 3, 5]	Device file for the μPD789842 subseries

FLASH MEMORY WRITE TOOLS

Flashpro III (Model number: FL-PR3[Note 4], PG-FP3)	Flash writer dedicated to the microcontrollers incorporating a flash memory.
FA-44GB[Note 4]	This is a flash memory writing adapter for a 44-pin plastic QFP. The FA-44GB must be connected to the target product properly.
Flashpro III controller	The Flashpro III controller program comes with Flashpro III and is controlled on the personal computer. This program runs under operating systems such as Windows™ 95.

DEBUGGING TOOLS

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging hardware and software of application system using 78K/0S series. Supports integrated debugger (ID78K0S-NS). Used in combination with AC adapter, emulation probe, and interface adapter for connecting the host machine.
IE-70000-MC-PS-B AC adapter	This is the adapter for supplying power from outlet of 100 to 240 VAC.
IE-70000-98-IF-C Interface adapter	This adapter is needed when PC-9800 series (excluding notebook models) is used as a host machine of IE-78K0S-NS. (Compatible with C bus)
IE-70000-CD-IF-A[Note 5] PC card interface	This PC card and interface cable are needed when a notebook-type personal computer is used as a host machine of IE-78K0S-NS. (Compatible with a PCMCIA socket)
IE-70000-PC-IF-C Interface adapter	This adapter is needed when IBM PC/AT™ and compatibles are used as a host machine of IE-78K0S-NS. (Compatible with ISA bus)
IE-70000-PCI-IF[Note 5] Interface adapter	This adapter is needed when a personal computer with a built-in PCI bus is used as a host machine of IE-78K0S-NS.
IE-789842-NS-EM1 Emulation board	Emulation board for emulating the peripheral hardware inherent to the device. Used in combination with in-circuit emulator.
NP-44GB[Note 4]	Board for connecting the in-circuit emulator and target system. This is for 44-pin plastic QFP.
SM78K0S[Notes 1, 2]	System simulator common to the 78K/0S series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to the 78K/0S series
DF789842[Notes 1, 2, 5]	Device file for the μPD789842 subseries

REAL-TIME OS

MX78K0S[Notes 1, 2]	OS for the 78K/0S series

Notes 1. Based on the PC-9800 series (MS-DOS™ + Windows)

2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)

4. Product manufactured by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813). Contact an NEC sales representative for purchase.

5. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789842.

APPENDIX B RELATED DOCUMENTS

DOCUMENTS RELATED TO DEVICES

Document name	Document No.	
	Japanese	English
μPD789841, 789842 Preliminary Product Information	U13790J	This manual
μPD78F9842 Preliminary Product Information	To be prepared	To be prepared
μPD789842 Subseries User's Manual	U13776J	To be prepared
78K/0 Series User's Manual - Instruction	U11047J	U11047E

DOCUMENTS RELATED TO DEVELOPMENT TOOLS (USER'S MANUAL)

Document name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows Base	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger Windows Base	Reference	U12901J	U12901E
IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789842-NS-EM1 Emulation Board		To be prepared	To be prepared

DOCUMENTS RELATED TO SOFTWARE TO BE INCORPORATED INTO THE PRODUCT (USER'S MANUAL)

Document name		Document No.	
		Japanese	English
OS for 78K/0S Series MX78K0S	Basic	U12938J	U12938E

OTHER DOCUMENTS

Document name	Document No.	
	Japanese	English
IC PACKAGE MANUAL	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality Control/Reliability Handbook	C12769J	-
Guide for Products Related to Micro-Computer: Other Companies	U11416J	-

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

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[MEMO]

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