NEC

MOS INTEGRATED CIRCUIT

μPD789830

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD789830 is an ASSP microcontroller in the 78K/0S series and is intended for use in card readers.

A bare chip version of the μPD789830 is also available. This microcontroller has an internal dot LCD driver (40 segment × 16 common) and is ideal for products that have an LCD display such as card readers.

A flash memory model, μPD78F9831, that operates on the same voltage as the mask ROM model, and various development tools are under development.

The functions of the μPD789830 are explained in detail in the following User's Manuals. Be sure to read these manuals when designing your system.

μPD789830 Subseries User's Manual: U13679E
78K/0S Series User's Manual - Instruction: U11047E

FEATURES

- Bare chip
- ROM and RAM capacities
  - Internal ROM : 24K bytes
  - Internal high-speed RAM : 1K byte
  - RAM for LCD display : 80 bytes
- ★ Minimum instruction execution time variable from high speed (0.4 μs: with 5.0-MHz main system clock) to low speed (122 μs: with 32.768-kHz subsystem clock)
- I/O port: 30 pins
- Serial interface (UART00): 1 channel
- LCD controller/driver
  - Segment signal output: 40 pins MAX.
  - Common signal output: 16 pins MAX.
  - 1/5 bias mode
- Timer: 4 channels
  - 16-bit timer : 1 channel
  - 8-bit timer : 1 channel
  - Watch timer : 1 channel
  - Watchdog timer : 1 channel
- Pulse output : Clock output/buzzer output
- Key return signal detector circuit
- Supply voltage: V_{DD} = 2.7 to 5.5 V

Document No. U13284EJ1V0DSJ1 (1st edition)
Date Published October 2000 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

APPLICATIONS

Card readers

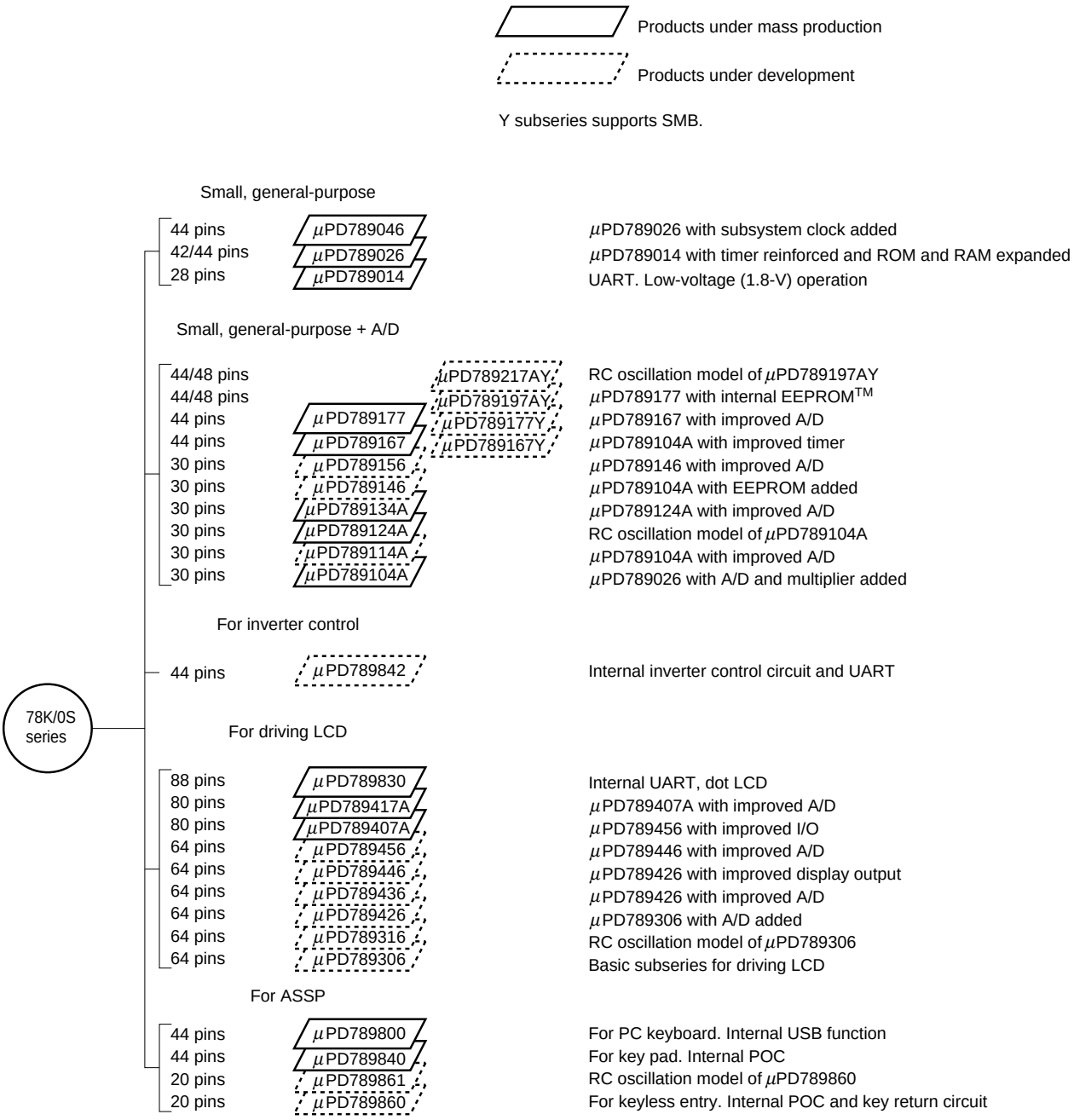
ORDERING INFORMATION

Part Number	Package
μPD789830P-×××	88-pin bare chip

Remark ××× indicates ROM code suffix.

★ **Development of 78K/0S series**

The following models are available in the 78K/0S series. The outlined part numbers indicate the name of a subseries.



The major differences between subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
			8-bit	16-bit	Watch	WDT						
Small, general-purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART:1 ch)	34 pins	1.8 V	–
	μPD789026	4 K-16 K			–							
	μPD789014	2 K-4 K	2 ch	–						22 pins		
Small, general-purpose + A/D	μPD789177	16 K-24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31 pins	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K-16 K	1 ch		–		–	4 ch		20 pins		Internal EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K-8 K						4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
For inverter control	μPD789842	8 K-16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30 pins	4.0 V	–
For LCD driving	μPD789830	24 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	30 pins	2.7 V	–
	μPD789417A	12 K-24 K	3 ch					7 ch		43 pins	1.8 V	
	μPD789407A						7 ch	–				
	μPD789456	12 K-16 K	2 ch				–	6 ch	1 ch (UART: 1 ch)	30 pins		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40 pins		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16K					–		2 ch (UART: 1 ch)	23 pins		RC oscillation version
	μPD789306											–
ASSP	μPD789800	8 K	2 ch	1 ch	–	1 ch	–	–	2 ch (USB: 1 ch)	31 pins	4.0 V	–
	μPD789840						4 ch		1 ch	29 pins	2.8 V	
	μPD789861	4 K		–			–		–	14 pins	1.8 V	RC oscillation version
	μPD789860											–

Note 10-bit timer: 1 channel

FUNCTIONAL OUTLINE

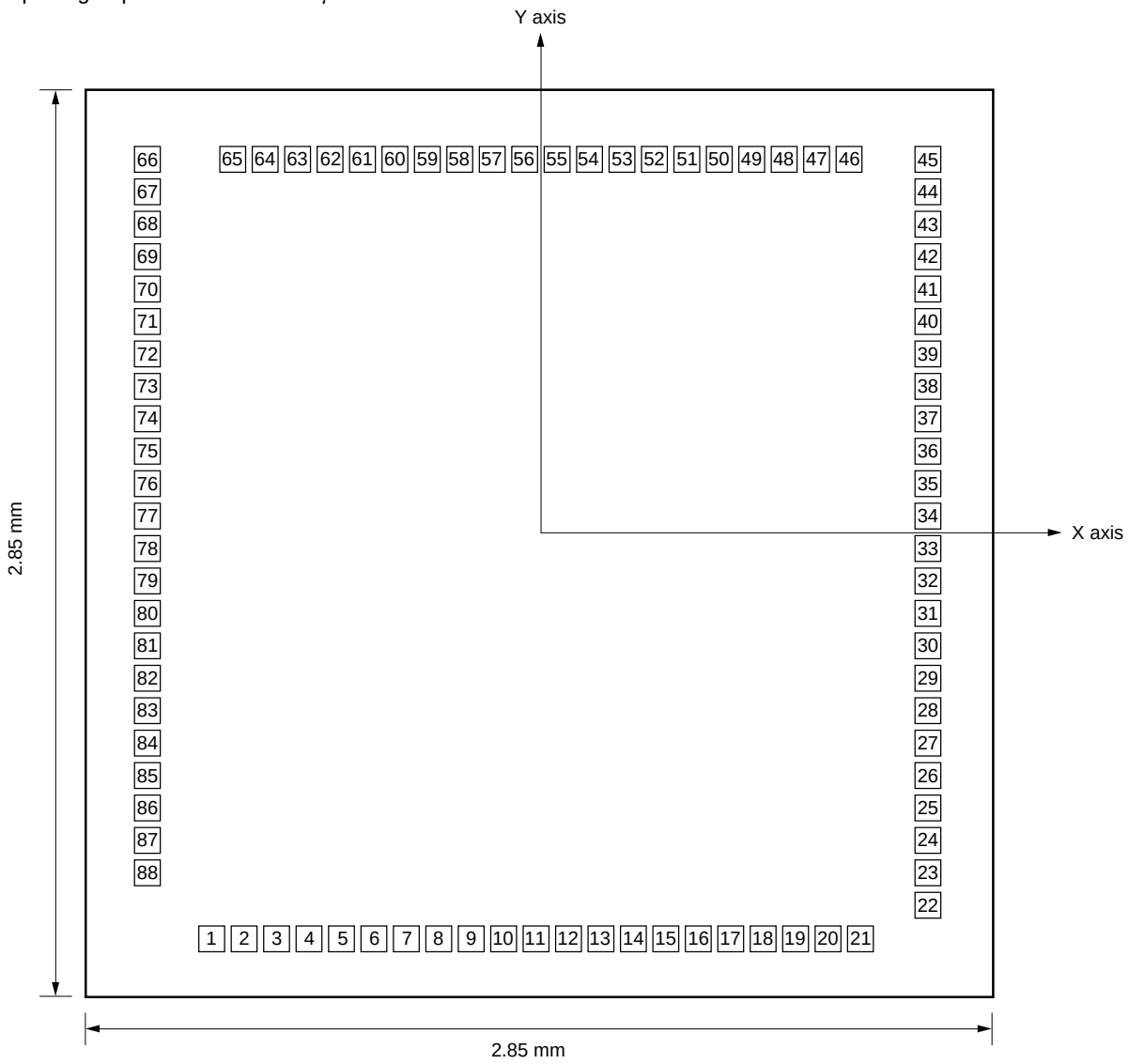
Item		Function
Internal memory	ROM	24 K bytes
	High-speed RAM	1 K bytes
	RAM for LCD display	80 bytes
★ Minimum instruction execution time		• 0.4 μs/1.6 μs (main system clock: 5 MHz) • 122 μs (subsystem clock: 32.768 kHz)
General-purpose register		8 bits × 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.
I/O port		Total : 30 pins • CMOS I/O : 29 pins • N-ch open drain : 1 pin
Serial interface		UART mode: 1 channel
LCD controller/driver		• Segment signal output : 40 pins max. • Common signal output : 16 pins • 1/5 bias mode
Timers		• 16-bit timer : 1 channel • 8-bit timer : 1 channel • Watch timer : 1 channel • Watchdog timer : 1 channel
Pulse output		Clock output/buzzer output
Vectored interrupt source	Maskable	Internal: 10, external: 4
	Non-maskable	Internal: 1
Supply voltage		V_{DD} = 2.7 to 5.5 V
Operating temperature		T_A = −20 to +60 °C
Package		88-pin bare chip

CONTENTS

1. PIN CONFIGURATION (Top View)

- 88-pin bare chip
  μPD789830P-×××

  Minimum pad interval : 110.04 μm
  Opening of pad : 80.04 μm



Pad coordinates (unit: μm: pad center coordinates) (1/2)

No.	Pin Name	X Axis	Y Axis
1	COM14	–1085.40	–1303.90
2	COM15	–975.40	–1303.90
3	S0	–865.30	–1303.90
4	S1	–755.30	–1303.90
5	S2	–645.20	–1303.90
6	S3	–535.20	–1303.90
7	S4	–425.20	–1303.90

No.	Pin Name	X Axis	Y Axis
8	S5	–315.10	–1303.90
9	S6	–205.10	–1303.90
10	S7	–95.00	–1303.90
11	S8	15.00	–1303.90
12	S9	125.00	–1303.90
13	S10	235.10	–1303.90
14	S11	345.10	–1303.90

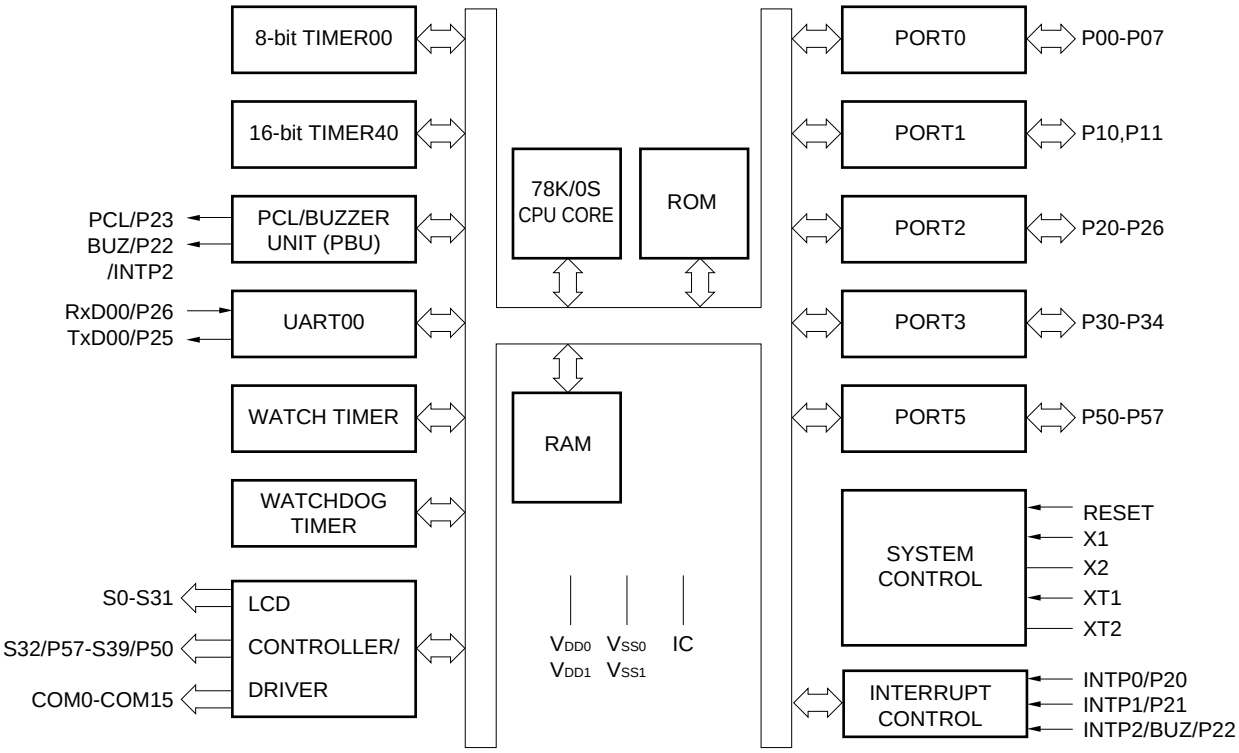
Pad coordinates (unit: μm: pad center coordinates) (2/2)

No.	Pin Name	X Axis	Y Axis
15	S12	455.20	–1303.90
16	S13	565.20	–1303.90
17	S14	675.20	–1303.90
18	S15	785.30	–1303.90
19	S16	895.30	–1303.90
20	S17	1005.40	–1303.90
21	S18	1115.40	–1303.90
22	S19	1303.90	–1227.00
23	S20	1303.90	–1117.00
24	S21	1303.90	–1006.90
25	S22	1303.90	–896.90
26	S23	1303.90	–786.80
27	S24	1303.90	–676.80
28	S25	1303.90	–566.80
29	S26	1303.90	–456.70
30	S27	1303.90	–346.70
31	S28	1303.90	–236.60
32	S29	1303.90	–126.60
33	S30	1303.90	–16.60
34	S31	1303.90	93.50
35	P57/S32	1303.90	203.50
36	P56/S33	1303.90	313.60
37	P55/S34	1303.90	423.60
38	P54/S35	1303.90	533.60
39	P53/S36	1303.90	643.70
40	P52/S37	1303.90	753.70
41	P51/S38	1303.90	863.80
42	P50/S39	1303.90	973.80
43	P11	1303.90	1083.80
44	P10	1303.90	1193.90
45	V_{DD1}	1294.30	1303.90
46	V_{SS1}	1039.80	1303.90
47	P34	929.80	1303.90
48	P33	819.70	1303.90
49	P32	709.70	1303.90
50	P31	599.60	1303.90
51	P30	489.60	1303.90

No.	Pin Name	X Axis	Y Axis
52	P07	379.60	1303.90
53	P06	269.50	1303.90
54	P05	159.50	1303.90
55	P04	49.40	1303.90
56	P03	–60.60	1303.90
57	P02	–170.60	1303.90
58	P01	–280.70	1303.90
59	P00	–390.70	1303.90
60	IC	–500.80	1303.90
61	$\overline{\text{RESET}}$	–610.80	1303.90
62	X2	–720.80	1303.90
63	X1	–830.90	1303.90
64	V_{SS0}	–940.90	1303.90
65	V_{DD0}	–1051.00	1303.90
66	XT2	–1303.90	1303.90
67	XT1	–1303.90	1193.90
68	P26/RxD00	–1303.90	1083.80
69	P25/TxD00	–1303.90	973.80
70	P24	–1303.90	863.80
71	P23/PCL	–1303.90	687.90
72	P22/INTP2/BUZ	–1303.90	577.90
73	P21/INTP1	–1303.90	467.80
74	P20/INTP0	–1303.90	357.80
75	COM0	–1303.90	247.70
76	COM1	–1303.90	137.70
77	COM2	–1303.90	27.70
78	COM3	–1303.90	–82.40
79	COM4	–1303.90	–192.40
80	COM5	–1303.90	–302.50
81	COM6	–1303.90	–412.50
82	COM7	–1303.90	–522.50
83	COM8	–1303.90	–632.60
84	COM9	–1303.90	–742.60
85	COM10	–1303.90	–852.70
86	COM11	–1303.90	–962.70
87	COM12	–1303.90	–1072.70
88	COM13	–1303.90	–1182.80

BUZ	: Buzzer Clock	PCL	: Programming Clock
COM0-COM15	: Common Output	$\overline{\text{RESET}}$	: Reset
IC	: Internally Connected	RxD00	: Receive Data
INTP0-INTP2	: Interrupt from Peripherals	S0-S39	: Segment Output
P00-P07	: Port0	TxD00	: Transmit Data
P10, P11	: Port1	V_{DD0}, V_{DD1}	: Power Supply
P20-P26	: Port2	V_{SS0}, V_{SS1}	: Ground
P30-P34	: Port3	X1, X2	: Crystal (Main system Clock)
P50-P57	: Port5	XT1, XT2	: Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



3. PIN FUNCTION LIST

3.1 Port Pins

Pin Name	I/O	Function	At Reset	Shared with:
P00-P07	I/O	Port 0. 8-bit I/O port. Can be set in input or output mode in 1-bit units. To use this port as an input port, an internal pull-up resistor can be connected in software.	Input	–
P10, P11	I/O	Port 1. 2-bit I/O port. Can be set in input or output mode in 1-bit units. To use this port as an input port, an internal pull-up resistor can be connected in software.	Input	–
P20	I/O	Port 2. 7-bit I/O port. Can be set in input or output mode in 1-bit units. P24 is an N-ch open-drain I/O port pin.	Input	INTP0
P21				INTP1
P22				INTP2/BUZ
P23				PCL
P24				–
P25				TxD00
P26				RxD00
P30-P34	I/O	Port 3. 5-bit I/O port. Can be set in input or output mode in 1-bit units. To use this port as an input port, an internal pull-up resistor can be connected in software.	Input	–
P50-P57	I/O	Port 5. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	S39-S32

3.2 Pins Other Than Port Pins

Pin Name	I/O	Function	At Reset	Shared with:
INTP0	Input	External interrupt input whose valid edge can be specified (rising edge, falling edge, or both rising and falling edges)	Input	P20
INTP1				P21
INTP2				P22/BUZ
RxD00	Input	Serial data input for asynchronous serial interface	Input	P26
TxD00	Output	Serial data output for asynchronous serial interface	Input	P25
BUZ	Output	Buzzer output	Input	P22/INTP2
PCL	Output	Clock output	Input	P23
S0-S31	Output	Segment signal output of LCD controller/driver	Output	–
S32-S39				P57-P50
COM0-COM15	Output	Common signal output of LCD controller/driver	Output	–
X1	Input	Crystal connection for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Crystal connection for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD0}	–	Positive power supply to ports	–	–
V_{DD1}	–	Positive power supply (except ports)	–	–
V_{SS0}	–	Ground for ports	–	–
V_{SS1}	–	Ground (except ports)	–	–
IC	–	Internally connected. Directly connect this pin to V_{SS0} or V_{SS1}.	–	–

3.3 I/O Circuit Type of Each Pin and Recommended Connections of Unused Pins

Table 3-1 shows the I/O circuit type of each pin and recommended connections of unused pins.
For the configuration of the circuit of each type, refer to Figure 3-1.

★ **Table 3-1. I/O Circuit Type of Each Pin and Recommended Connections of Unused Pins**

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00-P07	5-H	I/O	Input : Individually connected to V_{DD0}/V_{DD1} or V_{SS0}/V_{SS1} via resistor. Output : Leave unconnected.
P10, P11			
P20/INTP0	8-H		
P21/INTP1			
P22/INTP2/BUZ			
P23/PCL	5-S		
P24	13-AB		Input : Individually connected to V_{DD0} or V_{DD1} via resistor. Output : Leave unconnected.
P25/TxD00	5-S		Input : Individually connected to V_{DD0}/V_{DD1} or V_{SS0}/V_{SS1} via resistor. Output : Leave unconnected.
P26/RxD00	8-H		
P30-P34	8-C		
P50/S39-P57/S32	17-I		
S0-S31	17-H	Output	Leave unconnected.
COM0-COM15	18-C		
XT1	16	Input	Connected to V_{SS0} or V_{SS1}.
XT2		–	Leave unconnected.
$\overline{\text{RESET}}$	2	Input	–
IC	–	–	Connected to V_{SS0} or V_{SS1}.

Figure 3-1. I/O Circuit Type of Each Pin (1/2)

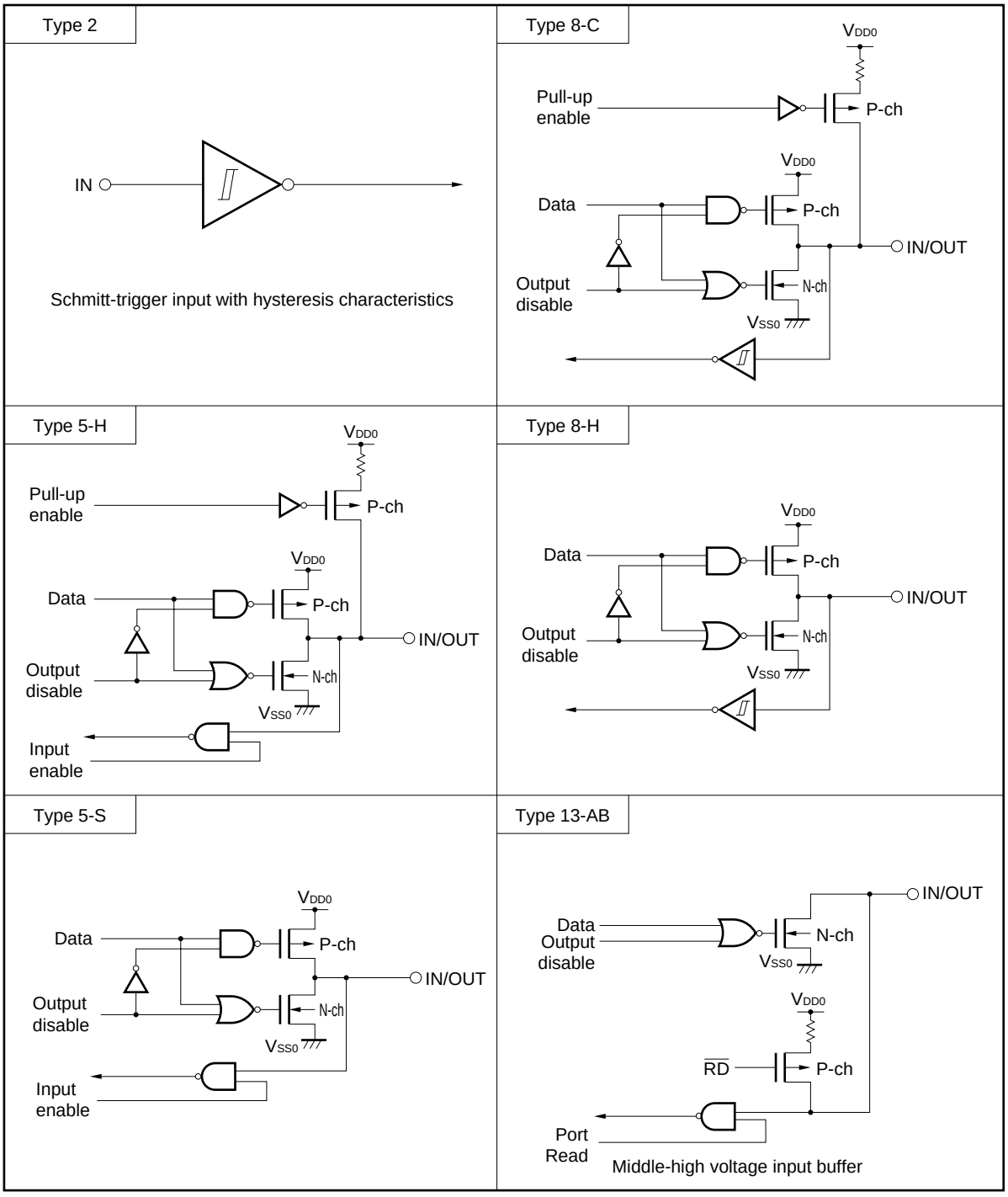
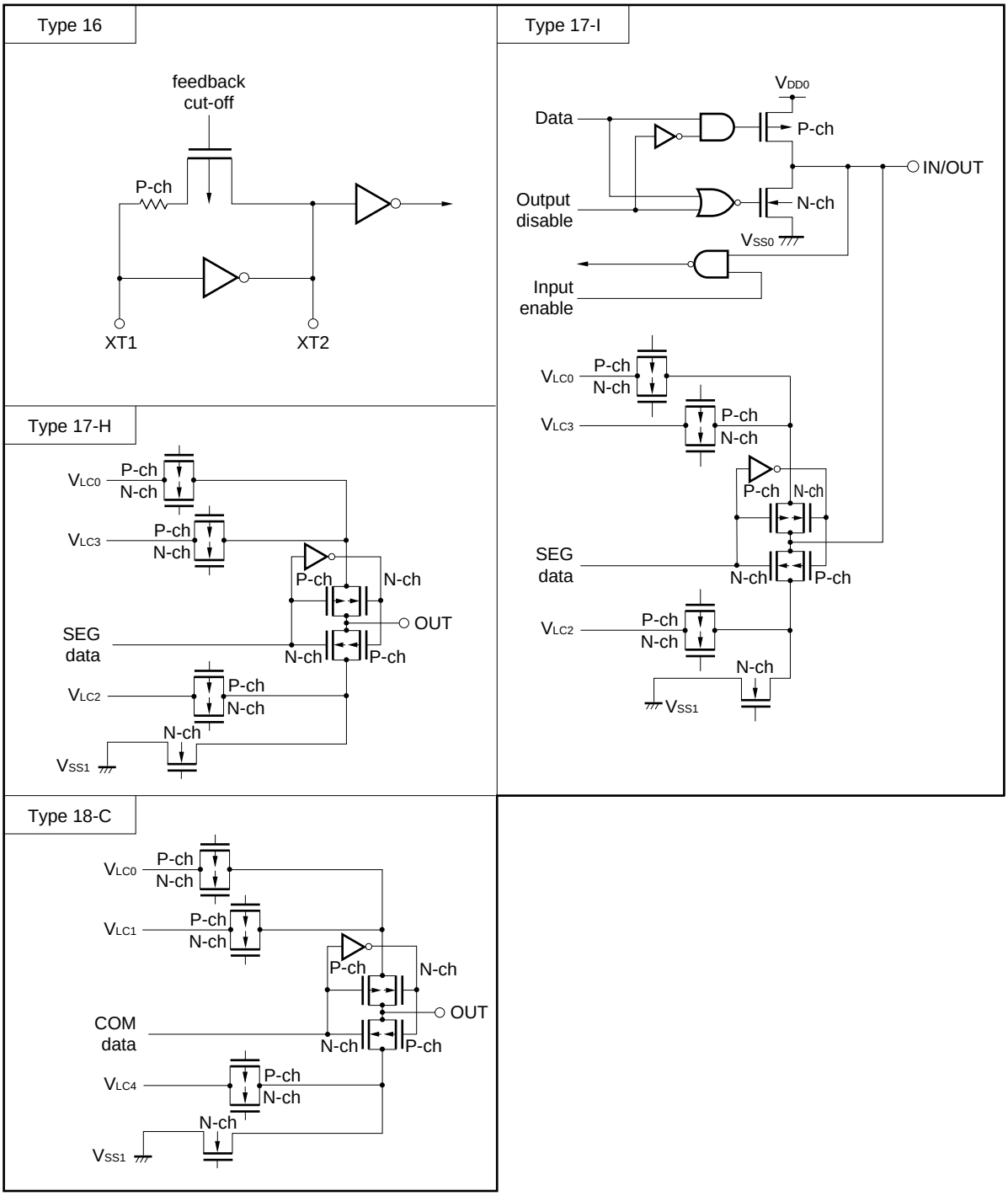


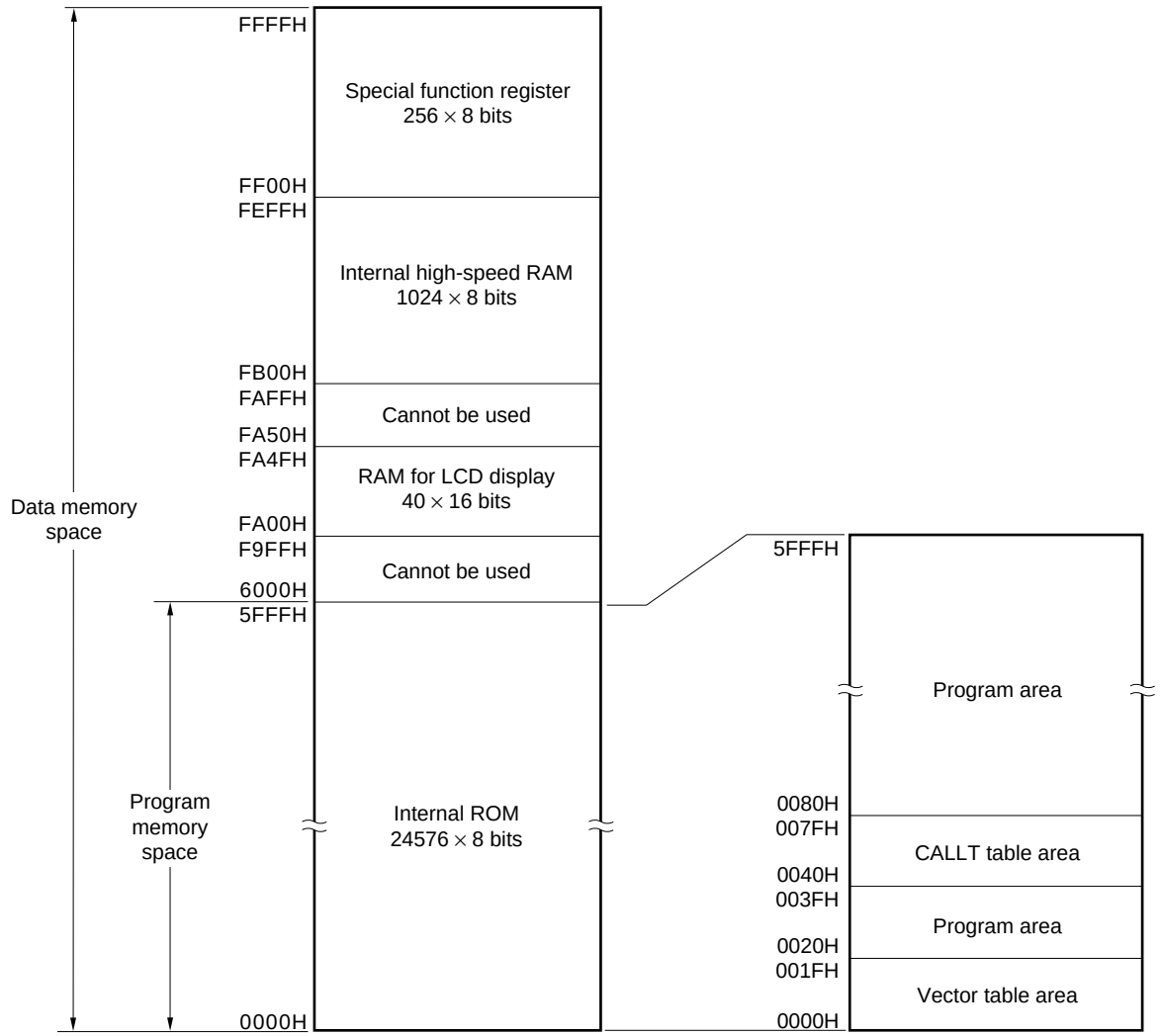
Figure 3-1. I/O Circuit Type of Each Pin (2/2)



4. CPU ARCHITECTURE

The μPD789830 can access a memory space of 64K bytes. Figure 4-1 shows the memory map.

Figure 4-1 Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The μPD789830 has the following two types of I/O ports.

- CMOS I/O : 29 pins
- N-ch open-drain I/O : 1 pin

Total : 30 pins

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00-P07	I/O port. Can be set in input or output mode in 1-bit units. When this port is used as an input port, an internal pull-up resistor can be connected in software.
Port 1	P10, P11	I/O port. Can be set in input or output mode in 1-bit units. When this port is used as an input port, an internal pull-up resistor can be connected in software.
Port 2	P20-P26	I/O port. Can be set in input or output mode in 1-bit units. P24 is an N-ch open-drain I/O port.
Port 3	P30-P34	I/O port. Can be set in input or output mode in 1-bit units. When this port is used as an input port, an internal pull-up resistor can be connected in software.
Port 5	P50-P57	I/O port. Can be set in input or output mode in 1-bit units.

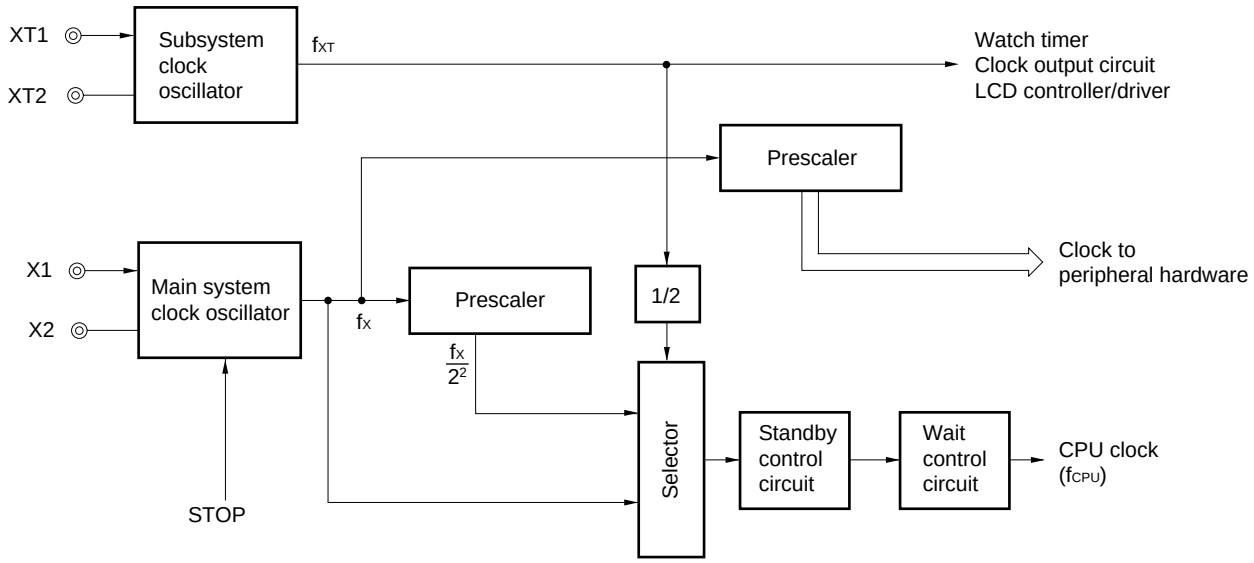
5.2 Clock Generation Circuit

A circuit that generates a system clock is provided.

Moreover, the minimum instruction execution time can be changed as follows:

★
- 0.4 μs/1.6 μs (main system clock: 5.0 MHz)
- 122 μs (subsystem clock: 32.768 kHz)

Figure 5-1. Block Diagram of Clock Generation Circuit



5.3 Timer

The following four timer channels are provided:

- 16-bit timer : 1 channel
- 8-bit timer : 1 channel
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Figure 5-2. Block Diagram of 16-Bit Timer 40

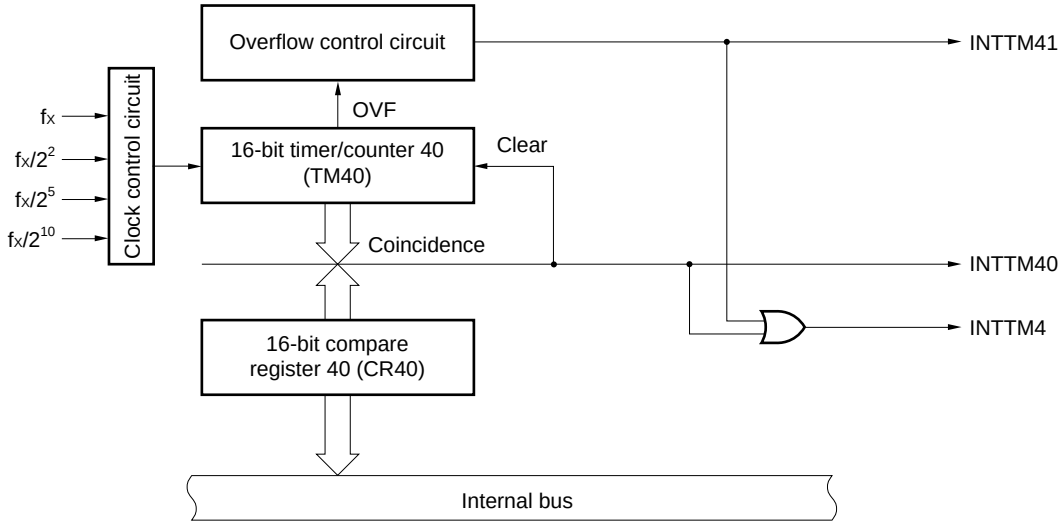


Figure 5-3. Block Diagram of 8-Bit Timer 00

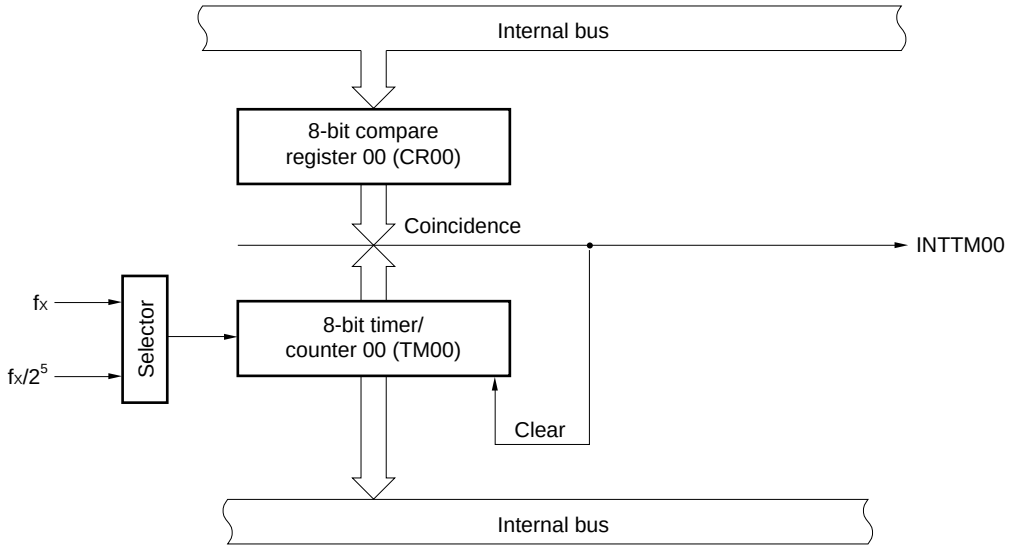
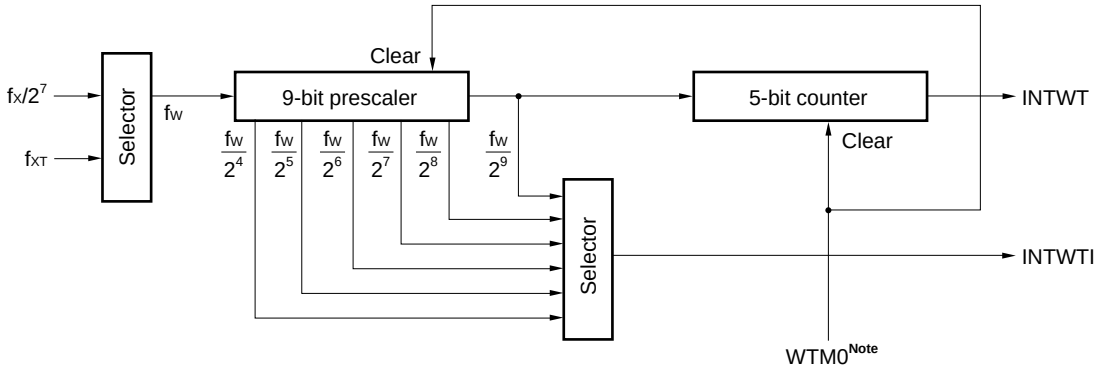
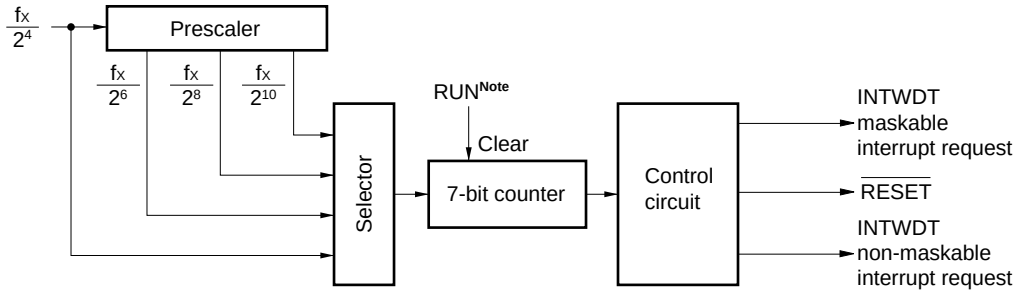


Figure 5-4. Block Diagram of Watch Timer



Note Bit 0 of watch timer mode control register (WTM)

Figure 5-5. Block Diagram of Watchdog Timer



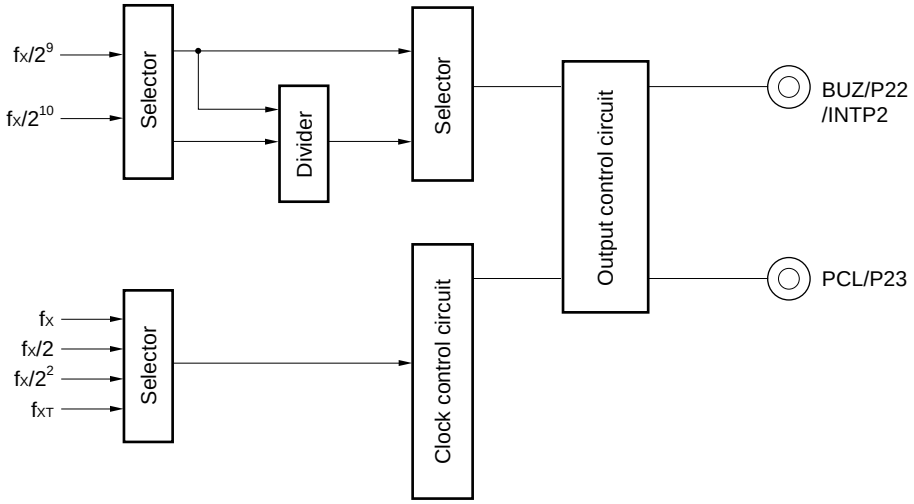
Note Bit 7 of watchdog timer mode register (WDTM)

5.4 Clock Output Circuit

The clock output circuit has the following functions:

- PCL output : Outputs a pulse clock to PCL/P23.
- Buzzer output : Outputs a buzzer frequency to BUZ/P22/INTP2

Figure 5-6. Block Diagram of Clock Output Circuit

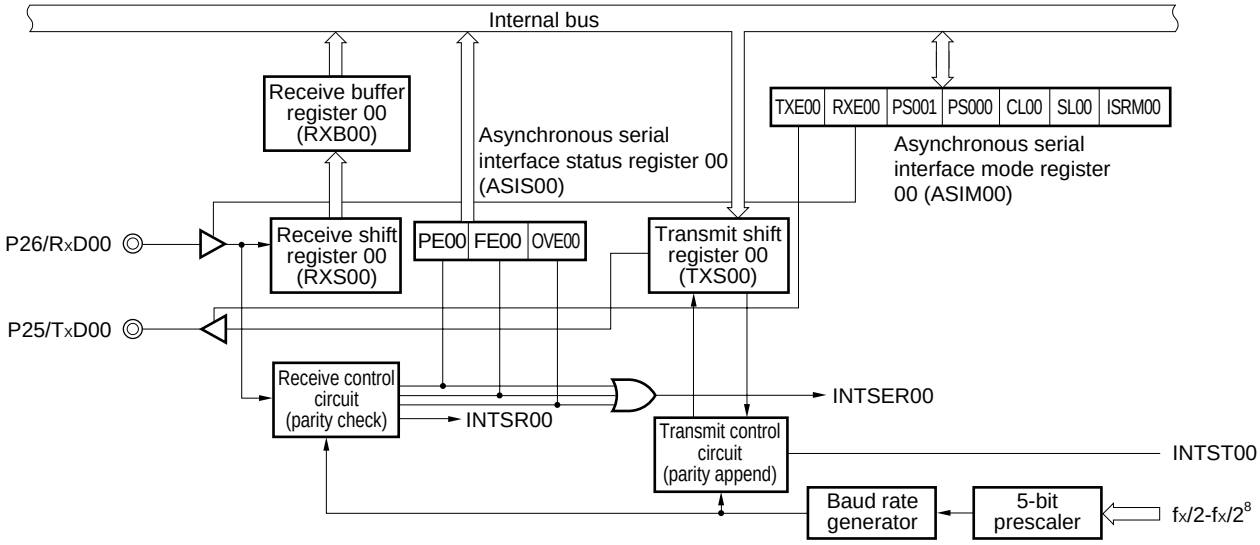


5.5 Serial Interface

The serial interface (UART00) has the following two modes:

- Operation stop mode
- Asyncronous serial interface (UART) mode

Figure 5-7. Block Diagram of Serial Interface (UART00)

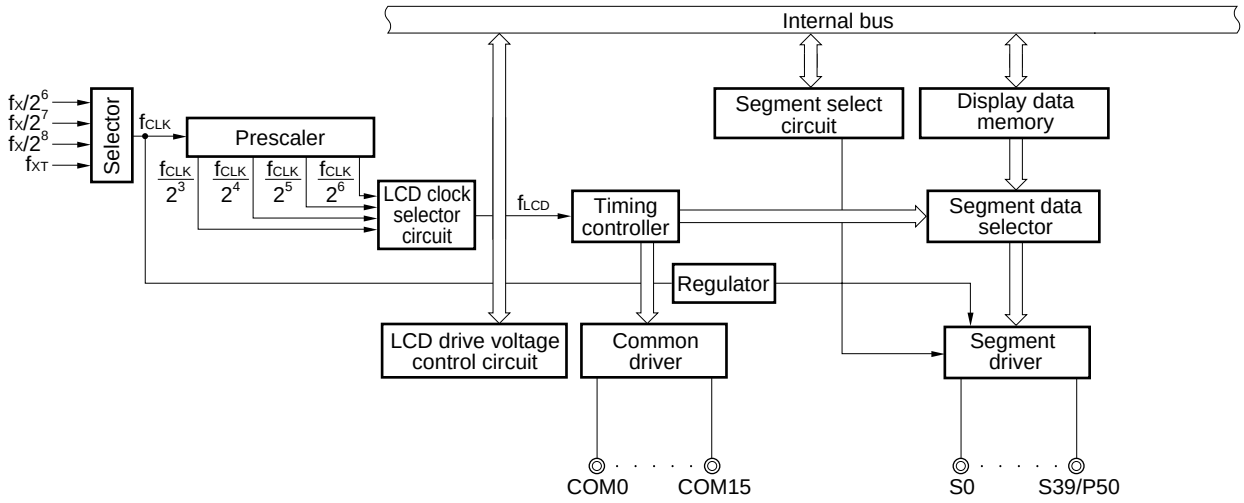


5.6 LCD Controller/Driver

The LCD controller/driver has the following functions:

(1) Automatically output segment and common signals by automatically reading the display data memory.
(2) Operates in a display mode of 1/16 duty (1/5 bias).
Maximum number of display pixels: 640 (40 segment × 16 common)
(3) Four frame frequencies selectable
(4) Up to 40 segment signal output pins (S0 through S39) and 16 common signal output pins (COM0 through COM15).
Eight segment signal output pins can be also used as I/O port pins (P50/S39 through P57/S32) in 1-bit units.
(5) Can also operate with the subsystem clock.

Figure 5-8. Block Diagram of LCD Controller/Driver



6. INTERRUPT FUNCTIONS

The following two types of interrupt functions and a total of 15 interrupt sources are available.

- Non-maskable : 1
- Maskable : 14

Table 6-1. Interrupt Sources

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Detection of input edge of pin	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSER00	Occurrence of reception error of serial interface (UART00)	Internal	000CH	(B)
	5	INTSR00	Completion of reception by serial interface (UART00)		000EH	
	6	INTST00	Completion of transmission by serial interface (UART00)		0010H	
	7	INTTM40	Generation of coincidence signal of 16-bit timer 40		0012H	
	8	INTTM41	Occurrence of overflow of 16-bit timer 40		0014H	
	9	INTTM4	Logical sum between coincidence signal and overflow signal of 16-bit timer 40		0016H	
	10	INTTM00	Generation of coincidence signal of 8-bit timer 00		0018H	
	11	INTWTI	Interval timer interrupt		001AH	
	12	INTWT	Watch timer interrupt		001CH	
	13	INTKR00	Detection of key return signal	External	001EH	(C)

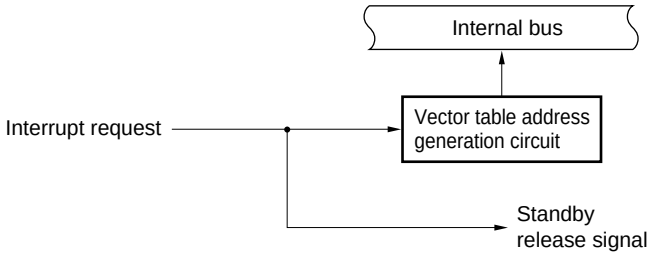
Notes 1. If two or more maskable interrupts occur at the same time, they are processed according to these priorities. Priority 0 is the highest, while 13 is the lowest.

2. (A) through (C) in Basic Configuration Type correspond to (A) through (C) in Figure 6-1.

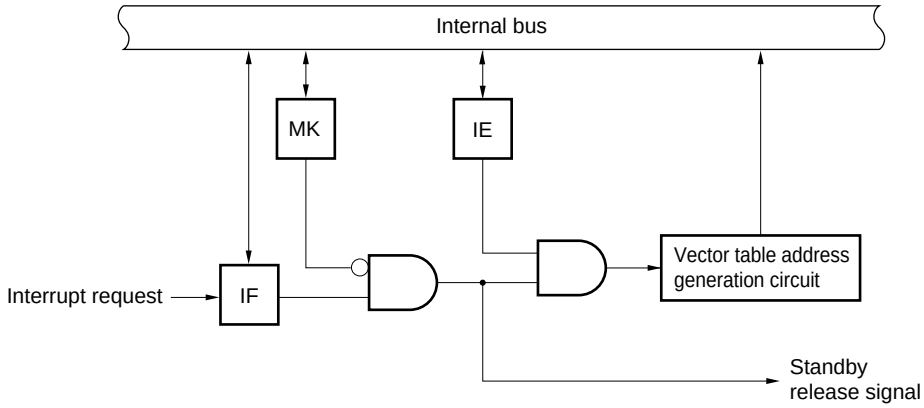
Remark Either a non-maskable or maskable interrupt (internal) can be selected as the interrupt source of the watchdog timer (INTWDT).

Figure 6-1. Basic Configuration of Interrupt Function

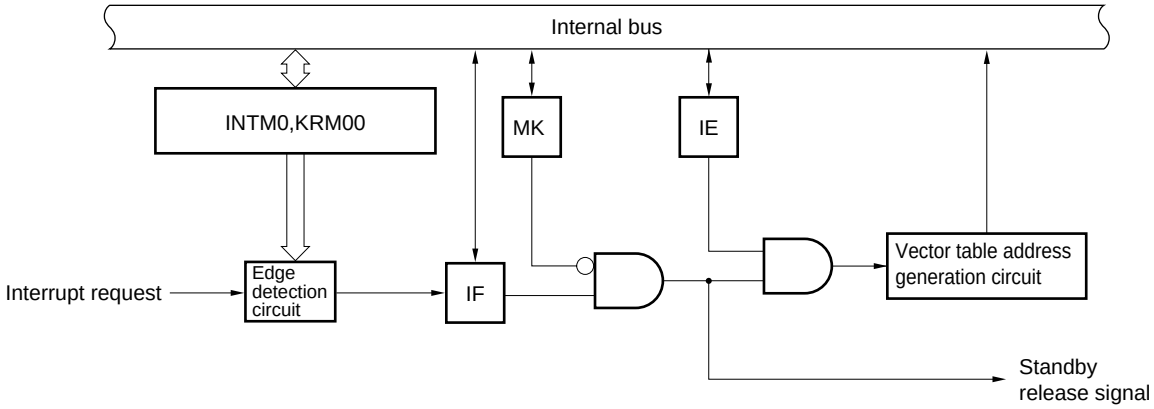
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



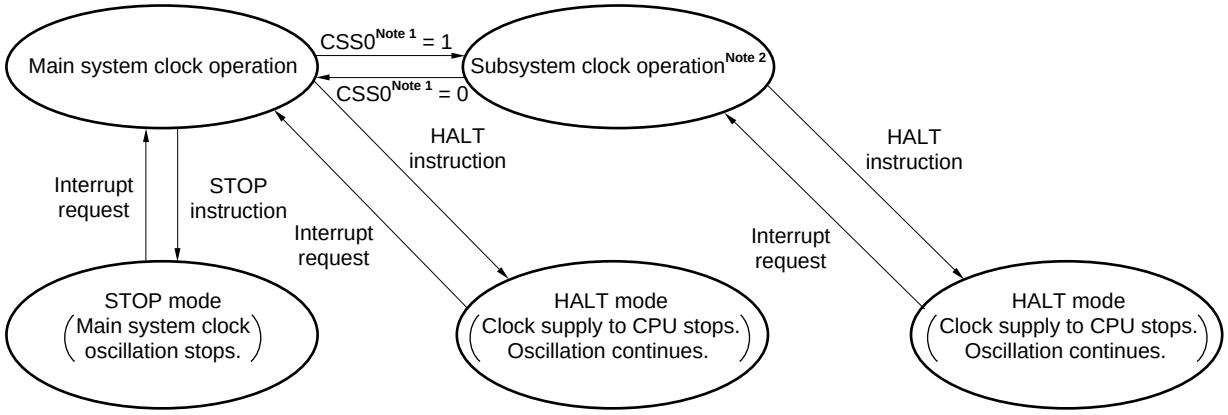
INTM0 : External interrupt mode register 0
KRM00 : Key return mode register 00
IF : Interrupt request flag
IE : Interrupt enable flag
MK : Interrupt mask flag

7. STANDBY FUNCTION

The standby function is used to lower the current consumption and can be used in the following two modes:

- HALT mode: In this mode, the operation of the CPU clock is stopped. By using this mode together with the normal operation mode to operate the system intermittently, the average current consumption can be reduced.
- STOP mode: In this mode, the oscillation of the main system clock is stopped, so that all internal operations based on the main system clock are stopped and the current consumption is minimized.

Figure 7-1. Standby Function



Notes 1. Bit 4 of subclock control register (CSS)

2. Current consumption can be reduced by stopping the main system clock.
When the CPU operates using the subsystem clock, stop the main system clock by using bit 7 (MCC) of the processor clock control register (PCC). The STOP instruction cannot be used.

Caution Make sure in software that the specified oscillation stabilization time has elapsed before the main system clock is selected again if the main system clock has been stopped and the subsystem clock is being used.

8. RESET FUNCTION

The microcontroller can be reset in the following two ways:

- External reset by using the $\overline{\text{RESET}}$ pin
- Internal reset by detecting hang-up of watchdog timer

9. OUTLINE OF INSTRUCTION SET

This section shows a list of the instructions of the μPD789830.

9.1 Conventions

9.1.1 Operand Formats and Syntax

One or more operands are written in the operand field of each instruction in accordance with the operand format and syntax of that instruction (for details, refer to **the assembler specifications**). If two or more operands are shown, select one of them. The uppercase characters, and the symbols #, !, $, [, and] are keywords and must be written as shown. The meanings of these symbols are as follows:

- # : Specifies immediate data.
- ! : Specifies an absolute address.
- $: Specifies a relative address.
- [ ] : Specifies an indirect address.

To specify immediate data, write an appropriate value or label. When using a label, be sure to use the symbols #, !, $, [, and].

The register syntax operands r and rp can be specified as either a function name (such as X, A, and C) or an absolute name (such as R0, R1, and R2 as shown in the parentheses in the table below).

Table 9-1. Operand Formats and Syntax

Format	Syntax
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH Immediate data or label
saddrp	FE20H to FF1FH Immediate data or label (even address only)
addr16	0000H to FFFFH Immediate data or label (even address only when 16-bit data transfer instruction is used)
addr5	0040H to 007FH Immediate data or label (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

9.1.2 Explanation of symbols in operation field

A : A register; 8-bit accumulator
X : X register
B : B register
C : C register
D : D register
E : E register
H : H register
L : L register
AX : AX register pair; 16-bit accumulator
BC : BC register pair
DE : DE register pair
HL : HL register pair
PC : Program counter
SP : Stack pointer
PSW : Program status word
CY : Carry flag
AC : Auxiliary carry flag
Z : Zero flag
IE : Interrupt request enable flag
NMIS : Non-maskable interrupt processing flag
( ) : Contents of memory addressed by address or register contents in ( )
X_H, X_L : High-order 8 bits and low-order 8 bits of 16-bit register
∧ : Logical product (AND)
∨ : Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
$\overline{\quad}$: Inverted data
addr16 : 16-bit immediate data or label
jdisp8 : Signed 8-bit data (displacement value)

9.1.3 Explanation of symbols in flag operation field

(Blank) : Not affected
0 : Cleared to 0
1 : Set to 1
× : Set or cleared depending on result
R : Previously saved value is stored.

9.2 Operation List

Mnemonic	Operand	Bytes	Clocks	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r←byte			
	saddr, #byte	3	6	(saddr)←byte			
	sfr, #byte	3	6	sfr←byte			
	A, r Note 1	2	4	A←r			
	r, A Note 1	2	4	r←A			
	A, saddr	2	4	A←(saddr)			
	saddr, A	2	4	(saddr)←A			
	A, sfr	2	4	A←sfr			
	sfr, A	2	4	sfr←A			
	A, !addr16	3	8	A←(addr16)			
	!addr16, A	3	8	(addr16)←A			
	PSW, #byte	3	6	PSW←byte	×	×	×
	A, PSW	2	4	A←PSW			
	PSW, A	2	4	PSW←A	×	×	×
	A, [DE]	1	6	A←(DE)			
	[DE], A	1	6	(DE)←A			
	A, [HL]	1	6	A←(HL)			
	[HL], A	1	6	(HL)←A			
	A, [HL+byte]	2	6	A←(HL+byte)			
	[HL+byte], A	2	6	(HL+byte)←A			
XCH	A, X	1	4	A↔X			
	A, r Note 2	2	6	A↔r			
	A, saddr	2	6	A↔(saddr)			
	A, sfr	2	6	A↔(sfr)			
	A, [DE]	1	8	A↔(DE)			
	A, [HL]	1	8	A↔(HL)			
	A, [HL+byte]	2	8	A↔(HL+byte)			
MOVW	rp, #word	3	6	rp←word			
	AX, saddrp	2	6	AX←(saddrp)			
	saddrp, AX	2	8	(saddrp)←AX			
	AX, rp Note 3	1	4	AX←rp			
	rp, AX Note 3	1	4	rp←AX			
XCHW	AX, rp Note 3	1	8	AX↔rp			

Notes 1. Except r = A

2. Except r = A, X

3. rp = BC, DE, or HL only

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY←A+byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte	×	×	×
	A, r	2	4	A, CY←A+r	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)	×	×	×
ADDC	A, #byte	2	4	A, CY←A+byte+CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte+CY	×	×	×
	A, r	2	4	A, CY←A+r+CY	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)+CY	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)+CY	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)+CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)+CY	×	×	×
SUB	A, #byte	2	4	A, CY←A–byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte	×	×	×
	A, r	2	4	A, C←A–r	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)	×	×	×
	A, !addr16	3	8	A, CY← A–(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)	×	×	×
SUBC	A, #byte	2	4	A, CY←A–byte–CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte–CY	×	×	×
	A, r	2	4	A, CY←A–r–CY	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)–CY	×	×	×
	A, !addr16	3	8	A, CY←A–(addr16)–CY	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)–CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)–CY	×	×	×
AND	A, #byte	2	4	A←A∧byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∧byte	×		
	A, r	2	4	A←A∧r	×		
	A, saddr	2	4	A←A∧(saddr)	×		
	A, !addr16	3	8	A←A∧(addr16)	×		
	A, [HL]	1	6	A←A∧(HL)	×		
	A, [HL+byte]	2	6	A←A∧(HL+byte)	×		

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A←A∨byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∨byte	×		
	A, r	2	4	A←A∨r	×		
	A, saddr	2	4	A←A∨ (saddr)	×		
	A, !addr16	3	8	A←A∨(addr16)	×		
	A, [HL]	1	6	A←A∨(HL)	×		
	A, [HL+byte]	2	6	A←A∨(HL+byte)	×		
XOR	A, #byte	2	4	A←A⊻byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)⊻byte	×		
	A, r	2	4	A←A⊻r	×		
	A, saddr	2	4	A←A⊻(saddr)	×		
	A, !addr16	3	8	A←A⊻(addr16)	×		
	A, [HL]	1	6	A←A⊻(HL)	×		
	A, [HL+byte]	2	6	A←A⊻(HL+byte)	×		
CMP	A, #byte	2	4	A–byte	×	×	×
	saddr, #byte	3	6	(saddr)–byte	×	×	×
	A, r	2	4	A–r	×	×	×
	A, saddr	2	4	A–(saddr)	×	×	×
	A, !addr16	3	8	A–(addr16)	×	×	×
	A, [HL]	1	6	A–(HL)	×	×	×
	A, [HL+byte]	2	6	A–(HL+byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY←AX+word	×	×	×
SUBW	AX, #word	3	6	AX, CY←AX–word	×	×	×
CMPW	AX, #word	3	6	AX–word	×	×	×
INC	r	2	4	r←r+1	×	×	
	saddr	2	4	(saddr)←(saddr)+1	×	×	
DEC	r	2	4	r←r+1	×	×	
	saddr	2	4	(saddr)←(saddr)–1	×	×	
INCW	rp	1	4	rp←rp+1			
DECW	rp	1	4	rp←rp–1			
ROR	A, 1	1	2	(CY, A_7←A_0, A_{m-1}←A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0←A_7, A_{m+1}←A_m) × 1			×
RORC	A, 1	1	2	(CY←A_0, A_7←CY , A_{m-1}←A_m) × 1			×
ROLC	A, 1	1	2	(CY←A_7, A_0←CY , A_{m+1}←A_m) × 1			×

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit)←1			
	sfr. bit	3	6	sfr. bit←1			
	A. bit	2	4	A. bit←1			
	PSW. bit	3	6	PSW. bit←1	×	×	×
	[HL]. bit	2	10	(HL). bit←1			
CLR1	saddr. bit	3	6	(saddr. bit)←0			
	sfr. bit	3	6	sfr. bit←0			
	A. bit	2	4	A. bit←0			
	PSW. bit	3	6	PSW. bit←0	×	×	×
	[HL]. bit	2	10	(HL). bit←0			
SET1	CY	1	2	CY←1			1
CLR1	CY	1	2	CY←0			0
NOT1	CY	1	2	CY←$\overline{CY}$			×
CALL	!addr16	3	6	(SP−1)←(PC+3)$_H$, (SP−2)←(PC+3)$_L$, PC←addr16, SP←SP−2			
CALLT	[addr5]	1	8	(SP−1)←(PC+1)$_H$, (SP−2)←(PC+1)$_L$, PC$_H$←(00000000, addr5+1), PC$_L$←(00000000, addr5), SP←SP−2			
RET		1	6	PC$_H$, (SP+1), PC$_L$←(SP), SP←SP+2			
RETI		1	8	PC$_H$, (SP+1), PC$_L$←(SP), PSW←(SP+2), SP←SP+3, NMIS←0	R	R	R
PUSH	PSW	1	2	(SP−1)←PSW, SP←SP−1			
	rp	1	4	(SP−1)←rp$_H$, (SP−2)←rp$_L$, SP←SP−2			
POP	PSW	1	4	PSW←(SP), SP←SP+1	R	R	R
	rp	1	6	rp$_H$←(SP+1), rp$_L$← (SP), SP←SP+2			
MOVW	SP, AX	2	8	SP←AX			
	AX, SP	2	6	AX←SP			
BR	!addr16	3	6	PC←addr16			
	$addr16	2	6	PC←PC+2+jdisp8			
	AX	1	6	PC$_H$←A, PC$_L$←2			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 1			
BNC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 0			
BZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B←B–1, then PC←PC+2+jdisp8 if B≠0			
	C, $addr16	2	6	C←C–1, then PC←PC+2+jdisp8 if C≠0			
	saddr, $addr16	3	8	(saddr)←(saddr)–1, then PC←PC+3+jdisp8 if (saddr)≠0			
NOP		1	2	No Operation			
EI		3	6	IE←1 (Enable Interrupt)			
DI		3	6	IE←0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

★ 10. ELECTRICAL SPECIFICATIONS

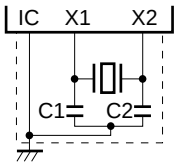
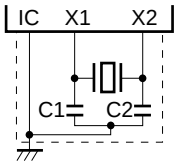
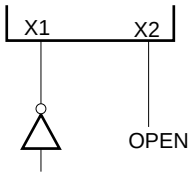
Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
Input voltage	V_{I1}	P00-P07, P10, P11, P20-P23, P25, P26, P30-P34, P50-P57, X1, X2, XT1, XT2, $\overline{\text{RESET}}$	–0.3 to V_{DD} + 0.3	V
	V_{I2}	P24 (N-ch open drain)	–0.3 to +13	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin	–10	mA
		Total of all pins	–30	mA
Low-level output current	I_{OL}	1 pin	30	mA
		Total of all pins	160	mA
Operating temperature	T_A		–20 to +60	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Remark Unless otherwise specified, the characteristics of a pin shared with a port pin are the same as the port pin.

Main System Clock Oscillator Characteristics (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	2.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} has reached MIN. of oscillation start voltage			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		2.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)[Note 1]		2.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		85		250	ns

Notes 1. These parameters indicate only the characteristics of the oscillator. For the instruction execution time, refer to **AC Characteristics**.

2. This is the time required for oscillation to stabilize after reset has been cleared or the STOP mode has been released. Use a resonator that stabilizes within the specified oscillation wait time.

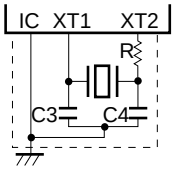
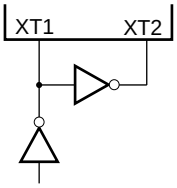
Cautions 1. When using the main system clock oscillator, wire the portion enclosed by the dotted line in the above figures as follows to avoid adverse influence due to wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Keep away from a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as V_{SS0}.**
- **Do not ground the wiring to a pattern through which a high current flows.**
- **Do not extract any signal from the oscillator.**

2. Make sure in software that the specified oscillation stabilization time has elapsed before the main system clock is selected again if the main system clock has been stopped and the subsystem clock is being used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem clock oscillator characteristics (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high- and low-level widths (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. These parameters indicate only the characteristics of the oscillator. For the instruction execution time, refer to **AC Characteristics**.

2. This is the time required for oscillation to stabilize after reset has been cleared or the STOP mode has been released. Use a resonator that stabilizes within the specified oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire the portion enclosed by the dotted line in the above figures as follows to avoid adverse influence due to wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Keep away from a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as V_{SS0}.**
- **Do not ground the wiring to a pattern through which a high current flows.**
- **Do not extract any signal from the oscillator.**

2. The subsystem clock oscillator is designed to have a low amplification factor in order to lower the current consumption. Consequently, it is more susceptible to noise than the main system clock oscillator. Therefore, utmost care must be exercised in wiring when using the subsystem clock oscillator.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V) (1/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}	Per pin				–1	mA
		Total of all pins				–15	mA
Low-level output current	I_{OL}	Per pin				10	mA
		Total of all pins				80	mA
High-level input voltage	V_{IH1}	P00-P07, P10, P11, P23, P25, P50-P57		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20-P22, P26, P30-34		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P24 (N-ch open drain)		0.7 V_{DD}		12	V
	V_{IH4}	X1, X2		V_{DD}–0.1		V_{DD}	V
	V_{IH5}	X1, XT2		V_{DD}–0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	P00-P07, P10, P11, P23, P25, P50-P57		0		0.3 V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$, P20-P22, P26, P30-P34		0		0.2 V_{DD}	V
	V_{IL3}	P24 (N-ch open drain)		0		0.3 V_{DD}	V
	V_{IL4}	X1, X2		0		0.1	V
	V_{IL5}	XT1, XT2		0		0.1	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = 2.7 to 5.5 V, I_{OH} = –100 μA		V_{DD}–0.5			V
Low-level output voltage	V_{OL1}	Pins other than P24	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 2.7 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P24(N-ch open drain)	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 2.7 to 5.5 V, I_{OL} = 1.6 mA			0.4	V

Remark Unless otherwise specified, the characteristics of a pin shared with a port pin are the same as the port pin.

DC Characteristics (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V) (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P07, P10, P11, P20-P23, P25, P26, P30-P34, P50-P57, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 12 V	P24 (N-ch open drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00-P07, P10, P11, P20-P23, P25, P26, P30-P34, P50-P57, $\overline{\text{RESET}}$, P24 (N-ch open drain), except during read			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P24 (N-ch open drain), during read			–30	μA
High-level output leakage current	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R_1	V_{IN} = 0 V, P00-P07, P10, P11, P30-P34		50	100	200	kΩ
Supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operation mode	V_{DD} = 5.0 V ±10%[Note 2]		1.7	3.2	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.45	0.9	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 2]		0.6	1.2	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.3	0.6	mA
	I_{DD3}	32.768-kHz crystal oscillation operation mode[Note 4]	V_{DD} = 5.0 V ±10%		25	50	μA
			V_{DD} = 3.0 V ±10%		12	35	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ±10%		17	34	μA
			V_{DD} = 3.0 V ±10%		5	17	μA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA

Notes 1. Does not include when the LCD is in operation (LCDON20 (bit 7 of LCD20 mode register (LCDM20)) = 1, LIPS20 (bit 4 of LCDM20) = 1), and port current (including the current flowing through the internal pull-up resistor). For the current when the LCD is in operation, refer to **LCD Operating Current** in **LCD Characteristics**.

2. In high-speed mode (when processor clock control register (PCC) is set to 00H)

3. In low-speed mode (when PCC = 02H)

4. When main system clock is stopped

Remark Unless otherwise specified, the characteristics of a pin shared with a port pin are the same as the port pin.

LCD Characteristics (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	$V_{LCD} = V_{DD}$	VAON20 = 0	3.5		5.5	V
			VAON20 = 1	2.7		5.5	V
Segment output voltage[Note 1]	V_{ODS}	When V_{LC0} is selected			V_{LCD}		V
		When V_{LC2} is selected			3/5 V_{LCD}		V
		When V_{LC3} is selected			2/5 V_{LCD}		V
Common output voltage[Note 1]	V_{ODC}	When V_{LC0} is selected			V_{LCD}		V
		When V_{LC1} is selected			4/5 V_{LCD}		V
		When V_{LC4} is selected			1/5 V_{LCD}		V
Segment output ON resistance	RSEG	$V_{LCn} \rightarrow$ SEGp I_O = | 20 μA |			5.0	12.5	kΩ
Common output ON resistance	RCOM	$V_{LCn} \rightarrow$ COMq I_O = | 20 μA |			4.0	10.0	kΩ
LCD input frequency	f_{LCD}	VAON20 = 1		32		78.13	kHz
		VAON20 = 0		7.81		78.13	kHz
LCD operating current[Note 2]	I_{LCD1}	V_{DD} = 5.0 V ± 10 % VAON20 = 0			25	50	μA
	I_{LCD2}	V_{DD} = 3.0 V ± 10 % VAON20 = 1			13	30	μA

Notes 1. Voltage under no load

2. Including the current flowing into the LCD divider resistor. The supply current when LCDON20 = 0 and LIPS20 = 0 (display OFF, internal drive voltage supply OFF) is included in **Supply current I_{DD5} (STOP mode)** in **DC Characteristics**.

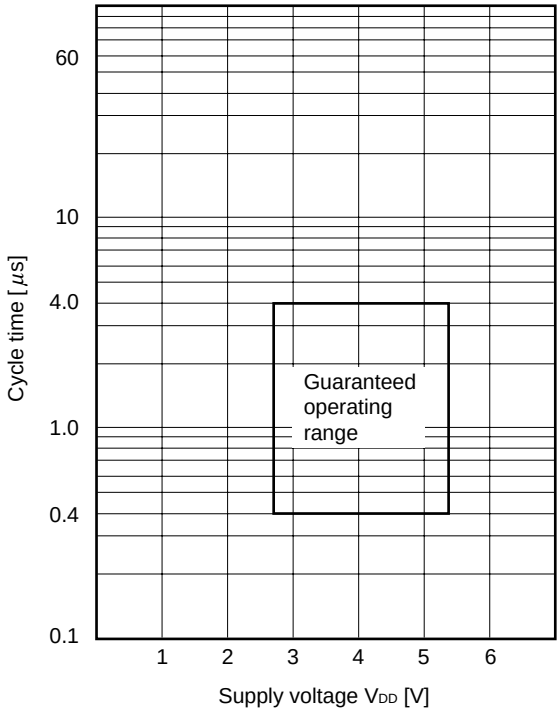
Remark n = 0 to 4
p = 0 to 39
q = 0 to 15

AC Characteristics

(1) Basic operation (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	With main system clock	0.4		4	μs
		With subsystem clock	114	122	125	μs
Interrupt input high- and low-level widths	t_{INTH}, t_{INTL}	INTP0-INTP2	10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}		10			μs

T_{CY} vs V_{DD} (Main system clock)

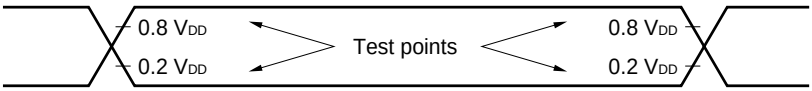


(2) Serial interface (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

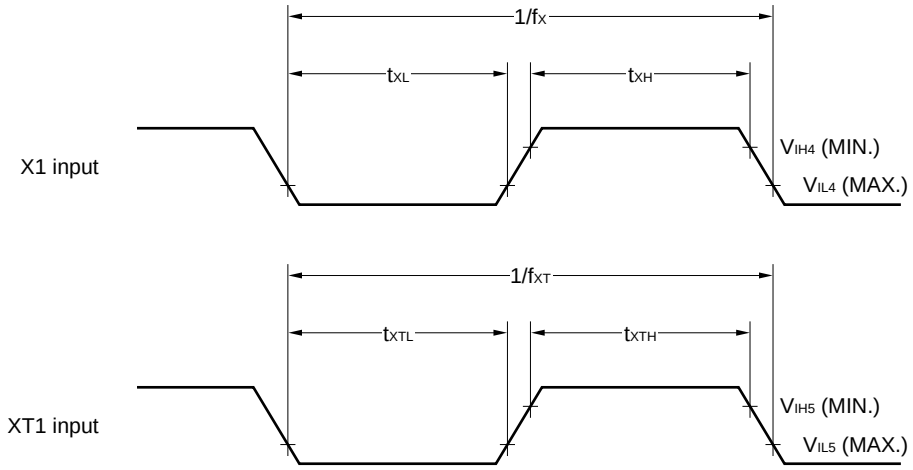
UART mode (dedicated baud rate generator output)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate		f_X = 5.0 MHz			78125	bps

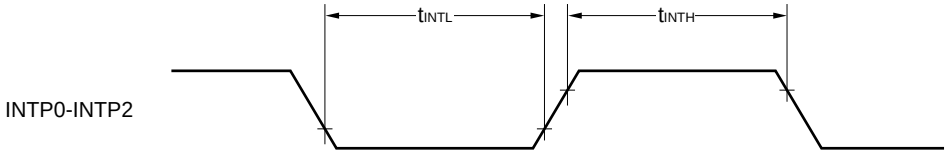
AC Timing Test Points (Except X1 and XT1 input)



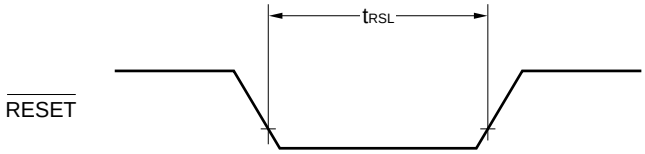
Clock Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Low-Voltage Data Retention Characteristics of Data Memory in STOP Mode (T_A = –20 to +60 °C, V_{DD} = 2.7 to 5.5 V)

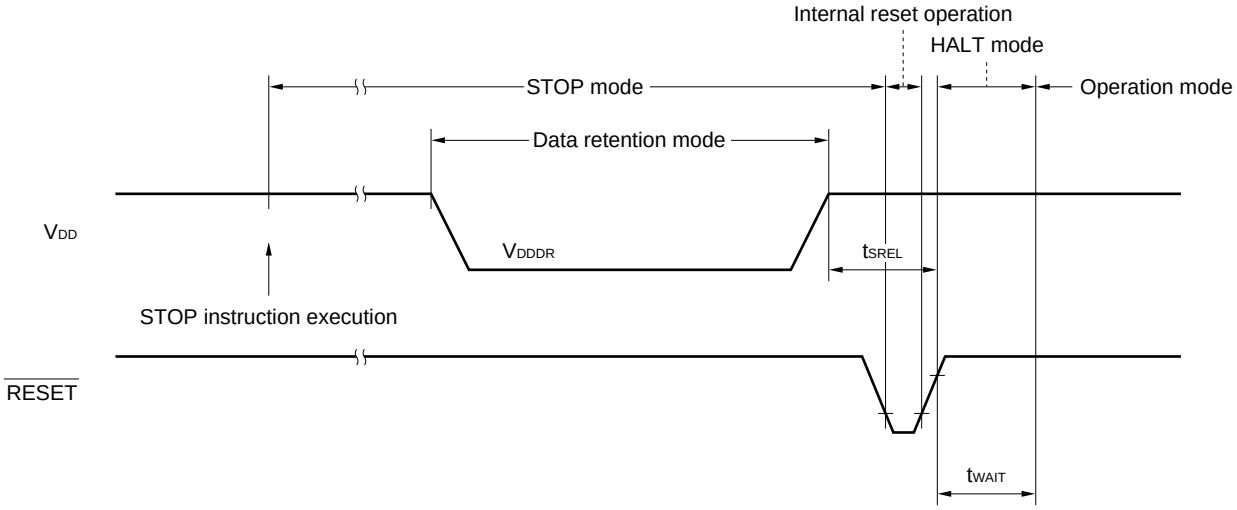
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Released by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time after oscillation has started during which the CPU is stopped to prevent unstable operation.

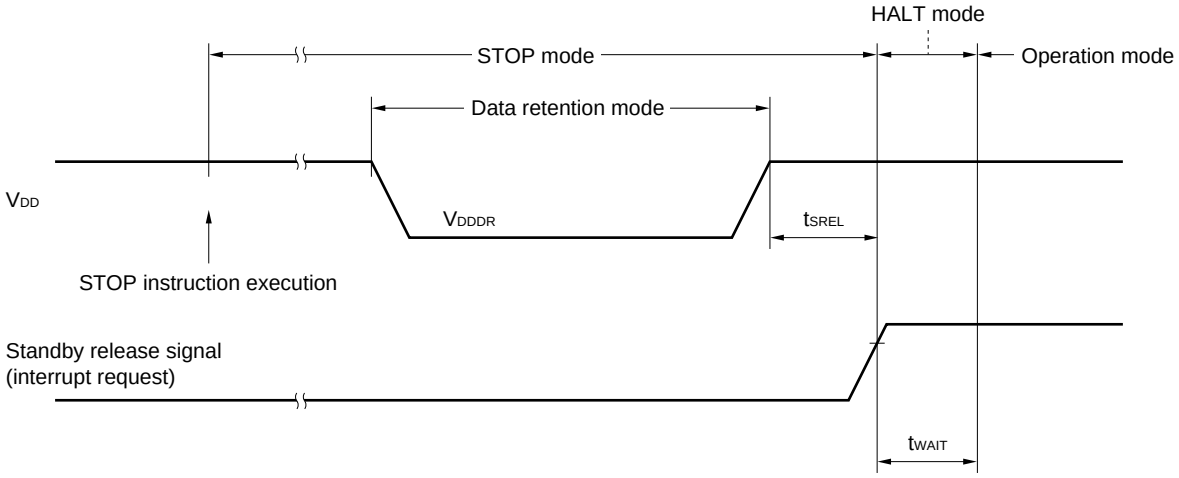
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected by using bits 0 through 2 (OSTS0 through OSTS2) of the oscillation stabilization time select register (OSTS).

Remark fx: Main system clock oscillation frequency

Data Retention Timing (Releasing STOP mode by $\overline{\text{RESET}}$)



Data Retention Timing (Standby release signal: Releasing STOP mode by interrupt signal)



APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of a system using the μPD789830.

Language processor software

RA78K0S[Notes 1, 2, 3]	Common assembler package for 78K/0S series
CC78K0S[Notes 1, 2, 3]	Common C compiler package for 78K/0S series
DF789831[Notes 1, 2, 3]	Device file for μPD789830 subseries
CC78K0S-L[Notes 1, 2, 3]	Common C compiler library source file for 78K/0S series

Flash memory writing tools

★

FlashproIII (FL-PR3[Note 4], PG-FP3)	Flash programmer for microcontrollers with flash memory
FA-100GC[Note 4]	Flash memory writing adapter

★ **Debugging tools**

IE-78K0S-NS in-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power from an AC 100 to 240-V outlet.
IE-70000-98-IF-C interface adapter	Adapter necessary when using a PC-9800 series (except notebook type) as the host machine of the IE-78K0S-NS (supports C bus).
IE-70000-CD-IF-A PC card interface	PC card and interface cable necessary when a notebook type personal computer is used as the host machine of the IE-78K0S-NS (supports PCMCIA socket).
IE-70000-PC-IF-C interface adapter	Adapter necessary when an IBM PC/AT™ or compatible machine is used as the host machine of the IE-78K0S-NS (supports ISA bus).
IE-70000-PCI-IF interface adapter	Adapter necessary when using a personal computer with PCI bus is used as the host machine of the IE-78K0S-NS.
IE-789831-NS-EM1 emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-100GC[Note 4] emulation probe	Probe connecting an in-circuit emulator and target system. For 100-pin plastic QFP.
SM78K0S[Notes 1, 2]	Common system simulator for 78K/0S series
DF789831[Notes 1, 2]	Device file for μPD789830 subseries

Real-time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S series

Notes 1. PC-9800 series (Japanese/English Windows™) based

2. IBM PC/AT or compatible machine (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEWS-OS™) based

4. This is a product of Naito Densei Machida Mfg. Co., Ltd. (Tel: 044-822-3813). Consult Naito Densei Machida Mfg. Co., Ltd. for purchasing.

Remark The RA78K0S, CC78K0S, and SM78K0S are used with the DF789831.

APPENDIX B. RELATED DOCUMENTS

Device-Related Documents

Document Name	Document No.	
	Japanese	English
μPD789830 Data Sheet	U13284J	This document
μPD78F9831 Preliminary Product Information	U13447J	U13477E
μPD789830 Subseries User's Manual	U13679J	U13679E
78K/0S Series User's Manual - Instructions	U11047J	U11047E

Documents on Development Tools (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly language	U11599J	U11599E
	Structured assembly language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator, Windows-based	Reference	U11489J	U11489E
SM78K Series System Simulator	External part user open interface specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger, Windows-based	Reference	U12901J	To be prepared
★ IE-78K0S-NS		U13549J	U13549E
★ IE-789831-NS-EM1		U14202J	U14202E

Documents on Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0S Series OS MX78K0S	Fundamental	U12938J	U12938E

Other Documents

Document Name	Document No.	
	Japanese	English
★ SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality/Reliability Handbook	C12769J	–
Guide to Microcomputer-Related Products by Third Party	U11416J	–

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents referred to in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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