NEC

MOS INTEGRATED CIRCUIT

μPD78P048A

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P048A is a product in the μPD78044F subseries within the 78K/0 series, in which the internal ROM of the μPD78042F, 78043F, 78044F, and 78045F is replaced with one-time PROM or EPROM.

As the μPD78P048A is user-programmable, it is ideal for evaluation in system development, short-run and multiple-device production, and early start-up.

★ **Caution The μPD78P048AKL-S does not provide the reliability intended for mass production of user systems. Use this model only for experiments and evaluation of functions.**

Details of functions are described in the User's Manuals shown below. Be sure to read in design.

μPD78044F subseries User's Manual: U10908E

78K/0 series User's Manual -Instruction: U12326E

FEATURES

- Pin compatible with mask ROM products (except the V_{PP} pin)
- Internal PROM: 60K bytes**Note 1**
- μPD78P048AKL-S: Reprogrammable. (ideal for system evaluation)
- μPD78P048AGF-3B9: Programmable only once (ideal for limited production)
- Internal high-speed RAM: 1024 bytes**Note 1**
- Internal expansion RAM: 1024 bytes**Note 2**
- Buffer RAM: 64 bytes
- FIP™ display RAM: 48 bytes
- Operable in the same supply voltage as mask ROM products: V_{DD} = 2.7 to 6.0 V (except A/D converter)
  A/D converter supply voltage: AV_{DD} = 4.0 to 6.0

Notes 1. Internal PROM and internal high-speed RAM capacities can be changed by memory size switching register (IMS).

2. Internal expansion RAM capacity can be changed by internal expansion RAM size switching register (IXS).

Remark For the difference between ROM products and mask ROM products, refer to **1. DIFFERENCES BETWEEN μPD78P048A AND MASK ROM PRODUCTS**.

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

Document No. U10611EJ2V0DS00 (2nd edition)
Date Published June 1997 N
Printed in Japan

The mark ★ shows major revised points.

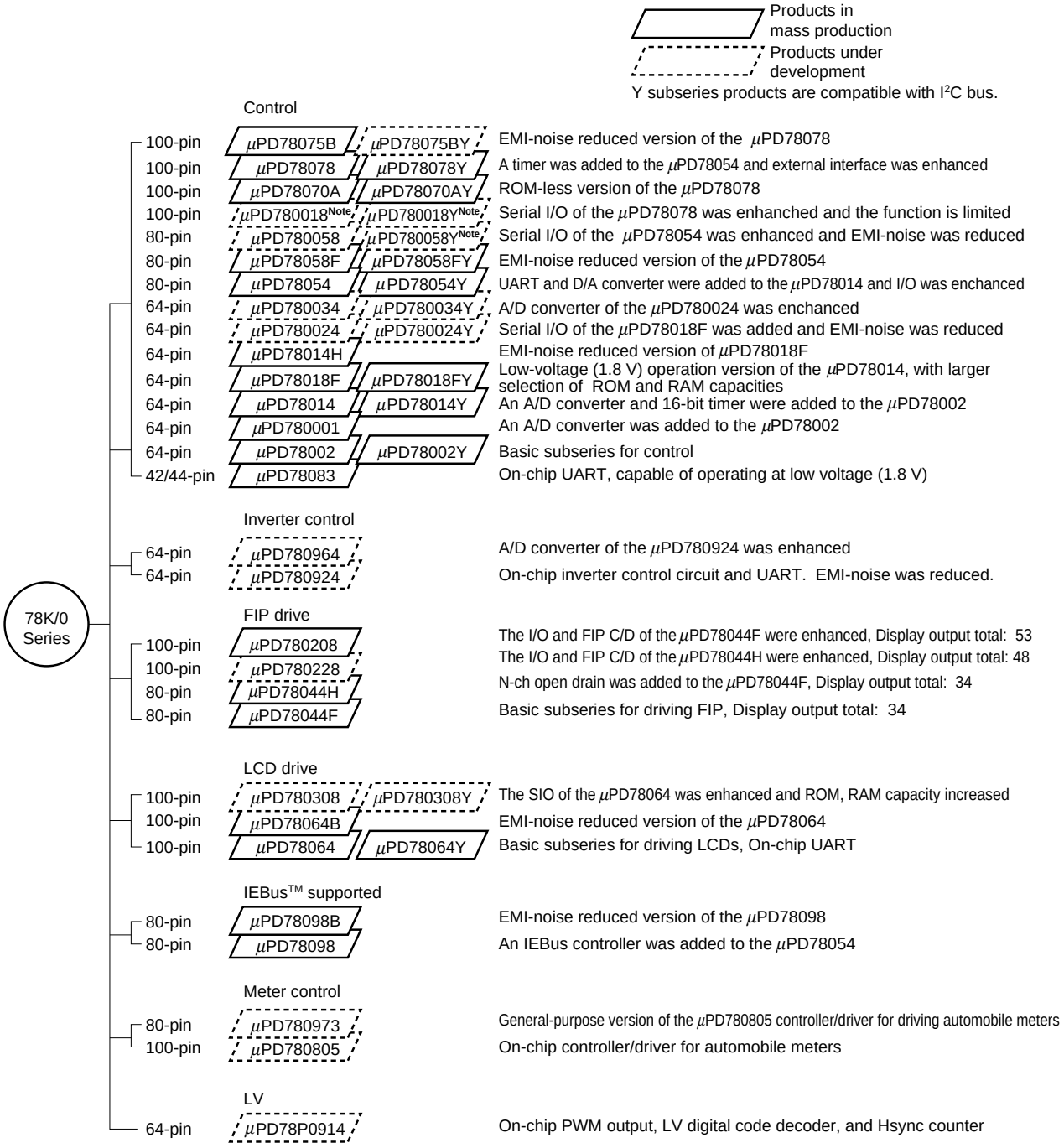
ORDERING INFORMATION

Part Number	Package	Internal ROM	Quality Grade
μPD78P048AGF-3B9	80-pin plastic QFP (14 × 20 mm)	One-time PROM	Standard
μPD78P048AKL-S	80-pin ceramic WQFN	EPROM	Not applicable

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The following shows the 78K/0 Series products development. Subseries name are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K-40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART : 1 ch)	88	1.8 V	○
	μPD78078	48 K-60 K											
	μPD78070A	–									61	2.7 V	
	μPD780018	48 K-60 K							–	2 ch (time division 3-wire: 1ch)	88		
	μPD780058	24 K-60 K	2 ch						2 ch	3 ch (time division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K-60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780034	8 K-32 K					–	8 ch	–	3 ch (UART: 1 ch, time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K-60 K											
	μPD78014	8 K-32 K										2.7 V	
	μPD780001	8 K		–	–					1 ch	39		–
	μPD78002	8 K-16 K			1 ch		–				53		○
	μPD78083				–		8 ch			1 ch (UART: 1 ch)	33	1.8 V	–
Inverter control	μPD780964	8 K-32 K	3 ch	**Note**	–	1 ch	–	8 ch	–	2 ch (UART: 2 ch)	47	2.7 V	○
	μPD780924						8 ch	–					
FIP drive	μPD780208	32 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780228	48 K-60 K	3 ch	–	–					1 ch	72	4.5 V	
	μPD78044H	32 K-48 K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16 K-40 K								2 ch			
LCD drive	μPD780308	48 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time division UART: 1ch)	57	2.0 V	–
	μPD78064B	32 K								2 ch (UART : 1 ch)			
	μPD78064	16 K-32 K											
IEBus supported	μPD78098B	40 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART : 1 ch)	69	2.7 V	○
	μPD78098	32 K-60 K											
Meter control	μPD780973	24 K-32 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	2 ch (UART : 1 ch)	56	4.5 V	–
	μPD780805	40 K-60 K	2 ch				8 ch				39	2.7 V	
LV	μPD78P0914	32 K	6 ch	–	–	1 ch	8 ch	–	–	2 ch	54	4.5 V	○

Note 10-bit timer: 1 channel

FUNCTION DESCRIPTION

Item		Function
Internal memory	PROM	60 K bytes[Note 1]
	High-speed RAM	1024 bytes[Note 1]
	Expansion RAM	1024 bytes[Note 2]
	Buffer RAM	64 bytes
	FIP display RAM	48 bytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		Instruction execution time variable function is built in.
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (when operating at 5.0 MHz)
	When subsystem clock is selected	122 μs (when operating at 32.768 kHz)
Instruction set		• Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation)
I/O ports (including FIP dual-function pin)		Total : 68 • CMOS input : 2 • CMOS input/output : 27 • N-ch open-drain input/output : 5 • P-ch open-drain input/output : 16 • P-ch open-drain output : 18
FIP controller/driver		Display output total : 34 • No. of segments : 9 to 24 • No. of digits : 2 to 16
A/D converter		• 8-bit resolution × 8 ch • Supply voltage: AV_{DD} = 4.0 to 6.0 V
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 ch • 3-wire serial I/O mode (on-chip max. 64 bytes automatic data transmit/receive function): 1 ch
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Clock timer : 1 channel • Watchdog timer : 1 channel • 6-bit up/down counter : 1 channel
Timer output		3 (14-bit PWM output capability : 1)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz (When operating at main system clock 5.0 MHz) 32.768 kHz (when operating at subsystem clock 32.768 kHz)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz (when operating at main system clock 5.0 MHz)
Vectored interrupt sources	Maskable	Internal: 10, External: 4
	Non-maskable	Internal: 1
	Software	1
Test input		Internal: 1
Supply voltage		V_{DD} = 2.7 to 6.0 V
Package		• 80-pin plastic QFP (14 × 20 mm) • 80-pin ceramic WQFN

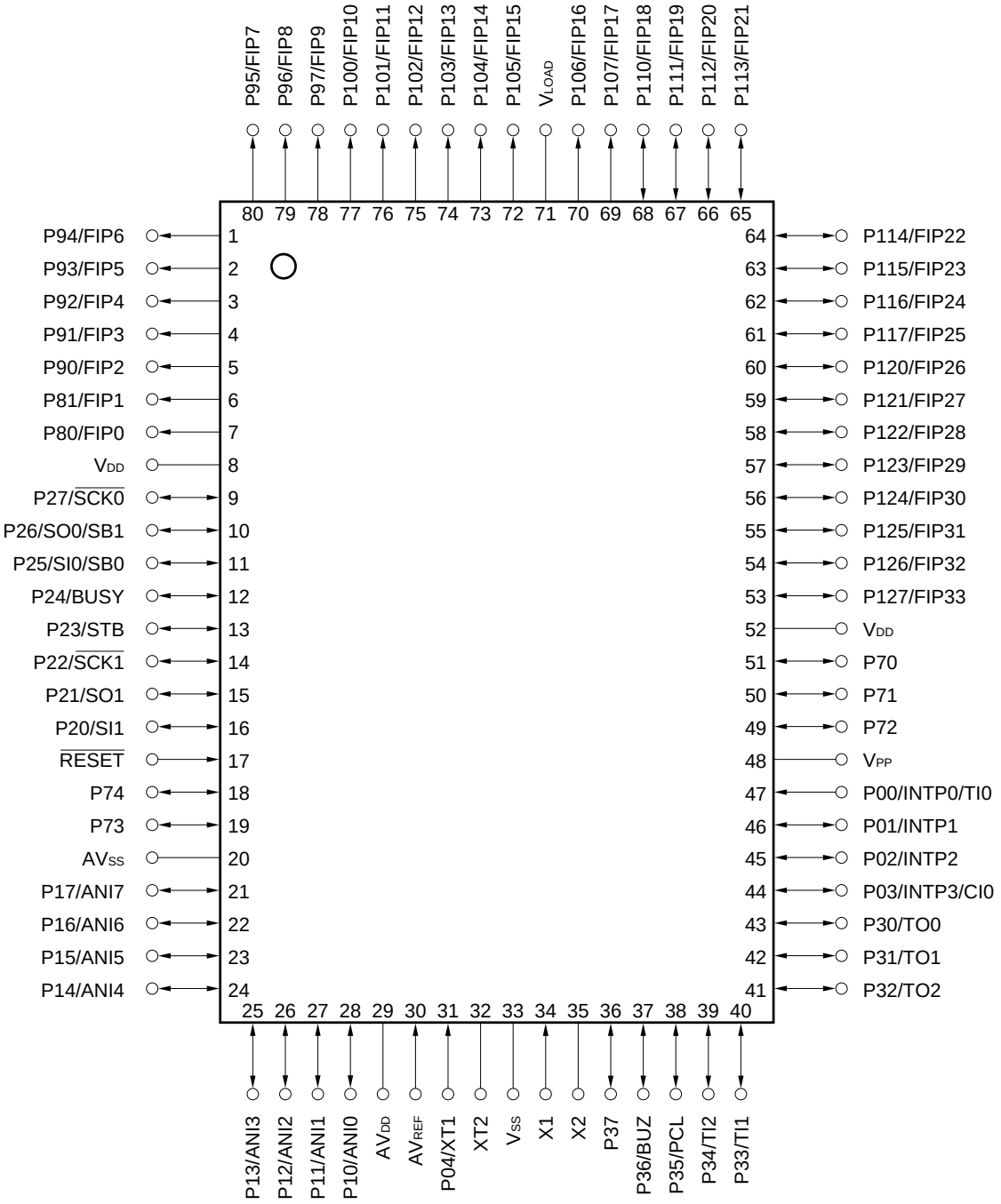
Notes 1. Internal PROM/internal high-speed RAM capacity can be changed by memory size switching register (IMS).

2. Internal expansion RAM capacity can be changed by internal expansion RAM size switching register (IXS).

PIN CONFIGURATION (Top View)

(1) Normal operating mode

- **80-pin plastic QFP (14 × 20 mm)**
  μPD78P048AGF-3B9
- **80-pin ceramic WQFN**
  μPD78P048AKL-S



Cautions 1. Connect V_{PP} pin directly to V_{SS}.

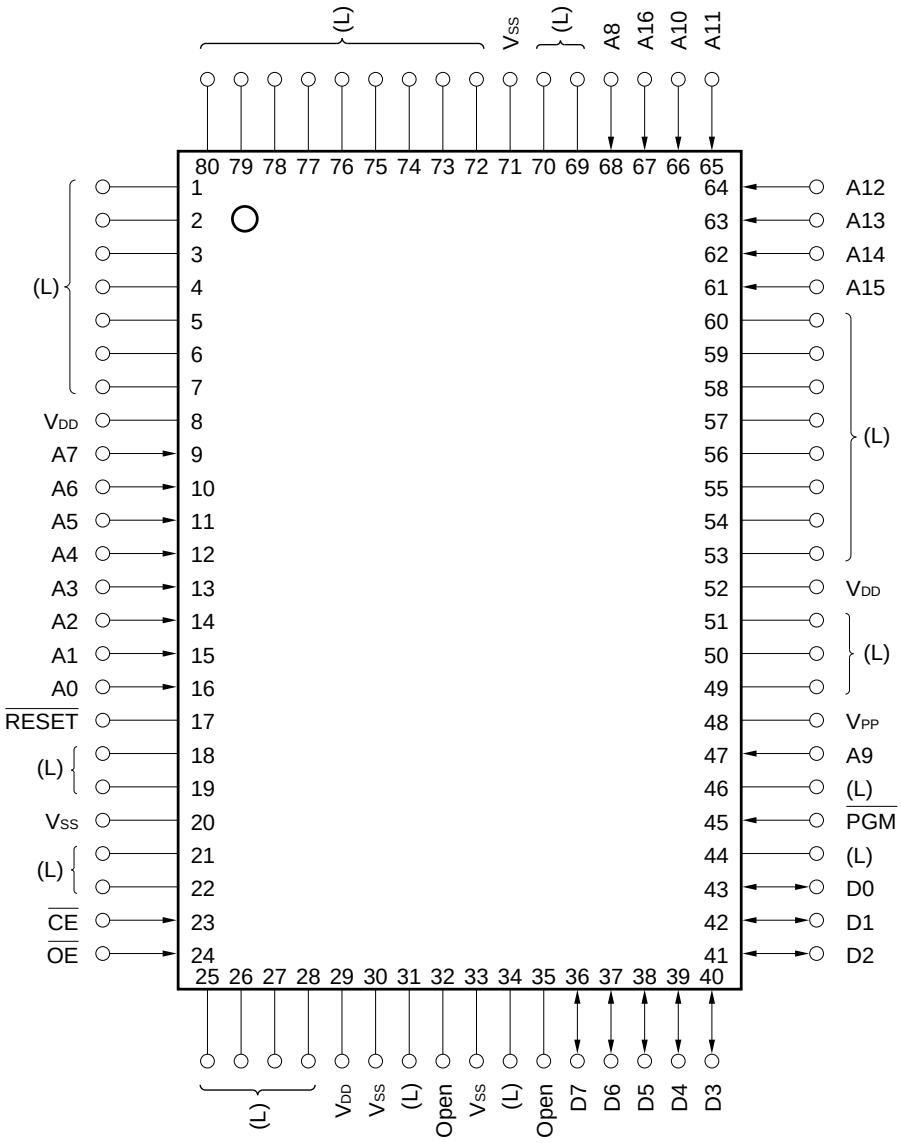
2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

P00 to P04	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P70 to 74	:	Port 7
P80, P81	:	Port 8
P90 to P97	:	Port 9
P100 to P107	:	Port 10
P110 to P117	:	Port 11
P120 to 127	:	Port 12
INTP0 to INTP3	:	Interrupt from Peripherals
TI0 to TI2	:	Timer Input
TO0 to TO2	:	Timer Output
CI0	:	Clock Input
SB0, SB1	:	Serial Bus
SI0, SI1	:	Serial Input
SO0, SO1	:	Serial Output
$\overline{SCK0}$, $\overline{SCK2}$	:	Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
FIP0 to FIP33	:	Fluorescent Indicator Panel
V_{LOAD}	:	Negative Power Supply
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground

(2) PROM programming mode

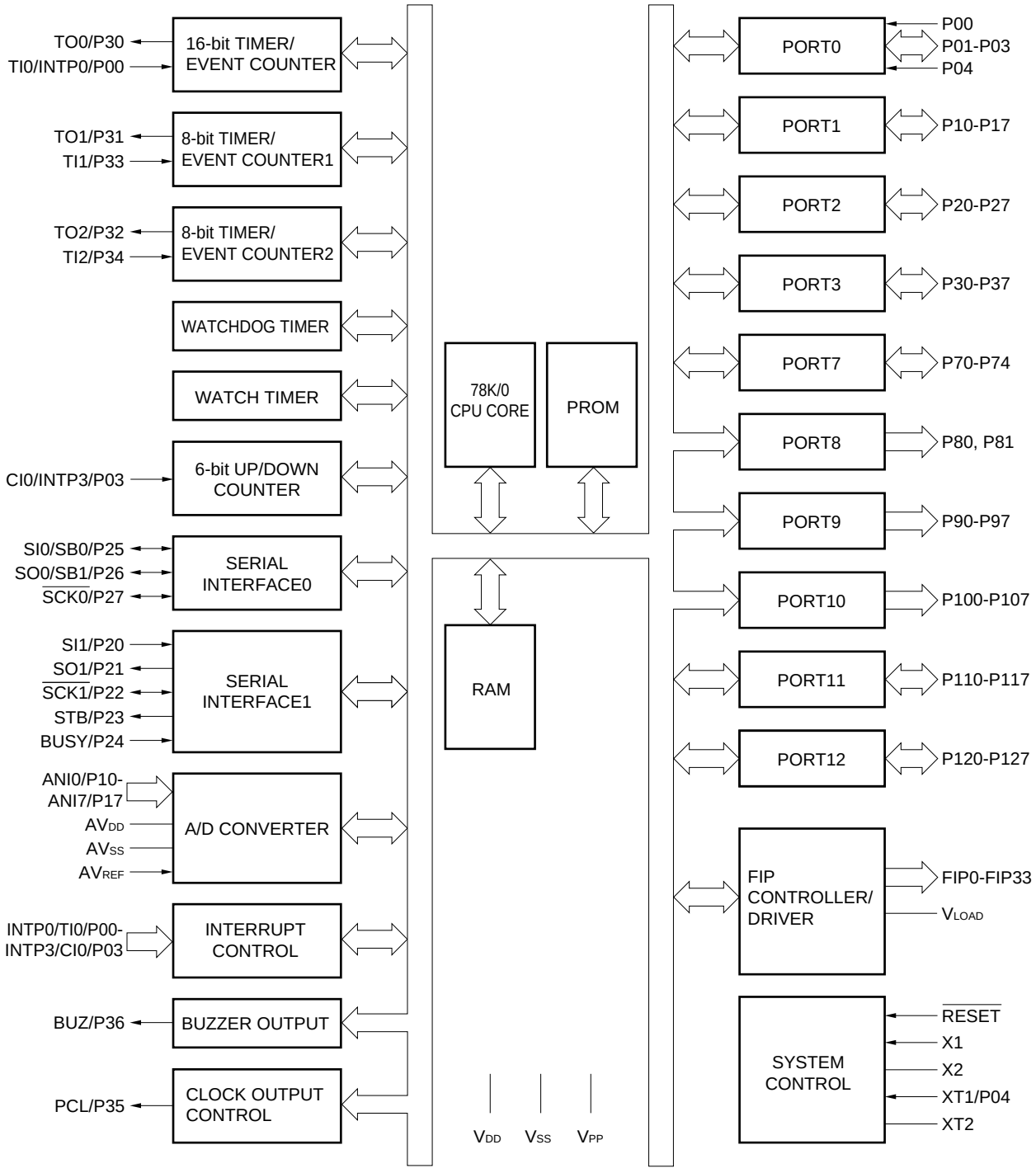
- **80-pin plastic QFP (14 × 20 mm)**
  μPD78P048AGF-3B9
- **80-pin ceramic WQFN**
  μPD78P048AKL-S



Cautions 1. (L) : Individually connect to VSS via a pull-down resistor.
2. VSS : Connect to ground.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open : No connection.

A0 to A16	: Address Bus	$\overline{\text{RESET}}$	: Reset
D0 to D7	: Data Bus	V_{DD}	: Power Supply
$\overline{\text{CE}}$	: Chip Enable	V_{PP}	: Programming Power Supply
$\overline{\text{OE}}$	: Output Enable	V_{SS}	: Ground
$\overline{\text{PGM}}$	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78P048A AND MASK ROM PRODUCTS

The μPD78P048A is a single-chip microcontroller with an on-chip one-time writable PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions except for PROM specification, and mask option, to the same as those of mask ROM products by setting the memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

Differences between the μPD78P048A and mask ROM products (μPD78042F, 78043F, 78044F, and 78045F) are shown in Table 1-1.

★ **Table 1-1. Differences between μPD78P048A and Mask ROM Products**

Item	μPD78P048A	Mask ROM Products
Internal ROM structure	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	60K bytes	μPD78042F: 16K bytes μPD78043F: 24K bytes μPD78044F: 32K bytes μPD78045F: 40K bytes
Internal high-speed RAM capacity	1024K bytes	μPD78042F: 512 bytes μPD78043F: 512 bytes μPD78044F: 1024 bytes μPD78045F: 1024 bytes
Changes of internal ROM and internal high-speed RAM capacities by memory size switching register (IMS)	Available**Notes 1**	Not available
Change of internal expansion RAM capacity by internal expansion RAM size switching register (IXS)	Available**Notes 2**	Not available
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask option with internal pull-down resistor for pins P30-P37, P106, P107, P110-P117, and P120-P127.	No	Yes
Mask option with internal pull-up resistor for pins P70-P74.	No	Yes
Electrical characteristics	Refer to the **Data Sheet** for each product.	

Notes 1. The internal PROM becomes to 60K bytes and the internal high-speed RAM becomes 1024 bytes by the $\overline{\text{RESET}}$ input.

2. The internal expansion RAM becomes to 1024 bytes by the $\overline{\text{RESET}}$ input.

Caution Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).

2. PIN FUNCTION

2.1 Pins in Normal Operating Mode

(1) Port pins (1/2)

Pin Name	Input/Output	Function		On Reset	Dual-Function Pin
P00	Input	Port 0	Input only Input	Input	INTP0/TI0
P01	Input/output	5-bit input/ output port	Input/Output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor in software.	Input	INTP1
P02					INTP2
P03					INTP3/CI0
P04[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor in software.[Note 2]		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use an on-chip pull-up resistor in software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. Direct LED drive capability. When used as the input port, it is possible to use an on-chip pull-up resistor in software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–

Notes 1. When the P04/XT1 pins are used as input ports, processor clock control register (PCC) bit 6 (FRC) should be set to 1 (the subsystem clock oscillator incorporated feedback resistor should not be used).

2. When the P10/ANI0 to P17/ANI7 pins are used as A/D converter analog input, port 1 should be set to the input mode. The on-chip pull-up resistor is not automatically used.

(1) Port pins (2/2)

Pin Name	Input/Output	Function	On Reset	Dual-Function Pin
P70 to P74	Input/output	Port 7 N-ch open-drain 5-bit input/output port. Direct LED drive capability. Input/output is specifiable bit-wise.	Input	—
P80, P81	Output	Port 8 P-ch open-drain 2-bit high-voltage output port. Direct LED drive capability. Pull-down resistor (connected to V_{LOAD}) on chip.	Output	FIP0, FIP1
P90 to P97	Output	Port 9 P-ch open-drain 8-bit high-voltage output port. Direct LED drive capability. Pull-down resistor (connected to V_{LOAD}) on chip.	Output	FIP2 to FIP9
P100 to P107	Output	Port 10 P-ch open-drain 8-bit high-voltage output port. Direct LED drive capability. Pull-down resistor (connected to V_{LOAD}) on chip in P100 to P105.	Output	FIP10 to FIP17
P110 to P117	Input/output	Port 11 P-ch open-drain 8-bit high-voltage output port. Input/output is specifiable bit-wise.	Input	FIP18 to FIP25
P120 to P127	Input/output	Port 12 P-ch open-drain 8-bit high-voltage output port. Direct LED drive capability. Input/output is specifiable bit-wise.	Input	FIP26 to FIP33

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	On Reset	Dual-Function Pin
INTP0	Input	Specifiable valid edges (rising edge, falling edge, and both rising and falling edges). External interrupt request input	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt request input	Input	P03/CI0
SI0	Input	Serial data input of the serial interface	Input	P25/SB0
SI1				P20
SO0	Output	Serial data output of the serial interface	Input	P26/SB1
SO1				P21
SB0	Input/output	Serial data input/output of the serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial clock input/output of the serial interface	Input	P27
$\overline{SCK1}$				P22
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (shared with 14-bit PWM output)	Iutput	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
CI0	Input	Clock input of the 6-bit up/down counter	Input	P03/INTP3
PCL	Output	Clock output (for main system clock, subsystem clock trimming)	Input	P35
BUZ	Output	Buzzer output	Input	P36
FIP0, FIP1	Output	FIP controller/driver digit output high-voltage high-current output	Output	P80, P81
FIP2 to FIP9				P90 to P97
FIP10 to FIP15	Output	FIP controller/driver digit/segment output high-voltage high-current output	Output	P100 to P105
FIP16, FIP17	Output	FIP controller/driver segment output high-voltage output	Output	P106, P107
FIP18 to FIP25			Input	P110 to P117
FIP26 to FIP33				P120 to P127
V_{LOAD}	—	FIP controller/driver pull-down resistor connection	—	—
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}	—	—

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	On Reset	Dual-Function Pin
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{PP}	—	Directly connected to V_{SS}	—	—
V_{SS}	—	Ground potential	—	—

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/ verification
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$	Input	Read strobe input to PROM
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programing mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommeded connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, refer to **Figure 2-1**.

Table 2-1. Type of Input/Output Circuit of Each Pin

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connecting Method when Unused
P00/TI0/INTP0	2	Input	Connect to V_{SS}.
P01/INTP1	8-A	Input/output	Individually connect to V_{SS} via resistor
P02/INTP2			
P03/INTP3/CI0			
P04/XT1	16	Input	Connect to V_{DD} or V_{SS}.
P10A/ANI0 to P17/AN7	11	Input/output	Individually connect to V_{DD} or V_{SS} via resistor
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0			
P26/SO0/SB1	10-A		
P27/$\overline{SCK0}$			
P30/TO0			
P31/TO1	5-A		
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P70 to P74	13-D		
P80/FIP0, P81/FIP1	14	Output	Leave open.
P90/FIP2 to P97/FIP9			
P100/FIP10 to P105/FIP15			
P106/FIP16, P107/FIP17	14-B		
P110/FIP18 to P117/FIP25	15-B	Input/output	Individually connect to V_{DD} or V_{SS} via resistor
P120/FIP26 to P127/FIP33			
$\overline{RESET}$	2	Input	—
XT2	16	–	Leave open
AV_{REF}	–		Connect to V_{SS}
AV_{DD}			Connect to V_{DD}
AV_{SS}			Connect to V_{SS}
V_{LOAD}			
V_{PP}			Directly connect to V_{SS}

Figure 2-1. List of Pin Input/Output Circuits (1/2)

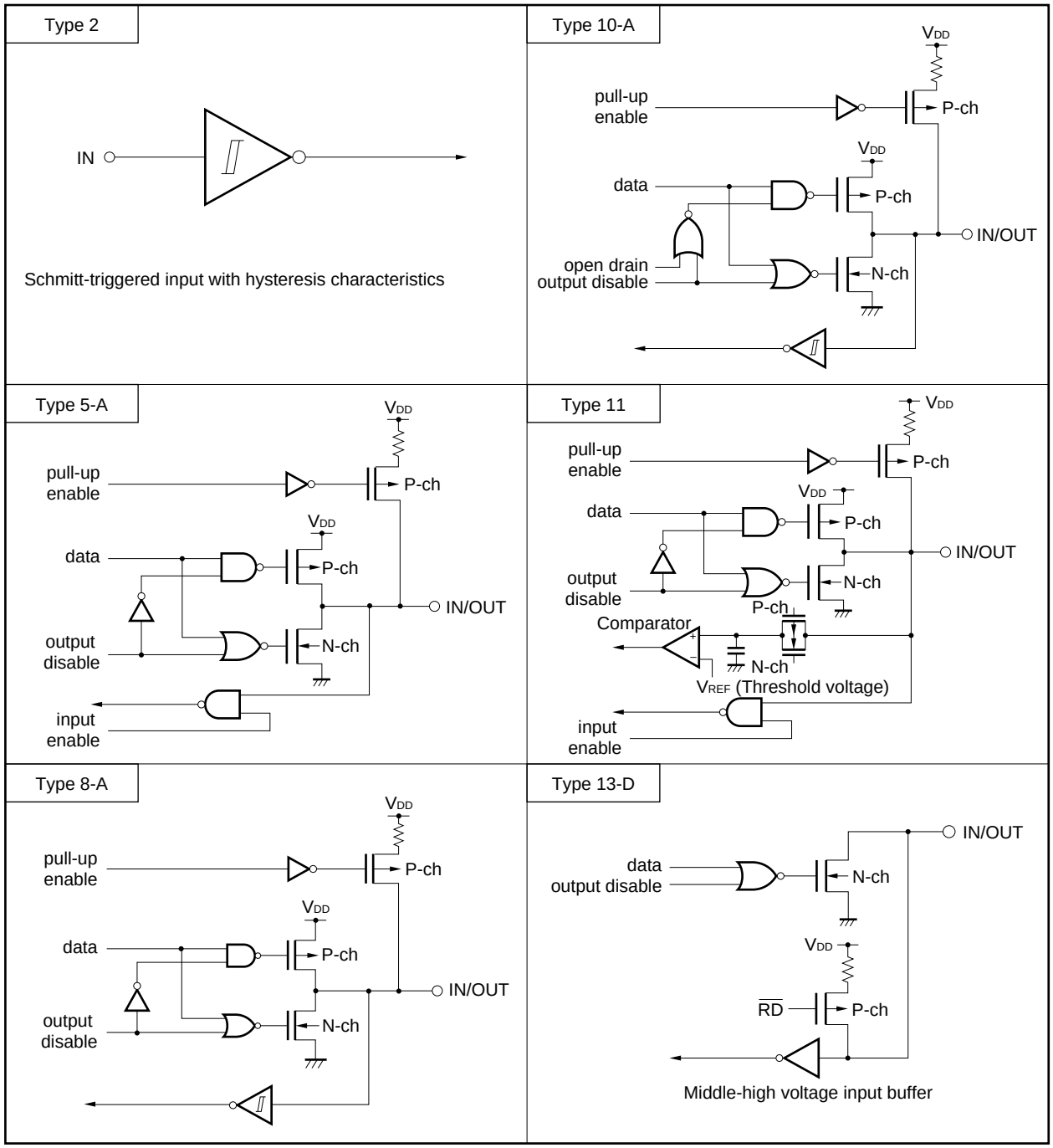
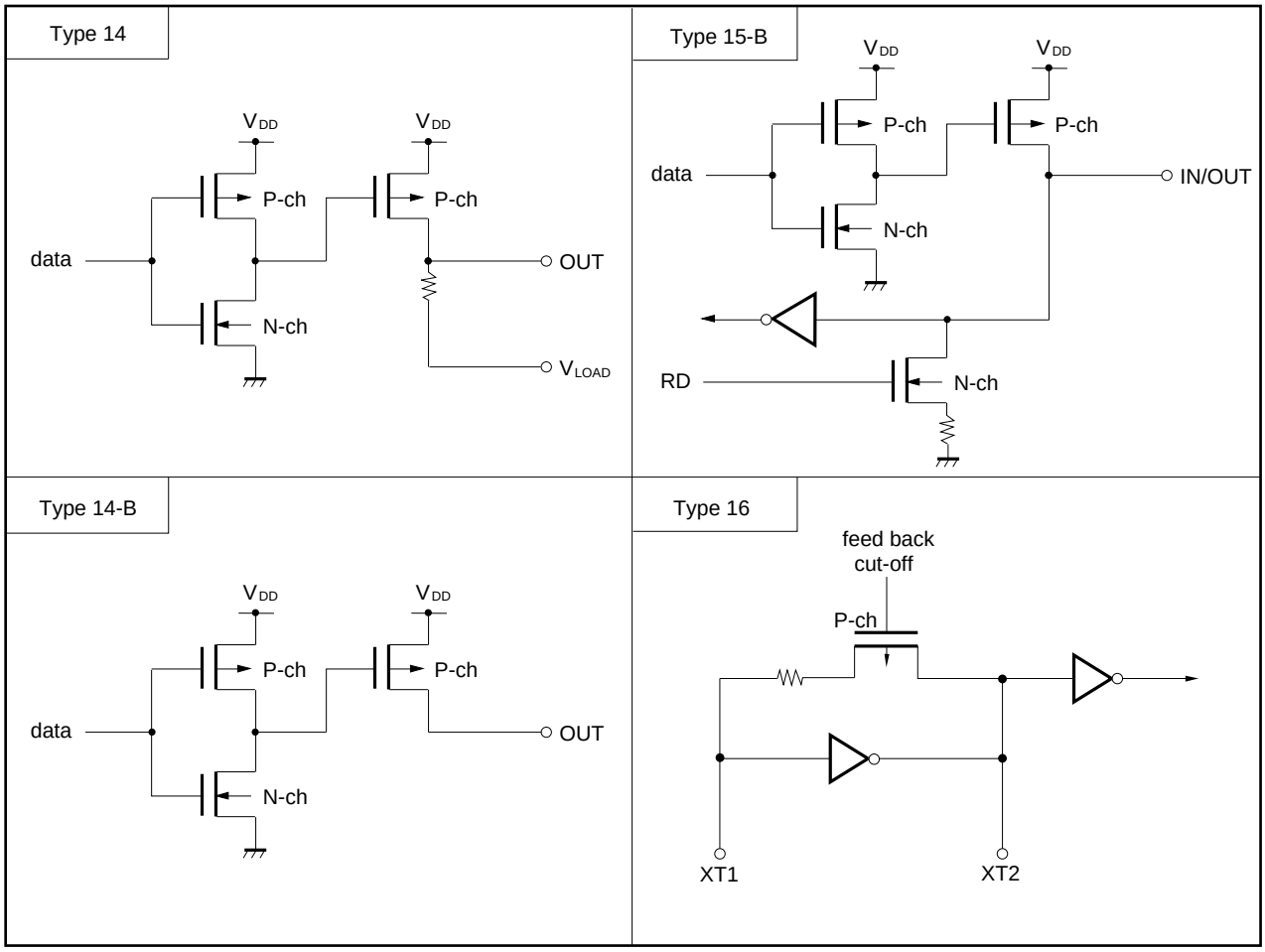


Figure 2-1. List of Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM product having different internal memories.

The IMS is set up by the 8-bit memory manipulation instruction.

CFH will result by the $\overline{\text{RESET}}$ input.

Figure 3-1. Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	On Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16K bytes
0	1	1	0	24K bytes
1	0	0	0	32K bytes
1	0	1	0	40K bytes
1	1	1	1	60K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which makes the memory mapping the same as that of the various mask ROM model.

Table 3-1. Memory Size Switching Register Setting Values

Target Mask ROM Product	IMS Setting Value
μPD78042F	44H
μPD78043F	46H
μPD78044F	C8H
μPD78045F	CAH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

By using this register, the internal expansion RAM of the μPD78P048A can be mapped in the same manner as a mask ROM model.

IXS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to 0AH at $\overline{\text{RESET}}$.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	On reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selects internal expansion RAM capacity
1	0	1	0	1024 bytes
1	1	0	0	No internal expansion RAM
Other than above				Setting prohibited

Table 4-1 shows the value settings of IXS to map the internal expansion RAM of the μPD78P048A in the same manner as the respective mask ROM models.

Table 4-1. Memory Size Switching Register Setting Values

Mask ROM Model	IXS Value Setting
μPD78042F	0CH
μPD78043F	
μPD78044F	
μPD78045F	

5. PROM PROGRAMMING

The μPD78P048A has an on-chip 60K-byte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For connecting unused pins, refer to **PIN CONFIGURATION (2) PROM programming mode**.

Caution Program writing should be performed in the address range 0000H to EFFFH (the last address, EFFFH, should be specified). Writing cannot be performed with a PROM programmer that cannot specify the write addresses.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

× : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P048As are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly, after the write.

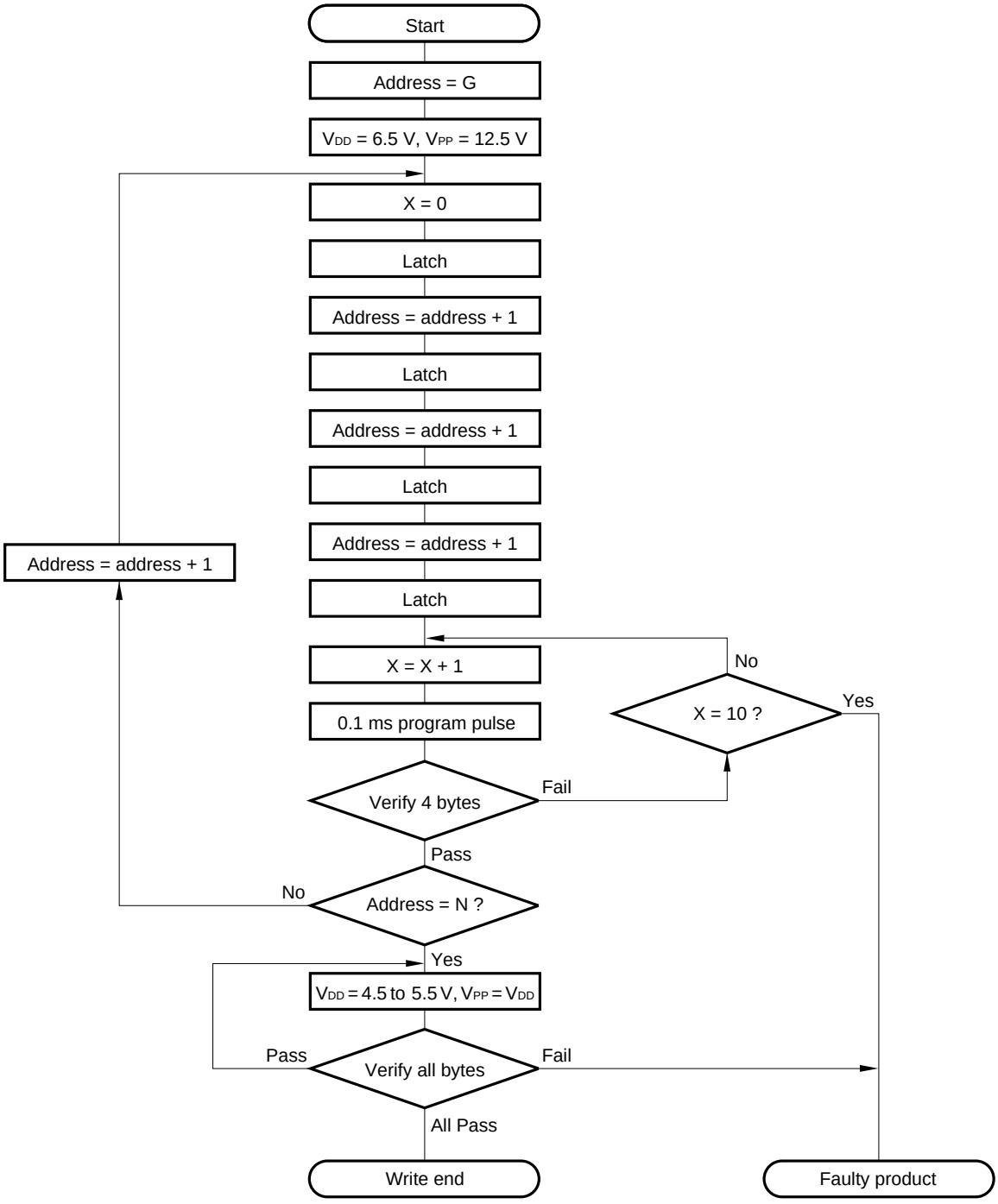
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P048As are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flow Chart



G = Start address

N = Program last address

Figure 5-2. Page Program Mode Timing

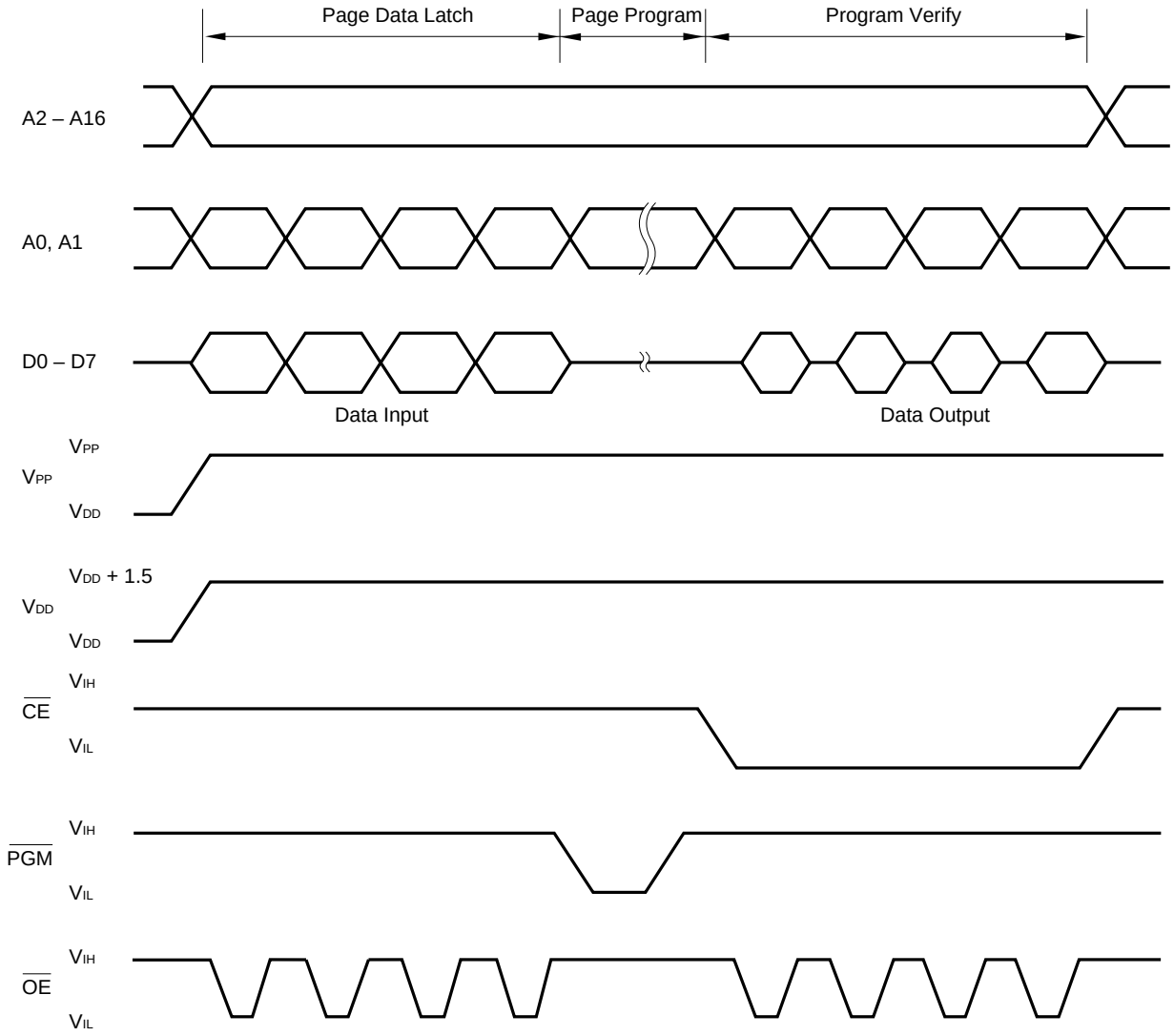
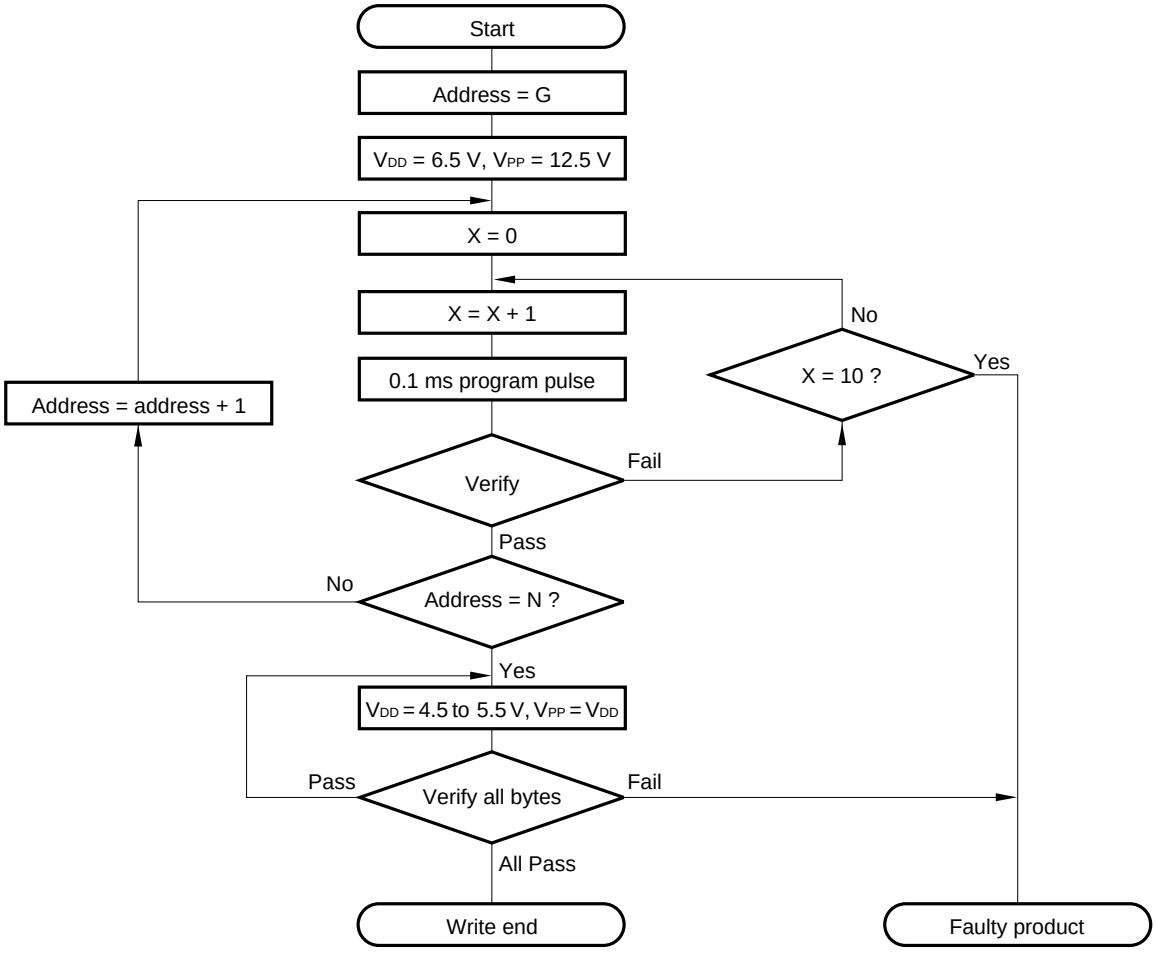


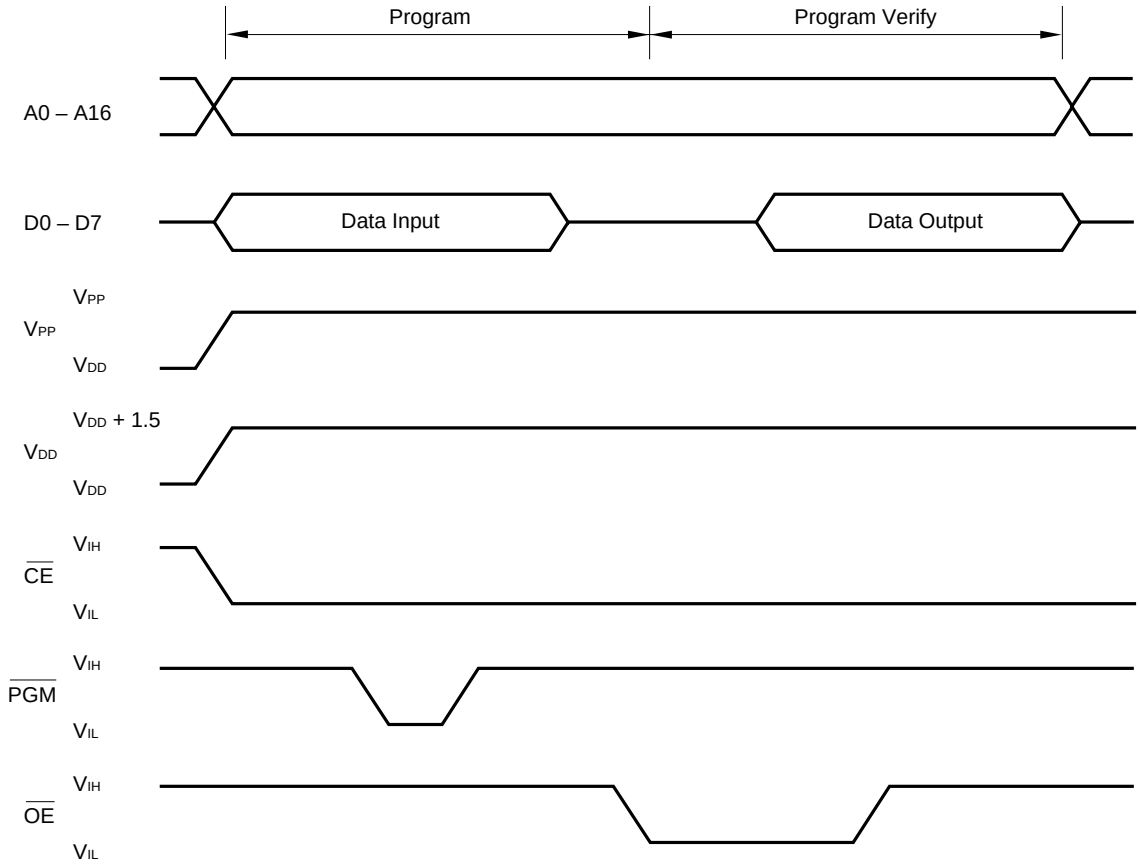
Figure 5-3. Byte Program Mode Flow Chart



G = Start address

N = Program last address

Figure 5-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **PIN CONFIGURATION (2) PROM programming mode**.

(2) Supply +5 V to the V_{DD} and V_{PP} pins.

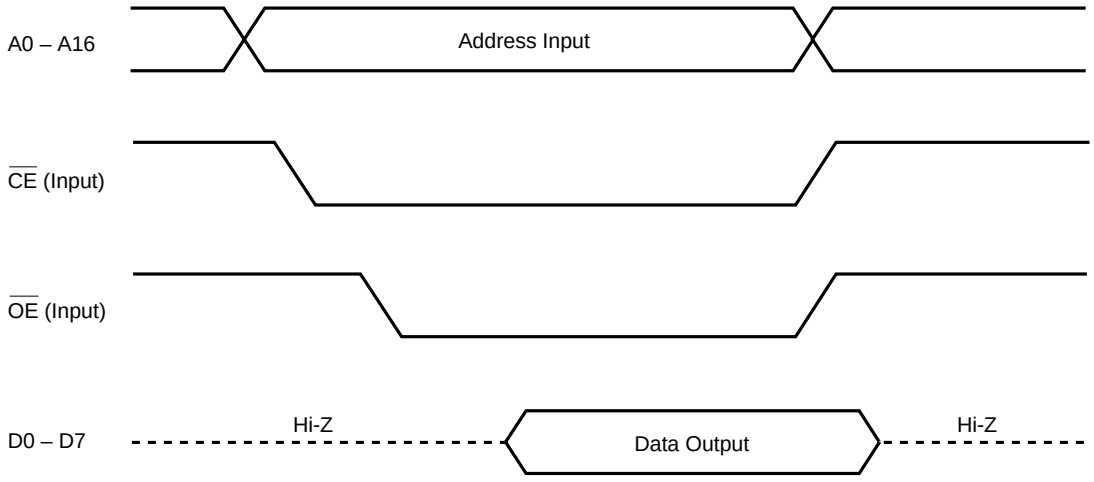
(3) Input address of read data into the A0 to A16 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

Figure 5-5. PROM Read Timings



6. ERASURE METHOD (μPD78P048AKL-S ONLY)

The μPD78P048AKL-S is capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the contents of data, irradiate light having a wavelength of less than about 400 nm to the erasing window. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of irradiation required to completely erase the contents of data is as follows:

★ • UV intensity × erasing time: 30 W•s/cm^2 or more

★ • Erasing time: 40 minutes (MIN.) (When a UV lamp of 12,000 μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

7. ERASURE WINDOW SEAL (μPD78P048AKL-S ONLY)

To protect from miserasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, stick a protection seal on the erasure window when EPROM contents erasure is not performed.

8. ONE-TIME PROM PRODUCTS SCREENING

The one-time PROM product (μPD78P048AGF-3B9) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

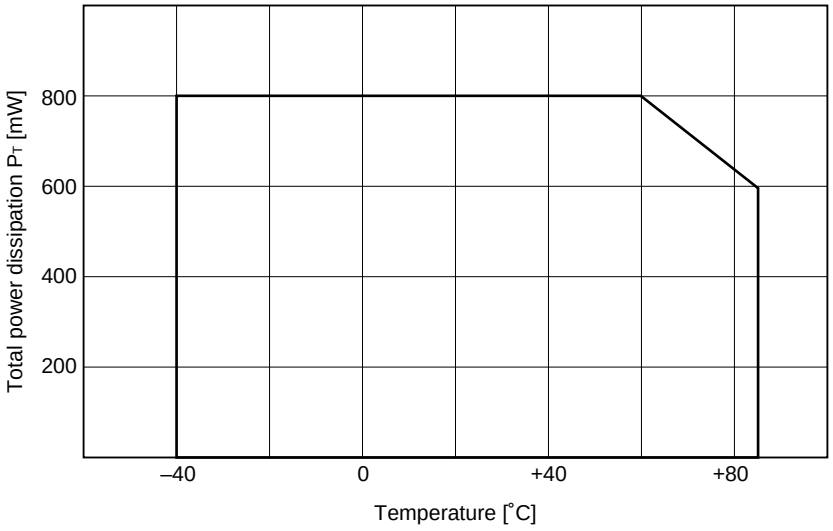
Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{LOAD}			V_{DD} –40 to V_{DD} +0.3	V
	V_{PP}			–0.3 to 13.5	V
	AV_{DD}			–0.3 to V_{DD} +0.3	V
	AV_{REF}			–0.3 to V_{DD} +0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P04, P10 to P17, P20 to P27, P30 to P37, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} +0.3	V
	V_{I2}	P70-P74	N-ch open drain	–0.3 to +16	V
	V_{I3}	P110 to P117, P120 to P127	P-ch open drain	V_{DD} –40 to V_{DD} +0.3	V
Output voltage	V_{O1}	P01 to P03, P10 to P17, P20 to P27, P30 to P37		–0.3 to V_{DD} +0.3	V
	V_{O2}	P70 to P74		–0.3 to +16	V
	V_{OD}	P80, P81, P90 to P97, P100 to P107, P110 to P117, P120 to P127		V_{DD} –40 to V_{DD} +0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI7	Analog input pins	AV_{SS} –0.3 to AV_{REF0} +0.3	V
High-level output current	I_{OH}	1 pin of P01 to P03, P10 to P17, P20 to P27, P30 to P37		–10	mA
		Total for P01 to P03, P10 to P17, P0 to P27, P30 to P37		–30	mA
		1 pin of P80, P81, P90 to P97, P100 to P107, P110 to P117, P120 to P127		–30	mA
		Total for P80, P81, P90 to P97, P100 to P107, P110 to P117, P120 to P127		–120	mA
Low-level output current	I_{OL} **Note 1**	1 pin of P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74	Peak value	30	mA
			rms	15	mA
		Total for P01 to P03, P10 to P17, P20 to P27, P30 to P37	Peak value	50	mA
			rms	20	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			rms	60	mA
		Total for P70 to P74	Peak value	100	mA
			rms	60	mA
Total power dissipation	P_T **Note 2**	T_A = –40 to +60 °C		800	mW
		T_A = +85 °C		600	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

Notes 1. The rms should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

Notes 2. Total power dissipation differs depending on the temperature (refer to the following figure).



How to calculate total power dissipation

The following three power dissipation are available for the μPD78P048A. The sum of the three power dissipation should be less than the total power dissipation P_T (80 % or less of ratings is recommended).

<1> CPU power dissipation: calculate V_{DD} (MAX.) × I_{DD} (MAX.).
<2> Output pin power dissipation: Power dissipation when maximum current flows into display output pin.
<3> Pull-down resistor power dissipation: Power dissipation by pull-down resistor incorporated in display output pin by mask option.

The following is how to calculate total power dissipation for the example in Figure 9-1.

★ **Example** Assume the following conditions:

V_{DD} = 5 V ± 10 %, 5.0 MHz oscillator
Supply current (I_{DD}) = 21.6 mA
Display output: 11 grids × 10 segments (Cut width = 1/16)
Maximum current at the grid pin is 15 mA.
Maximum current at the segment pin is 3 mA.
At the key scan timing, display output pin is OFF.
Display output voltage: grid $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
segments $V_{OD} = V_{DD} – 0.4$ V (voltage drop of 0.4 V)
Fluorescent display control voltage (V_{LOAD}) = –30 V
Mask option pull-down resistor = 25 kΩ

By placing the above conditions in calculation <1> to <3>, the total dissipation can be worked out.

<1> CPU power dissipation: 5.5 V × 21.6 mA = 118.8 mW

<2> Output pin power dissipation:

Grid $(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{The number of grids + 1}} \times \text{Digit width (1 – Cut width)}$

$= 2\ V \times \frac{15\ mA \times 11\ Grids}{11\ Grids + 1} \times (1 - \frac{1}{16}) = 25.8\ mW$

Segment $(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{The number of grids +1}}$

$= 0.4\ V \times \frac{3\ mA \times 31\ Dots}{11\ Grids + 1} = 3.1\ mW$

<3> Pull-down resistor power dissipation:

Grid $\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{The number of grids}}{\text{The number of grids + 1}} \times \text{Digit width}$

$= \frac{(5.5\ V - 2\ V - (-30\ V))^2}{25\ k\Omega} \times \frac{11\ Grids}{11\ Grids + 1} \times (1 - \frac{1}{16}) = 38.6\ mW$

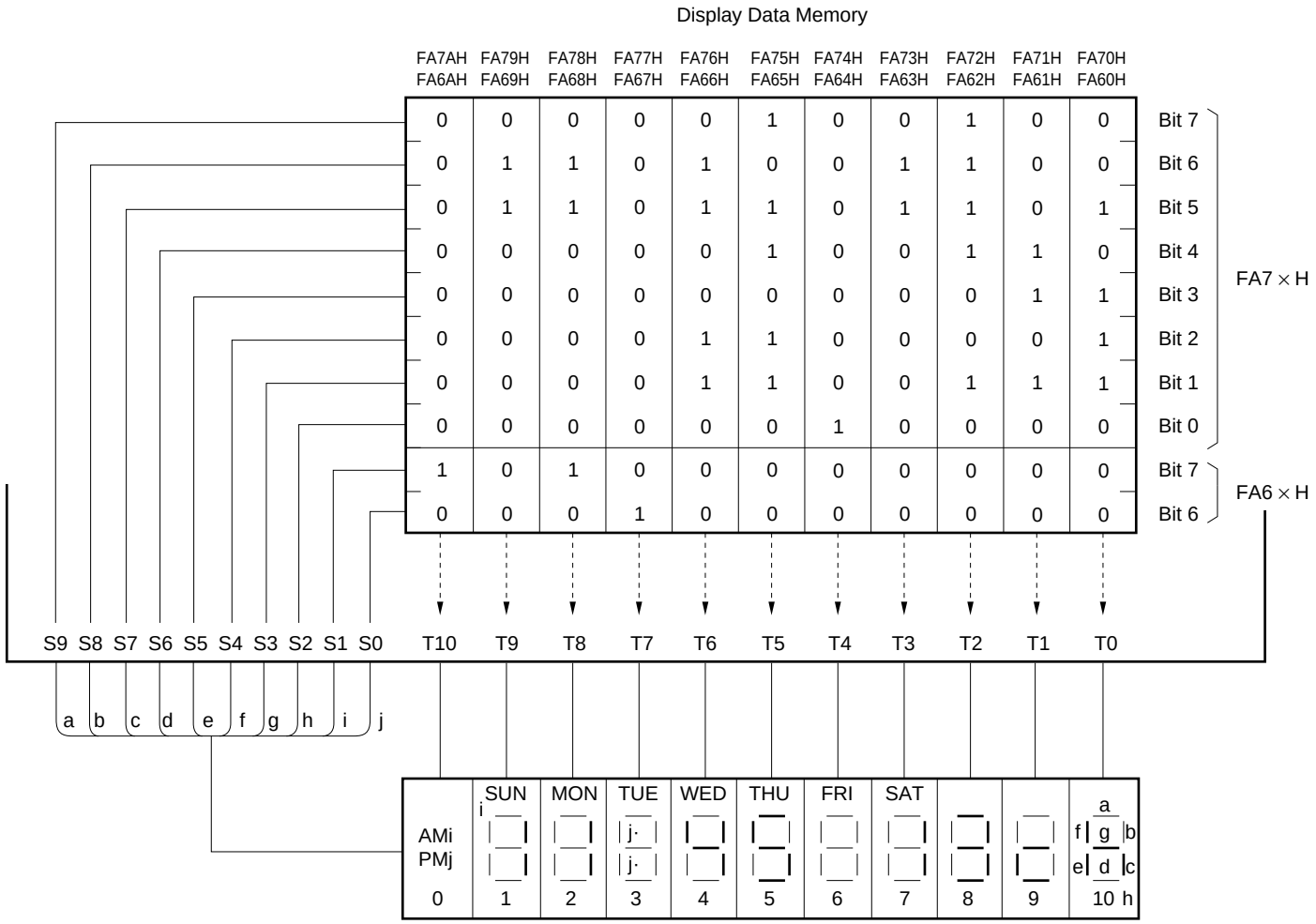
Segment $\frac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{The number of illuminated dots}}{\text{The number of grids + 1}}$

$= \frac{(5.5\ V - 0.4\ V - (-30\ V))^2}{25\ k\Omega} \times \frac{31\ dots}{11\ Grids + 1} = 127.3\ mW$

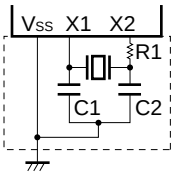
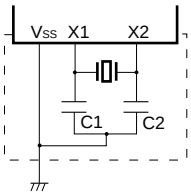
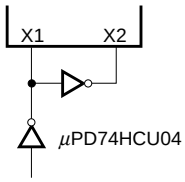
Total power dissipation = <1> + <2> + <3> = 118.8 + 25.8 + 3.1 + 38.6 + 127.3 = 313.6 mW

In this example, the total power dissipation do not exceed the rating of the total power dissipation shown in the figure above, so there is no problem in power dissipation.
However, when the total power dissipation exceeds the rating of the total power dissipation, it is necessary to lower the power dissipation. To reduce power dissipation, reduce the number of pull-down resistor.

Figure 9-1. Display Example of 10 Segments-11 Digits



Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)**Note 1**		1		5	MHz
		Oscillator stabilization time**Note 2**				4	ms
Crystal resonator		Oscillator frequency (f_X)**Note 1**		1	4.19	5	MHz
		Oscillator stabilization time**Note 2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. Refer to **AC characteristics** for instruction execution times.

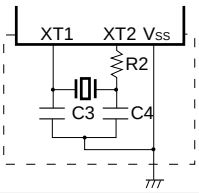
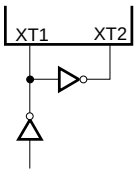
2. This is the time required for oscillation to stabilize after addition of V_{DD}, or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Osillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

	Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
	Crystal resonator		Oscillator frequency (f_{XT})**Note1**		32	32.768	35	kHz
			Oscillator stabilization time**Note2**	V_{DD} = 4.5 to 6.0 V		1.2	2	s
							10	
★	External clock		XT1 input frequency (f_{XT})**Note1**		32		100	kHz
★			XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. Refer to **AC characteristics** for instruction execution times.

2. This is the time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main system clock: ceramic resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency	Circuit Constant			Oscillator Voltage Range		Remark
		(MHz)	C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	5.6	2.8	6.0	
	CSA2.00MG	2.00			—	2.9		
	CST2.00MG	2.00	—	—				Built-in capacitor
	CSA×.××MG	3.00 to 5.00	30	30		2.8		
	CST×.××MGW	3.00 to 5.00	—	—				Built-in capacitor
Matsushita Electronics Components Co., Lltd.	EFOGC2004A4	2.00				2.7		Built-in capacitor
	EFOEC3004A4	3.00						Built-in capacitor
	EFOEC4004A4	4.00						Built-in capacitor
	EFOEC4194A4	4.19						Built-in capacitor
	EFOGC5004A4	5.00						Built-in capacitor
TDK Corp.	FCR2.0MC3	2.00						Built-in capacitor
	FCR4.0MC5	4.00						Built-in capacitor
	OCR4.0MC3**Note**	4.00						Built-in capacitor
	CCR5.0MC5**Note**	5.00						Built-in capacitor

Note Surface-mount type

Remark ×.×× indicates frequencies.

Subsystem clock: crystal resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency	Circuit Constant			Oscillator Voltage Range	
		(kHz)	C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Kyocera Corp.	KF-38G**Note** (Load capacitance 12 pF)	32.768	15	22	220	2.7	6.0

Note Maintained product.

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation. However, they do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator that being used.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V				35	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37			15	pF
			P70 to P74			20	pF
			P110 to P117, P120 to P127			35	pF

Remark Unless otherwise specified, the characteristics of the shared pin are the same as the characteristics of the port pin.

Operating power supply voltage (T_A = –40 to +85 °C)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
CPU[Note 1]		2.7[Note 2]		6.0	V
Display controller		4.5		6.0	V
PWM mode of 16-bit time/event counter (TM0)		4.5		6.0	V
A/D converter		4.0		6.0	V
Other hardware		2.7		6.0	V

Notes 1. Except for system clock oscillator, display controller/driver, and PWM.

2. Operating power supply voltage differs depending on the cycle time. Refer to **AC Characteristics**.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P21, P23		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P70 to P74	N-ch open-drain	0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	V_{DD} = 4.5 to 6.0 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.3		V_{DD}	V
	V_{IH6}	P10 to P17, P30 to P32,	V_{DD} = 4.5 to 6.0 V	0.65 V_{DD}		V_{DD}	V
		P35 to P37		0.7 V_{DD}		V_{DD}	V
	V_{IH7}	P110 to P117, P120 to P127	V_{DD} = 4.5 to 6.0 V	0.7 V_{DD}		V_{DD}	V
				V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P21, P23		0		0.3 V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	P70 to P74	V_{DD} = 4.5 to 6.0 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2	V_{DD} = 4.5 to 6.0 V	0		0.4	V
				0		0.3	V
	V_{IL6}	P10 to P17, P30 to P32, P35 to P37	V_{DD} = 4.5 to 6.0 V	0		0.3 V_{DD}	V
	V_{IL7}	P110 to P117, P120 to P127		V_{DD} – 3.5		0.3 V_{DD}	V
High-level output voltage	V_{OH}	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P80, P81, P90 to P97, P100 to P107, P110 to P117, P120 to P127	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			I_{OH} = –100 μA	V_{DD} – 0.5			V
Low-level output voltage	V_{OL1}	P30 to P37, P70 to P74	V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27	V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 6.0 V With open-drain and pull-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74	I_{OL} = 400 μA			0.5	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	P00 to P03, P10 to P17, P20 to P27, P30 to P37, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
★	I_{LIH3}	V_{IN} = 15 V	P70 to P74			20	μA
	I_{LIH4}	P110 to P117, P120 to P127	V_{DD} = 4.5 to 6.0 V			3 Note 1	μA
		V_{IN} = V_{DD}				3 Note 2	μA

★ **Notes 1.** For P110 to P117 and P120 to P127, a high-level input leak current of 150 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed to read out ports 11, 12 (P11, 12) or port mode registers 11, 12 (PM11, 12). Outside the period of 1.5 clocks following executing a read-out instruction, the current is 3 μA (MAX.).

★ **2.** For P110 to P117 and P120 to P127, a high-level input leak current of 90 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed to read out P11, P12, PM11, and PM12. Outside the period of 1.5 clocks following executing a read-out instruction, the current is 3 μA (MAX.).

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, $\overline{\text{RESET}}$			–3	μA
		I_{LIL2}		X1, X2, XT1/P04 XT2			–20	μA
		I_{LIL3}		P70 to P74			–3 Note 4	μA
		I_{LIL4}		P110 to P117, P120 to P127			–10	μA
	High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P80, P81, P90 to P97, P100 to P107, P110 to P117, P120 to P127			3	μA
★		I_{LOH2}	V_{OUT} = 15 V	P70 to P74			20	μA
	Low-level output leakage current	I_{LOL1}	V_{OUT} = 0 V	P01 to P03, P10 to P17, P10 to P27, P30 to P37, P70 to P74			–3	μA
		I_{LOL2}	V_{OUT} = V_{LOAD} = V_{DD} – 35 V	P80, P81, P90 to P97, P100 to 107, P110 to P117, P120 to P127			–10	μA
★	Display output current	I_{OD}	V_{DD} = 4.5 to 6.0 V, V_{OD} = V_{DD} – 2 V		–15	–25		mA
	Software pull-up resistor	R_1	V_{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37	V_{DD} = 4.5 to 6.0 V	15	40	90	kΩ
					20		500	kΩ
	On-chip pull-down resistor	R_2	P80, P81, P90 to P97, P100 to P105	V_{OD} – V_{LOAD} = 35 V	25	70	135	kΩ
★	Power supply current Note 1	I_{DD1}	5.0 MHz crystal oscillation operation mode	V_{DD} = 5.0 V ± 10 % Note 2		9.5	28.5	mA
★						9.75 Note 5	29 Note 5	mA
				V_{DD} = 3.0 V ± 10 % Note 3		0.9	2.7	mA
★		I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		2.5	7.5	mA
★				V_{DD} = 3.0 V ± 10 %		1.0	3.0	mA
★		I_{DD3}	32.768 kHz crystal oscillation operation mode	V_{DD} = 5.0 V ± 10 %		90	180	μA
				V_{DD} = 3.0 V ± 10 %		55	110	μA
		I_{DD4}	32.768 kHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		25	50	μA
				V_{DD} = 3.0 V ± 10 %		5	10	μA
		I_{DD5}	XT1 = 0 V STOP mode when connecting to feedback resistor	V_{DD} = 5.0 V ± 10 %		1	20	μA
				V_{DD} = 3.0 V ± 10 %		0.5	10	μA
		I_{DD6}	XT1 = 0 V STOP mode when not connecting to feedback resistor	V_{DD} = 5.0 V ± 10 %		0.1	20	μA
				V_{DD} = 3.0 V ± 10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the built-in pull-down resistor.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when the PCC is set to 04H)

4. For P70 to P74, a low-level input leak current of –150 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed to read out port 7 (P7) or port mode register 7 (PM7). Outside the period ★ of 1.5 clocks following executing a read-out instruction, the current is –3 μA (MAX.).

★ **5.** This current includes the AV_{DD} current by the A/D converter operation.

Remark Unless otherwise specified, the characteritics of a shared pin are the same as those of a port pin.

AC Characteristics

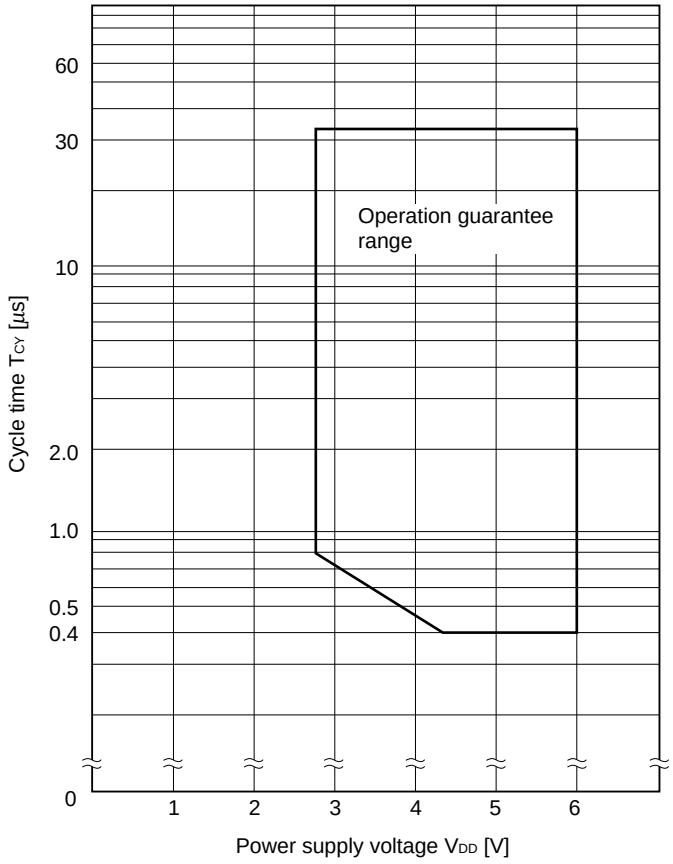
(1) Basic operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum) instruction execution time)	T_{CY}	Operated with main system clock	V_{DD} = 4.5 to 6.0 V	0.4		32	μs
				0.8		32	μs
★		Operated with subsystem clock		40 Note 1	122	125	μs
TI1, 2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		2	MHz
				0		138	kHz
TI1, 2 input high, low-level width	f_{TIH}	V_{DD} = 4.5 to 6.0 V		250			ns
	f_{TIL}			3.6			μs
Interrupt input high, low-level width	f_{INTH}	INTP0		$8/f_{sam}$ Note 2			μs
	f_{INTL}	INTP1 to INTP3		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when external clock input is used as subsystem clock. When crystal is used, the value becomes 114 μs.

2. Selection of $f_{sam} = fx/2^{N+1}$, fx/64, fx/128 is available (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of sampling clock select register (SCS).

T_{CY} vs V_{DD} (with main system clock operated)



(2) Serial interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2 - 50$			ns
	t_{KL1}			$t_{KCY1}/2 - 150$			ns
SI0 setup time to $\overline{SCK0}\uparrow$	t_{SIK1}			100			ns
SI0 hold time from $\overline{SCK0}\uparrow$	t_{KSI1}			400			ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 output delay time	t_{KSO1}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

Note C is a load capacitance of the $\overline{SCK0}$ or SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL2}			1600			ns
SI0 setup time to $\overline{SCK0}\uparrow$	t_{SIK2}			100			ns
SI0 hold time from $\overline{SCK0}\uparrow$	t_{KSI2}			400			ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 output delay time	t_{KSO2}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{SCK0}$ rise, fall time	t_{R2} t_{F2}					160	ns

Note C is a load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2 - 50$			ns
	t_{KL3}			$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time to $\overline{SCK}\uparrow$	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}\uparrow$	t_{KSI3}			$t_{KCY3}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$ SB0, SB1 output delay time	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
$\overline{SCK0}\uparrow\rightarrow$SB0, SB1$\downarrow$	t_{KSB}			t_{KCY3}			ns
SB0, SB1$\downarrow\rightarrow\overline{SCK0}\downarrow$	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R is a load resistance of the $\overline{SCK0}$, SB0, or SB1 output line, and C is its load capacitance.

(iv) SBI mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time to $\overline{SCK0}\uparrow$	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}\uparrow$	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$ SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK0}\uparrow\rightarrow$SB0, SB1$\downarrow$	t_{KSB}			t_{KCY4}			ns
SB0, SB1$\downarrow\rightarrow\overline{SCK0}\downarrow$	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	1600			ns
				3800			ns
$\overline{SCK0}$ high-level width	t_{KH5}			$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}			$t_{KCY5}/2 - 50$			ns
SB0, SB1 setup time to $\overline{SCK0}$↑	t_{SIK5}			300			ns
SB0, SB1 hold time from $\overline{SCK0}$↑	t_{KSI5}			600			ns
$\overline{SCK0}$↓→SB0, SB1 output delay time	t_{KSO5}		V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

Note R is a load resistance of the $\overline{SCK0}$, SB0, or SB1 output line, and C is its load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	1600			ns
				3800			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time to $\overline{SCK0}$↑	t_{SIK6}			100			ns
SB0, SB1 hold time from $\overline{SCK0}$↑	t_{KSI6}			$t_{KCY6}/2$			ns
$\overline{SCK0}$↓→SB0, SB1 output delay time	t_{KSO6}		V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH7}	V_{DD} = 4.5 to 6.0 V		$t_{KCY7}/2 - 50$			ns
	t_{KL7}			$t_{KCY7}/2 - 100$			ns
SI1 setup time to $\overline{SCK1}\uparrow$	t_{SIK7}			100			ns
SI1 hold time from $\overline{SCK1}\uparrow$	t_{KSI7}			400			ns
$\overline{SCK1}\downarrow\rightarrow$ SO1 output delay time	t_{KSO7}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

Note C is a load capacitance of the $\overline{SCK1}$ or SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH8}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL8}			1600			ns
SI1 setup time to $\overline{SCK1}\uparrow$	t_{SIK8}			100			ns
SI1 hold time from $\overline{SCK1}\uparrow$	t_{KSI8}			400			ns
$\overline{SCK1}\downarrow\rightarrow$ SO1 output delay time	t_{KSO8}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{SCK1}$ rise, fall time	t_{R8} t_{F8}					160	ns

Note C is a load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH9}	V_{DD} = 4.5 to 6.0 V		$t_{KCY9}/2 - 50$			ns
	t_{KL9}			$t_{KCY9}/2 - 150$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}			100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}			400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO9}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
STB$\uparrow$ from $\overline{SCK1}\downarrow$	t_{SBD}			$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}			$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
B signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (from busy signal detection timing	t_{BYH}			100			ns
$\overline{SCK1}\downarrow$ from busy inactibe	t_{SPS}					$2t_{KCY9}$	ns

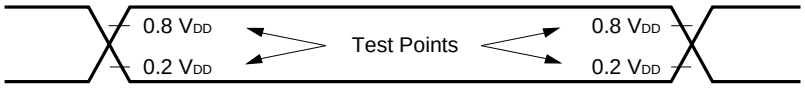
Note R is a load resistance of the $\overline{SCK1}$ or SO1 output line, and C is its load capacitance.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$: External clock input)

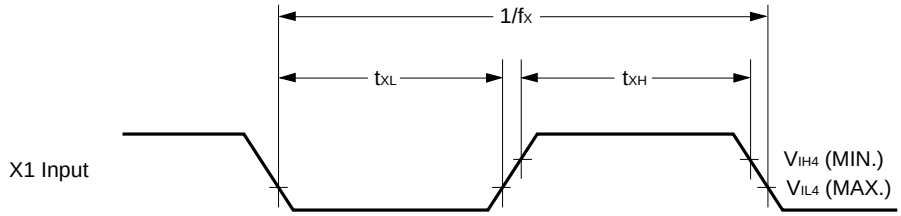
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK1}$ high, low-level width	t_{KH10}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL10}			1600			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}			100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}			400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO10}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{SCK1}$ rise, fall time	t_{R10} t_{F10}					160	ns

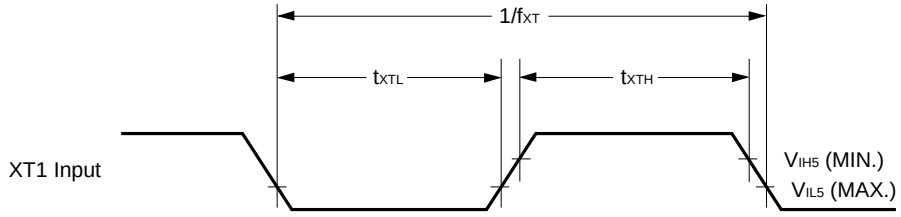
Note C is a load capacitance of the SO1 output line.

AC Timing Test Point (Excluding X1, XT1 Input)

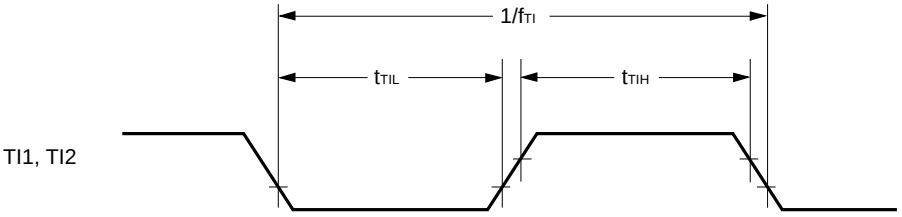


Clock timing



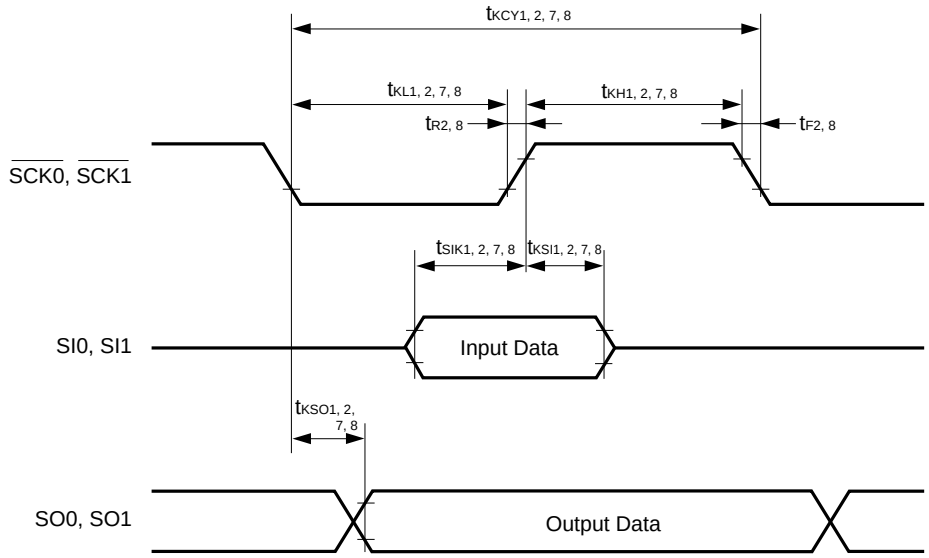


TI timing

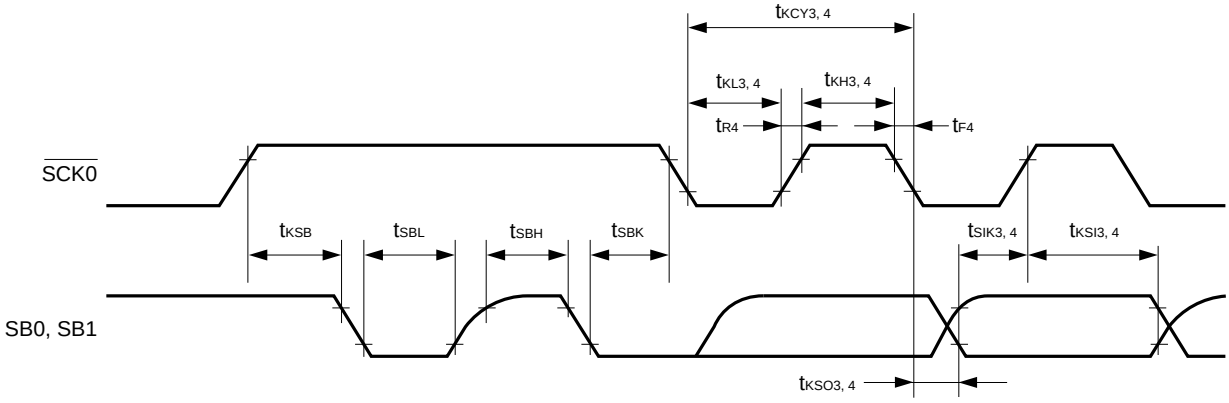


Serial Transfer Timing

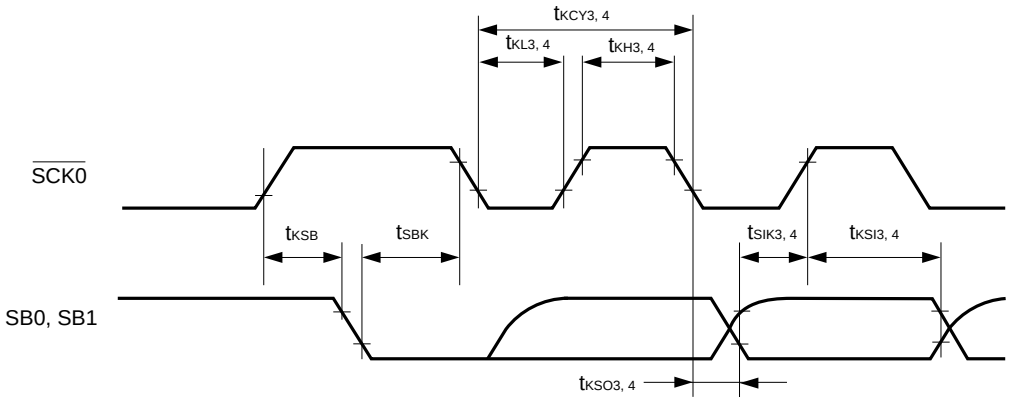
3-wire serial I/O mode:



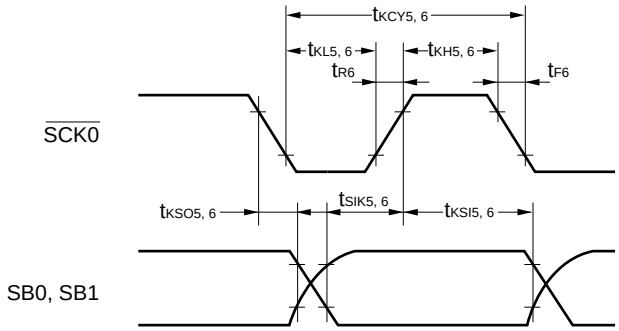
SBI mode (bus release signal transfer):



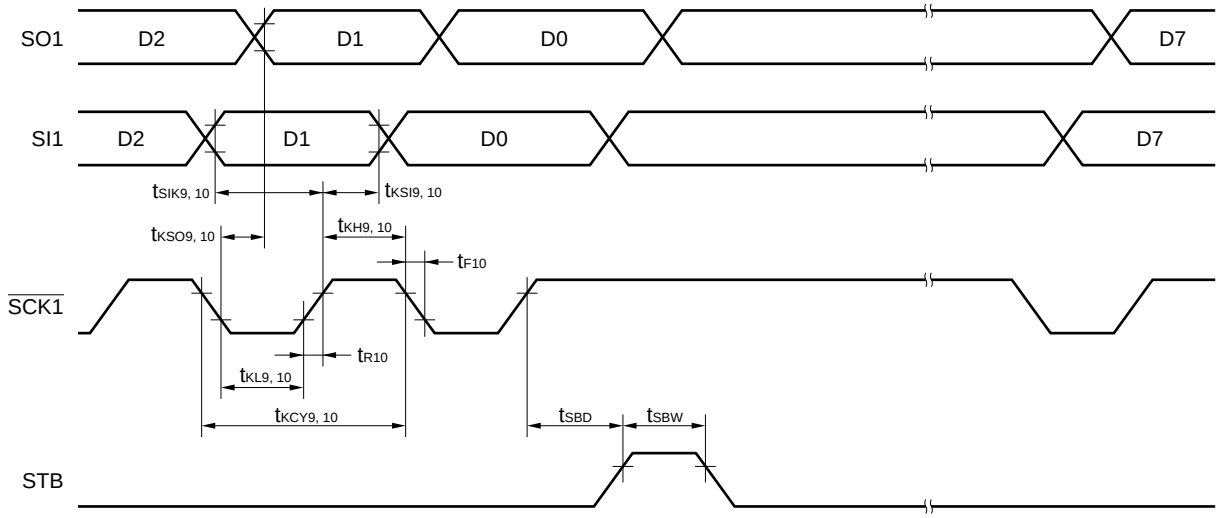
SBI mode (command signal transfer):



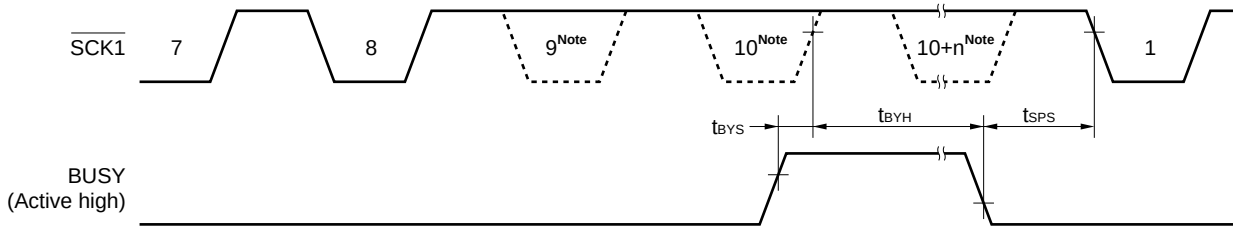
2-wire serail I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (Busy processing):



Note Though it does not become low level actually, heve described as it does due to the timing rule.

A/D Converter Characteristics (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 4.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
★ Total error[Note 1]					0.8	%
Conversion time[Note 2]	t_{CONV}	1 MHz ≤ fx ≤ 5.0 MHz	19.1		200	μs
Sampling time[Note 3]	t_{SAMP}		2.86		30	μs
Analog signal input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.0		AV_{DD}	V
AV_{REF} resistor	R_{AIREF}		4	14		kΩ

Notes 1. Quantization error (+1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

2. Set the A/D conversion time to 19.1 μs or more.

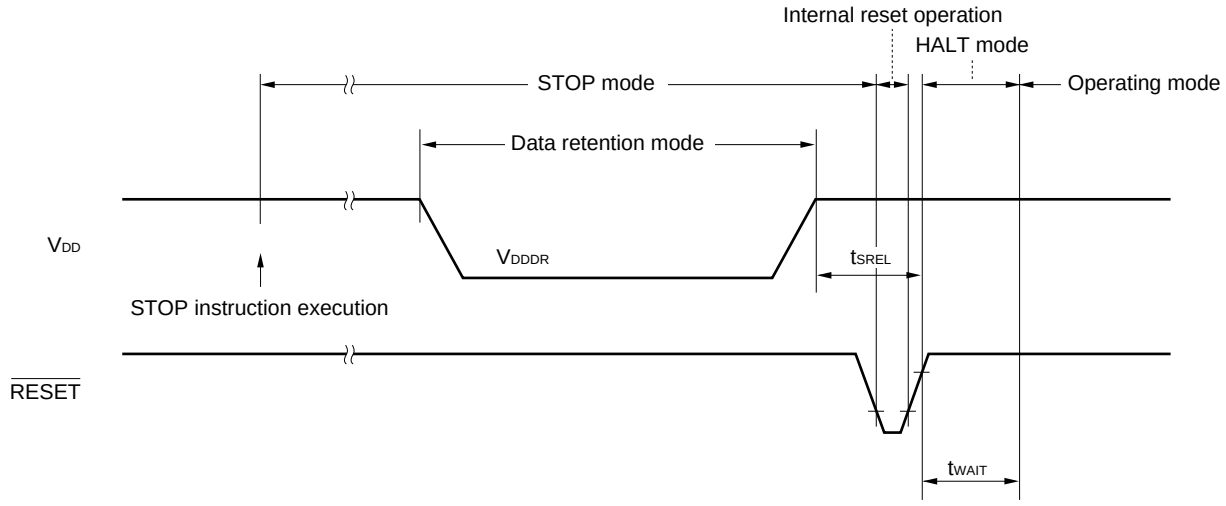
3. Sampling time depends on the conversion time.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

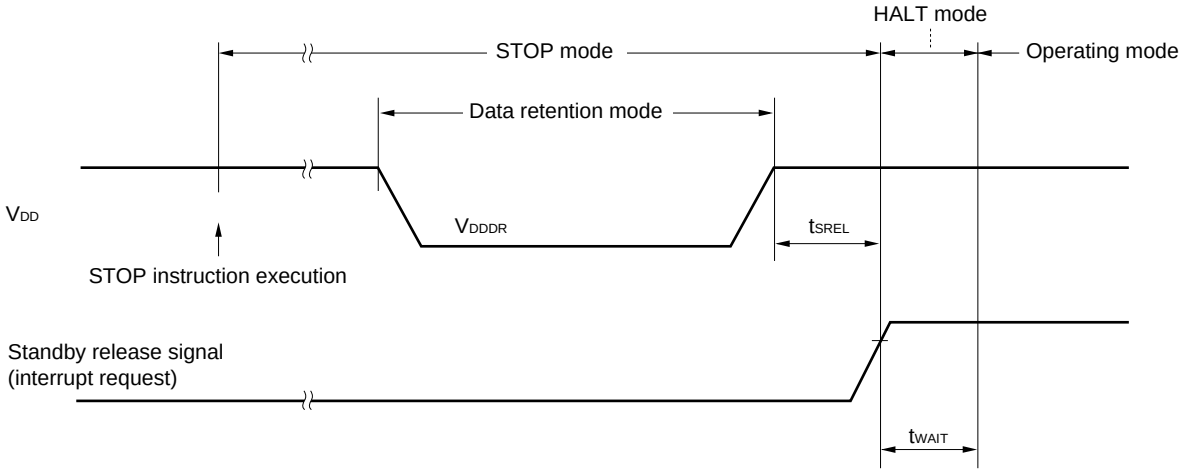
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, Feedback resistor non-connected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		ms
		Release by interrupt		**Note**		ms

Note Selection of 2^{12}/fx, 2^{14}/fx to 2^{17}/fx is available by bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS).

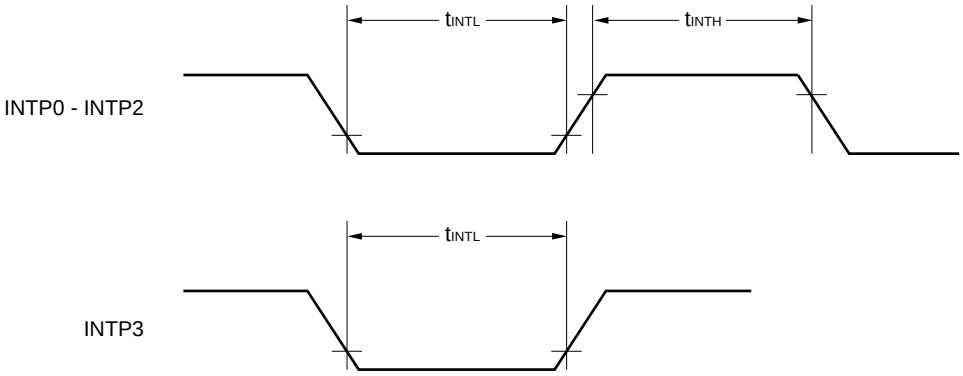
Data retention timing (STOP mode release by $\overline{RESET}$)



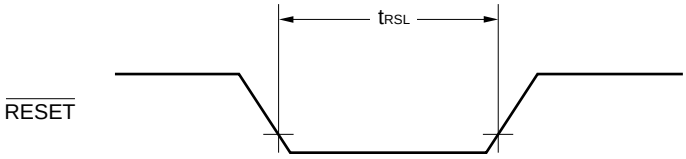
Data retention timing (standby release signal: STOP mode release by interrupt signal)



Interrupt input timing



$\overline{\text{RESET}}$ input timing



PROM Programming Characteristics

DC characteristics

(1) PROM write mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} –1.0			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM read mode (T_A = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} –1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} –0.5			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} –0.6	V_{DD}	V_{DD} +0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding μPD27C1001A symbol.

AC characteristics

(1) PROM write mode

(a) Page program mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AHL}	t_{AHL}		2			μs
Input data hold time (from $\overline{PGM}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM read mode (T_A = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

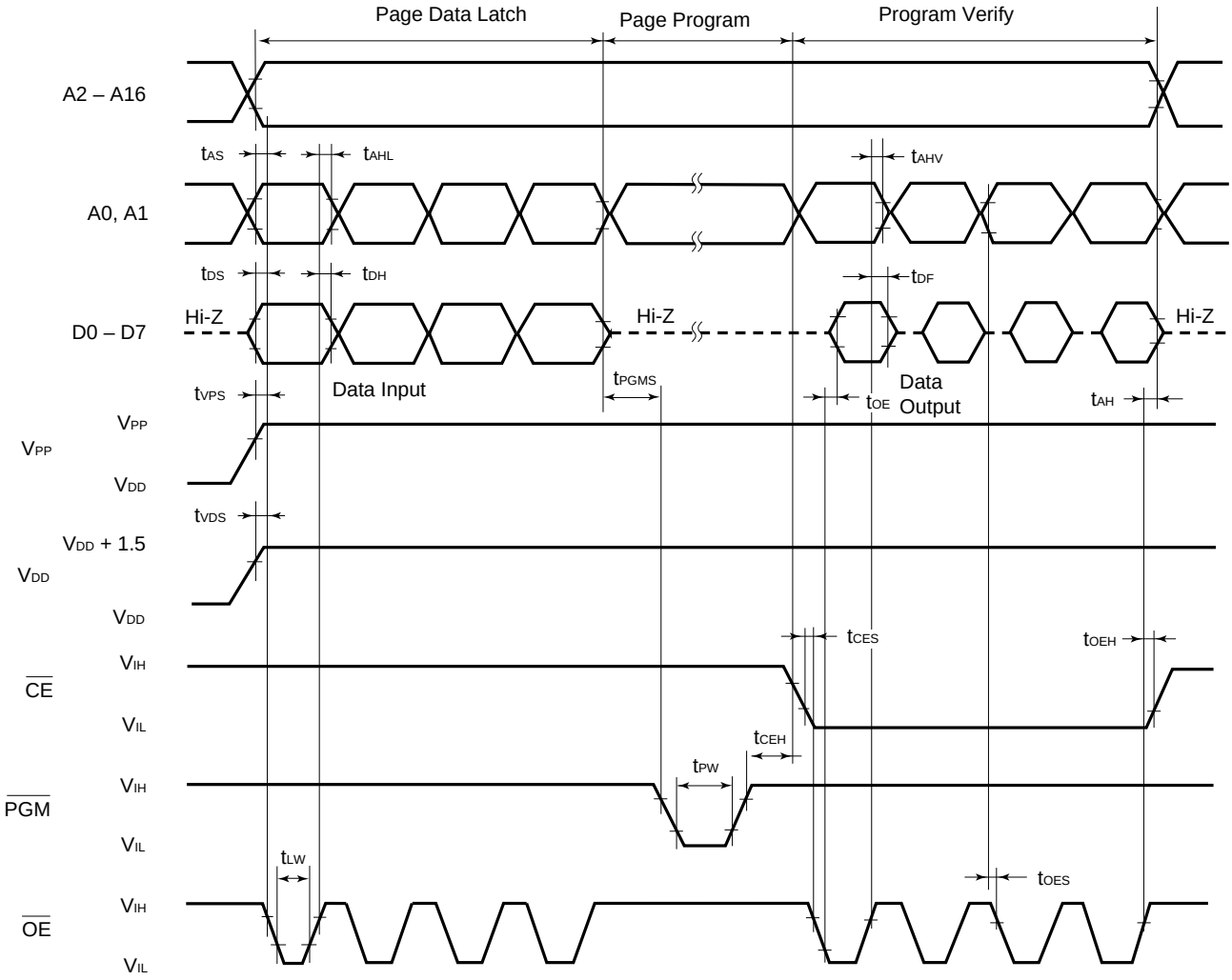
Parameter	Symbol	Symbol[Note]	Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol

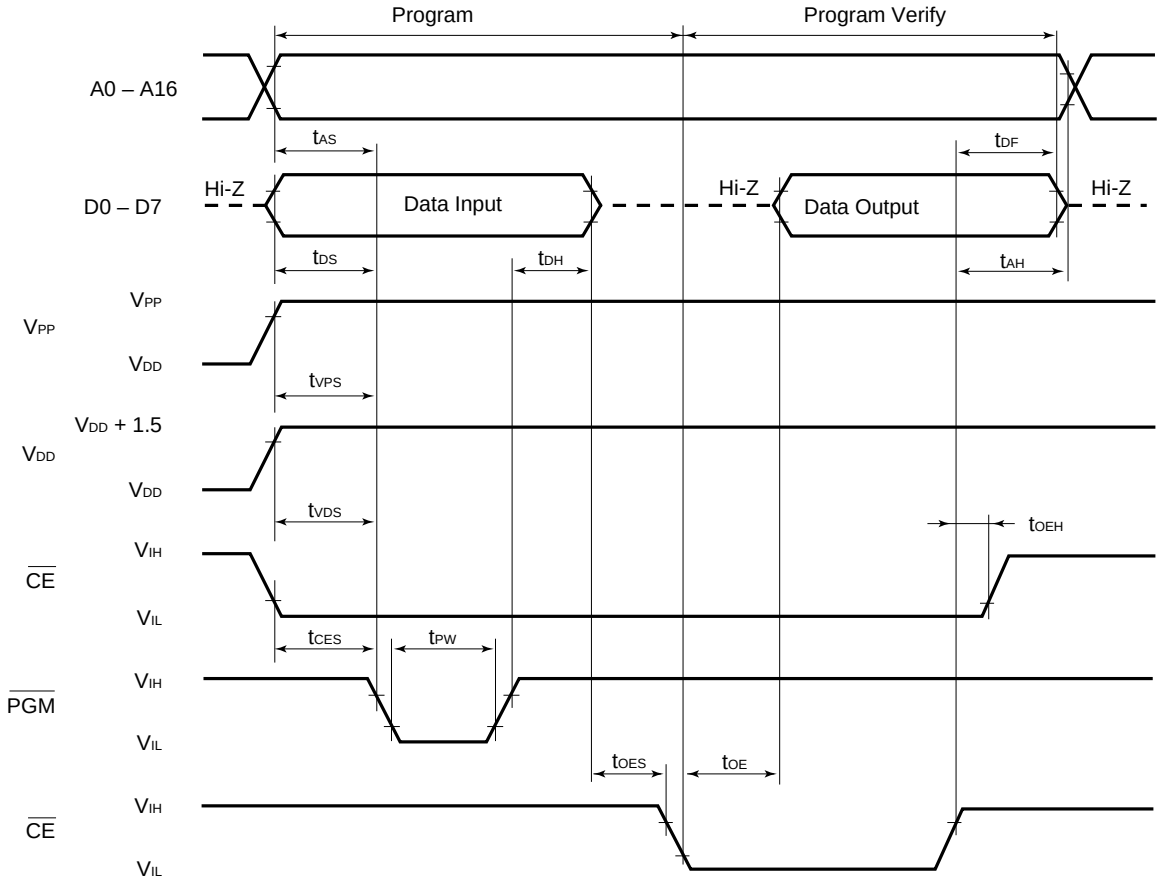
(3) PROM programming mode setting (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM write mode timing (page program mode)



PROM write mode timing (byte program mode)

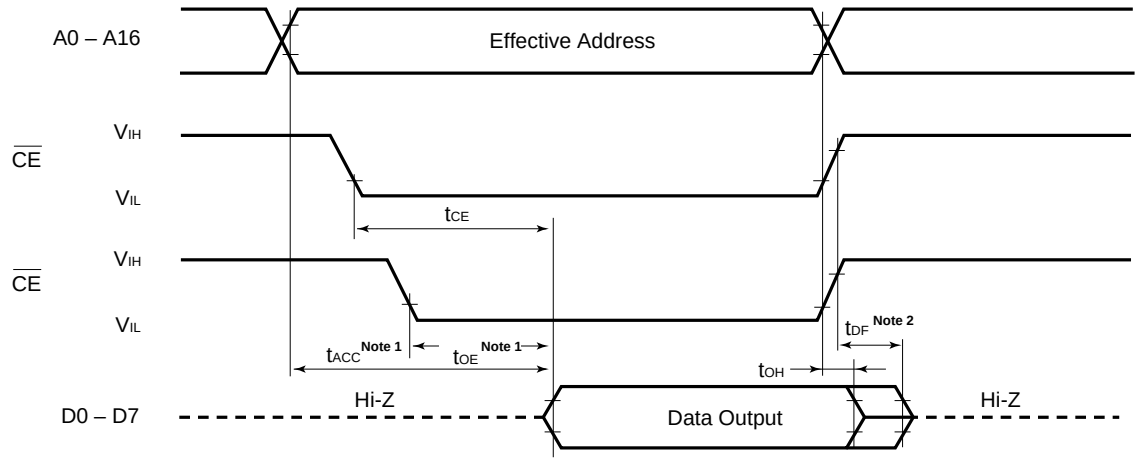


Cautions 1. V_{DD} shonld be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} shonld not exceed +13.5 V including overshoot.

3. Disconnection during application of ±12.5 V to V_{PP} may have an adverse effect on reliability.

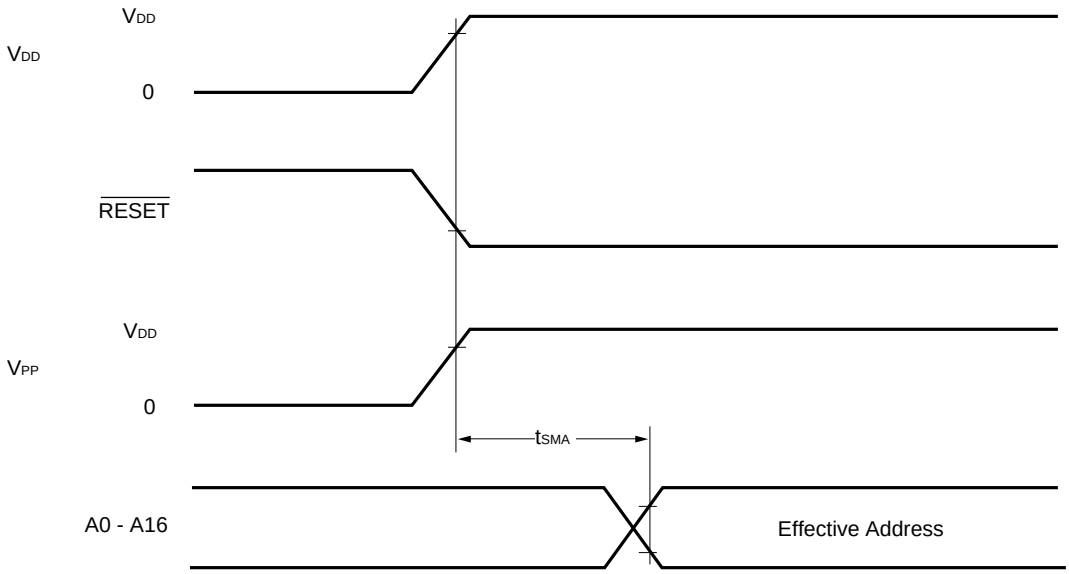
PROM read mode timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of $t_{ACC} - t_{OE}$.

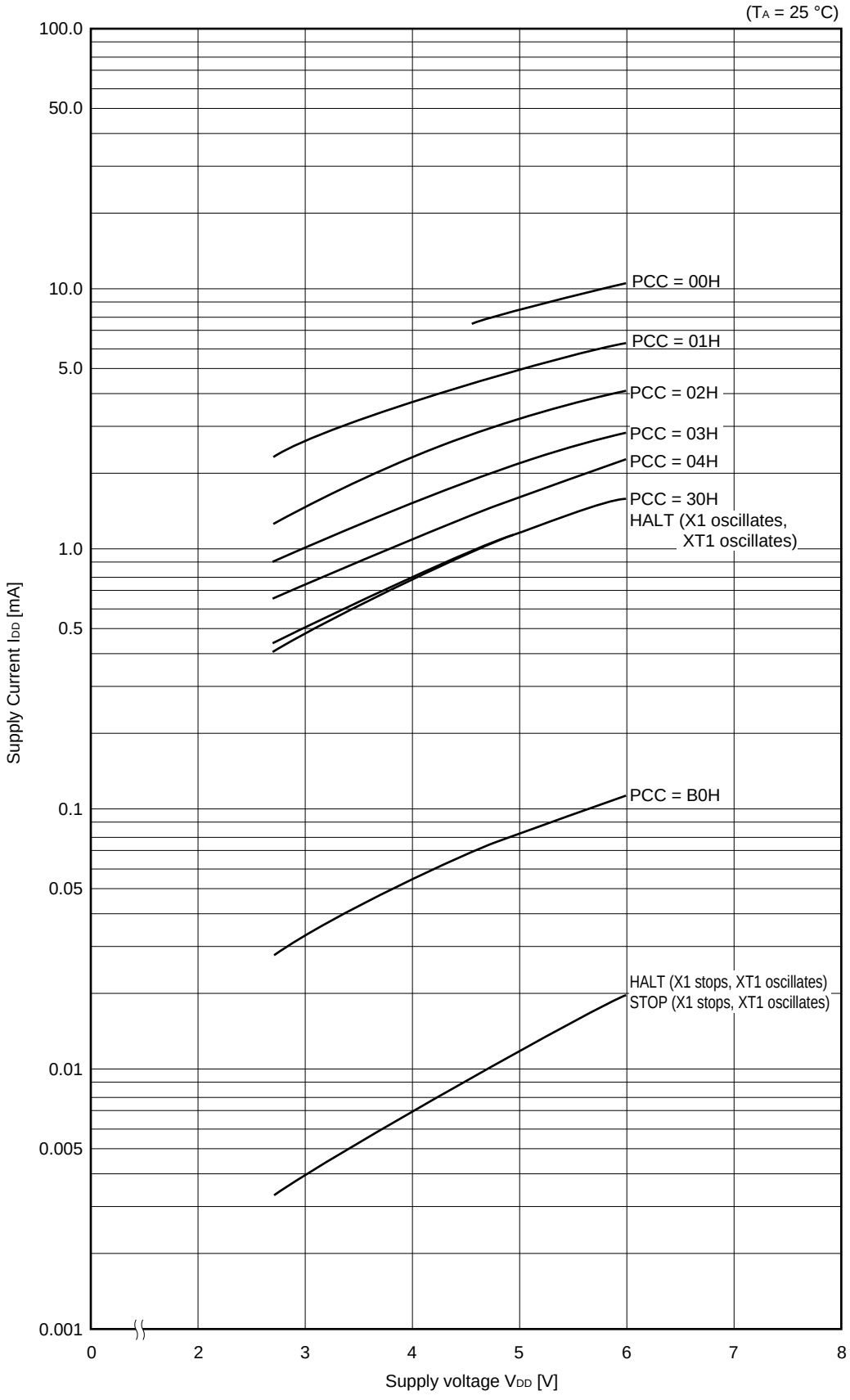
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

PROM programming mode setting timing



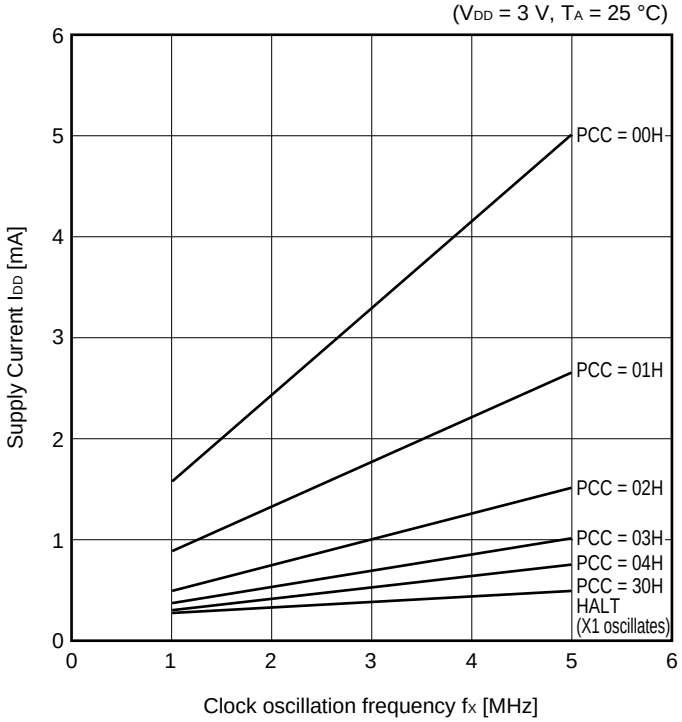
★ 10. CHARACTERISTIC CURVE (REFERENCE VALUE)

I_{DD} vs. V_{DD} (Main system clock : 5.0 MHz)



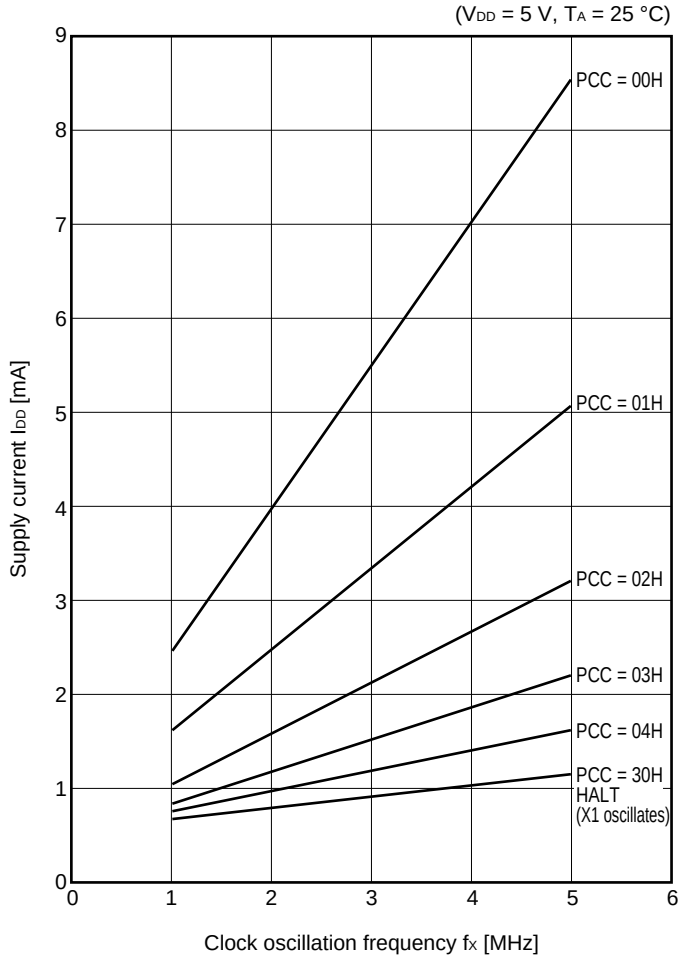
I_{DD} vs. f_X

(V_{DD} = 3 V, T_A = 25 °C)

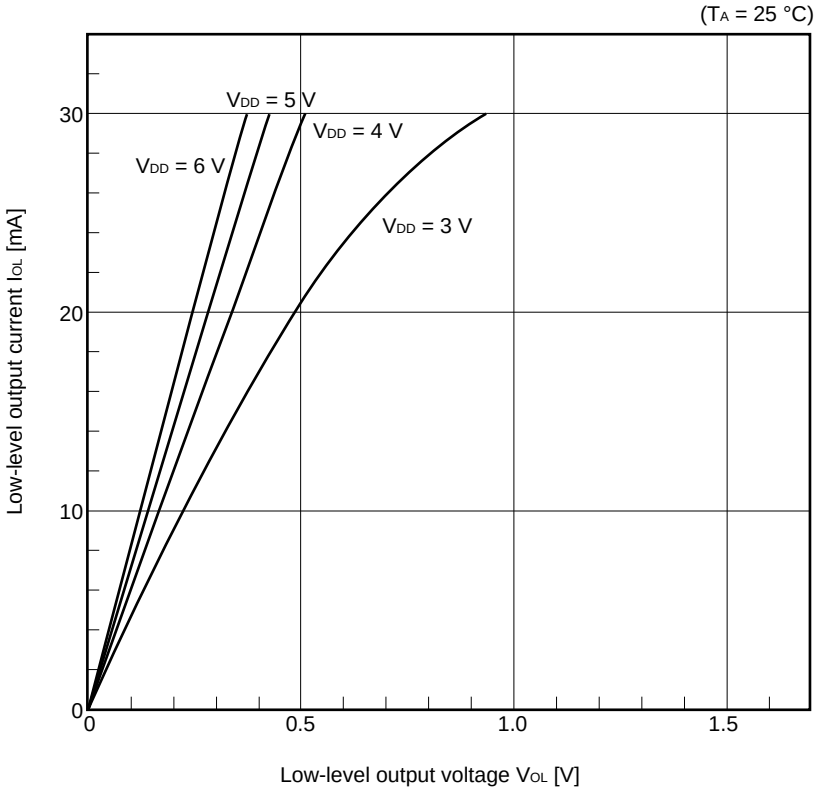


I_{DD} vs. f_X

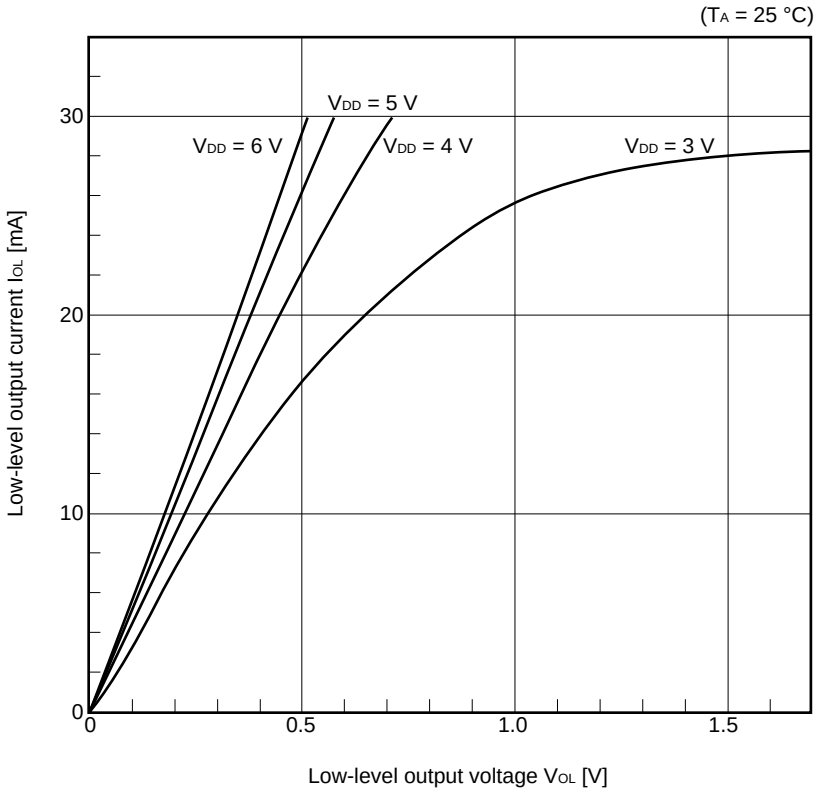
(V_{DD} = 5 V, T_A = 25 °C)



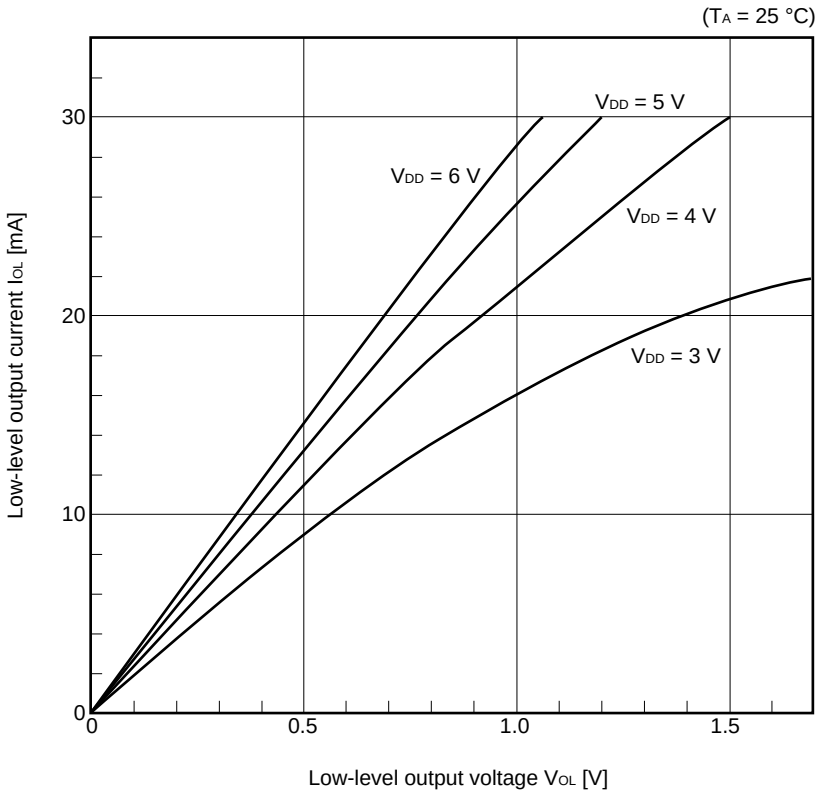
I_{OL} vs. V_{OL} (Port 1)



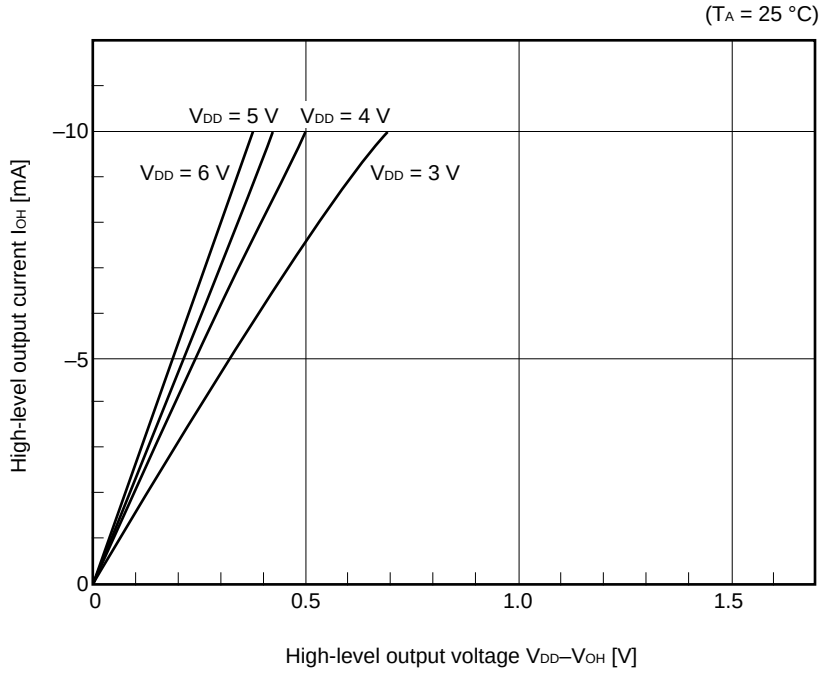
I_{OL} vs. V_{OL} (Ports 0, 2, 3)



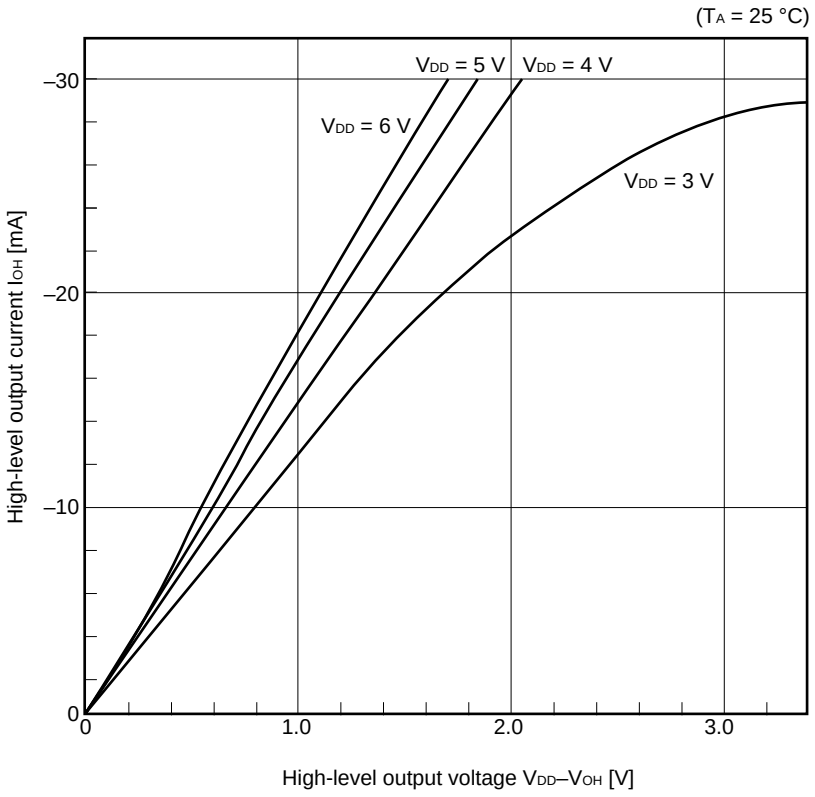
I_{OL} vs. V_{OL} (Port 7)



I_{OH} vs. V_{DD}–V_{OH} (Port 0-Port 3)

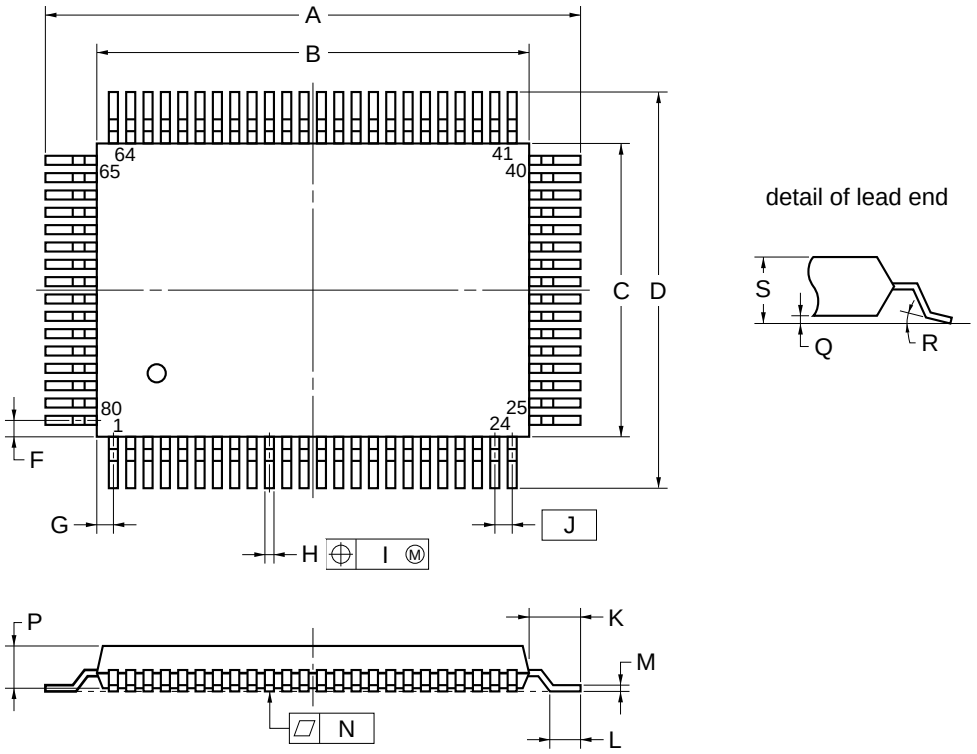


I_{OH} vs. $V_{DD}–V_{OH}$ (Port 8-Port 12)



11. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)



NOTE

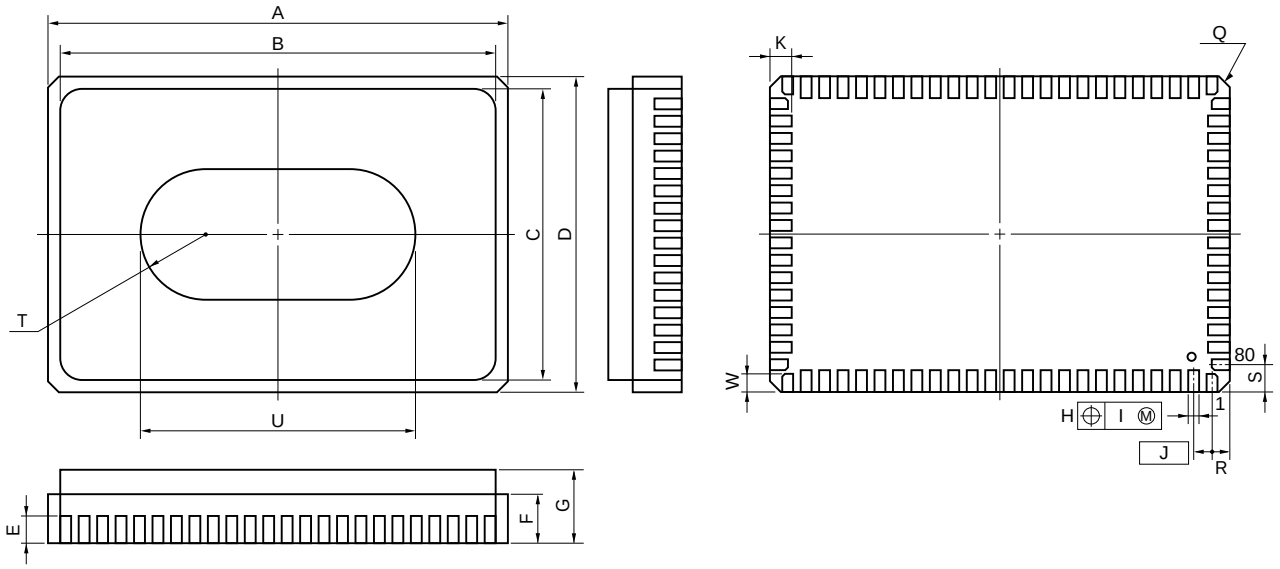
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P80GF-80-3B9-3

Remark Dimensions and materials of ES products are the same as those of mass-production products.

80 PIN CERAMIC WQFN



X80KW-80A-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.2±0.4	0.559±0.016
E	1.64	0.065
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.5	C 0.020
R	0.8	0.031
S	1.1	0.043
T	R 3.0	R 0.118
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$

Remark Dimensions and materials of ES products are the same as those of mass-production products.

12. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78P048A.

For details of the recommended soldering conditions, refer to our information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 12-1. Soldering Conditions for Surface-Mount Type

μPD78P048AGF-3B9: 80-pin plastic QFP (14 × 20 mm)

	Soldering Method	Soldering Conditions	Recommended Condition Symbol
★	Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Thrice max.	IR35-00-3
★	VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Thrice max.	VP15-00-3
	Wave soldering	Solder bath temperature: 260 °C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120 °C max. (Package surface temperature)	WS60-00-1
	Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Caution Using more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for development of systems using the μPD78P048A:

Language Processing Software

RA78K/0[Note 1, 2, 3, 4]	Assembler package common to 78K/0 series
CC78K/0[Note 1, 2, 3, 4]	C compiler package common to 78K/0 series
DF78044[Note 1, 2, 3, 4]	Device file for μPD78044F subseries
CC78K/0-L[Note 1, 2, 3, 4]	C compiler library source file common to 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P048GF PA-78P048KL-S	Programmer adapter connected to PG-1500
PG-1500 Controller[Note 1, 2]	Control program for PG-1500

Debugging Tools

	IE-78000-R	In-circuit emulator common to 78K/0 series
★	IE-78000-R-A	In-circuit emulator common to 78K/0 series (for integrated debugger)
	IE-78000-R-BK	Break board common to 78K/0 series
	IE-78044-R-EM	Emulation board for evaluating μPD78044F subseries
	EP-78130GF-R	Emulation probe common to μPD78134
	EV-9200G-80	Socket mounted to target system created for 80-pin plastic QFP (GF-3B9 type)
	SM78K0[Note 5, 6, 7]	System simulator common to 78K/0 series
★	ID78K0[Note 4, 5, 6, 7]	Integrated debugger for IE-78000-R-A
	SD78K/0[Note 1, 2]	Screen debugger for IE-78000-R
	DF78044[Note 1, 2, 4, 5, 6, 7]	Device file for μPD78044F subseries

Real-time OS

RX78K/0[Note 1, 2, 3, 4]	Real-time OS for 78K/0 series
MX78K0[Note 1, 2, 3, 4]	OS for 78K/0 series

Notes 1. PC-9800 series (MS-DOS™) based

2. IBM PC/AT™ and compatible (PC DOS™/IBM DOS™/MS-DOS) based

3. HP9000 series 300™ (HP-UX™) based

4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (Sun OS™) based, EWS4800 series (EWS-UX/V) based

5. PC-9800 series (MS-DOS + Windows™) based

6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based

★ **7.** NEWS™ (NEWS-OS™) based

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 3]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Note 1, 2]	Fuzzy inference module
FD78K0[Note 1, 2]	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS) based

2. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS) based

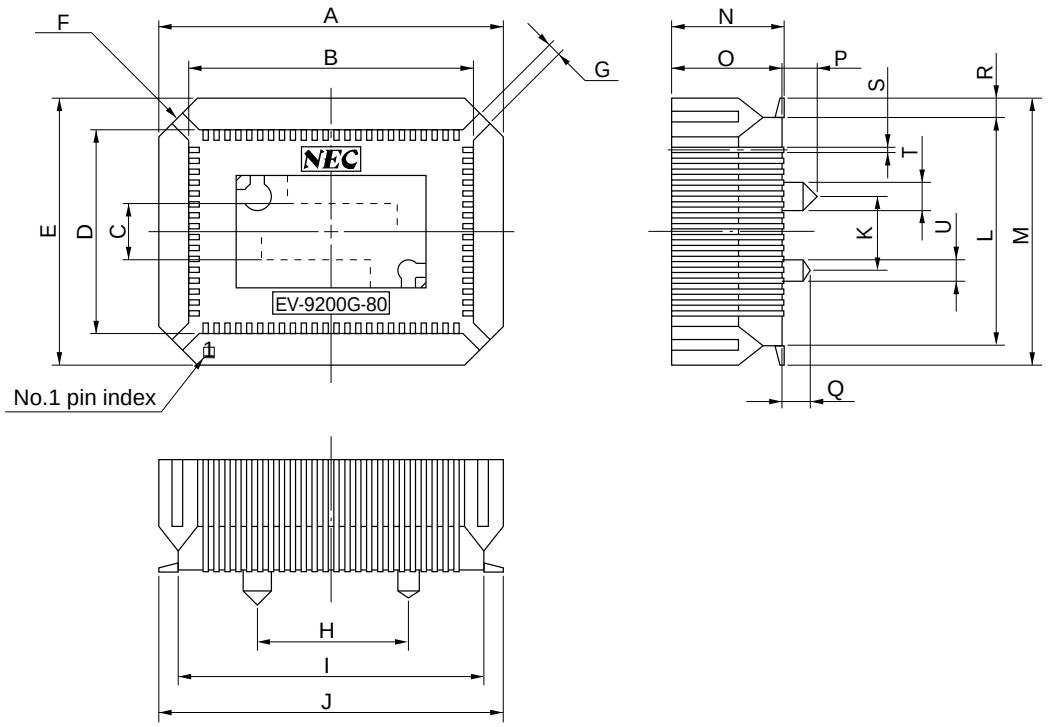
3. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based

Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.

2. RA78K/0, CC78K/0, SM78K0, ID78K0, RX78K/0, and SD78K/0 are used in combination with DF78044.

DIMENSIONS AND RECOMMENDED MOUNTING PATTERN OF CONVERSION SOCKET

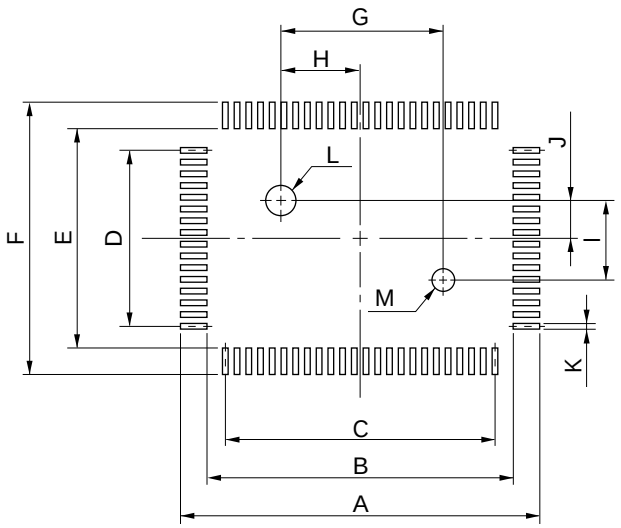
Figure A-1. Dimensions of EV-9200G-80 (Reference)



EV-9200G-80-G0E

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
N	8.0	0.315
O	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	φ2.3	φ0.091
U	φ1.5	φ0.059

Figure A-2. Recommended Mounting Pattern of V-9200G-80



EV-9200G-80-P1E

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$0.8\pm0.02\times23=18.4\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.906=0.724^{+0.003}_{-0.002}$
D	$0.8\pm0.02\times15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00 ± 0.08	$0.433^{+0.004}_{-0.003}$
H	5.50 ± 0.03	$0.217^{+0.001}_{-0.002}$
I	5.00 ± 0.08	$0.197^{+0.003}_{-0.004}$
J	2.50 ± 0.03	$0.098^{+0.002}_{-0.001}$
K	0.5 ± 0.02	$0.02^{+0.001}_{-0.002}$
L	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
M	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

- **Device Related Documents**

Document Name	Document No.	
	Japanese	English
μPD78044F Subseries User's Manual	U10908J	U10908E
μPD78042F, 78043F, 78044F, 78045F Data Sheet	U10700J	U10700E
μPD78P048A Data Sheet	U10611J	This document
μPD78044A, 78044F Subseries Special Function Register Table	U10701J	—
78K/0 Series User's Manual-Instruction	U12326J	U12326E
78K/0 Series Instruction Set	U10904J	—
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Application Note-Basics (II)	U10121J	U10121E

- **Development Tool Related Documents (User's Manual) (1/2)**

	Document Name		Document No.	
			Japanese	English
	RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
		Language	EEU-815	EEU-1404
	RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
★	RA78K0 Assembler Package	Structured assembly language	U11789J	U11789E
		Assembly language	U11801J	U11801E
		Operation	U11802J	U11802E
	CC78K Series C Compiler	Operation	EEU-656	EEU-1280
		Language	EEU-655	EEU-1284
★	CC78K/0 C Compiler	Operation	U11517J	U11517E
		Language	U11518J	U11518E
	CC78K Series Library Source File		U12322J	—
	CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	EEA-1208
	PG-1500 PROM Programmer		U11940J	EEU-1335
	PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
	PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
	IE-78000-R		U11376J	U11376E
★	IE-78000-R-A		U10057J	U10057E
	IE-78000-R-BK		EEU-867	EEU-1427
	IE-78044-R-EM		EEU-833	EEU-1424
	EP-78130GF-R		EEU-943	EEU-1470
	SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
	SM78K Series System Simulator	External part user open interface specifications	U10092J	U10092E
★	ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
★	ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E

- **Development Tool Related Documents (User's Manual) (2/2)**

Document Name		Document No.	
		Japanese	English
★ ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
SD78K/0 Screen Debugger	Introduction	EEU-852	U10539E
PC-9800 Series (MS-DOS) Based	Reference	U10952J	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Based	Reference	U11279J	U11279E

- **Embedded Software Related Documents (User's Manual)**

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Fundamental	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Fundamental	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

- **Other Related Documents**

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Devices Quality Guarantee Guide	C11893J	MEI-1202
Microcomputer-Related Product Guide (Products by Other Manufacturers)	U11416J	—

Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The documents referred to in this publication may include preliminary versions. However preliminary versions are not marked as such.

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