

**SANYO****LC99350****2/5-Inch Frame Transfer CCD  
1.1M Pixel Color Image Sensor****Preliminary****Overview**

The LC99350 is a low-cost frame transfer CCD (charge-coupled device) solid-state imaging element that features 1.1M pixels in a 2/5-inch optical size. It supports both progressive scan readout of all 1296 × 846 pixels as well as a real-time monitor mode with data compressed by 1/3.

**Applications**

PC cameras, TV telephones, image input units, and digital still cameras

**Features**

- Progressive scan readout
- Real-time compressed-data monitor mode
- Variable speed electronic shutter
- Horizontal dual readout adopted (Since the even and odd pixels on a single horizontal line are read out in two operations, a line memory is required for signal processing.)

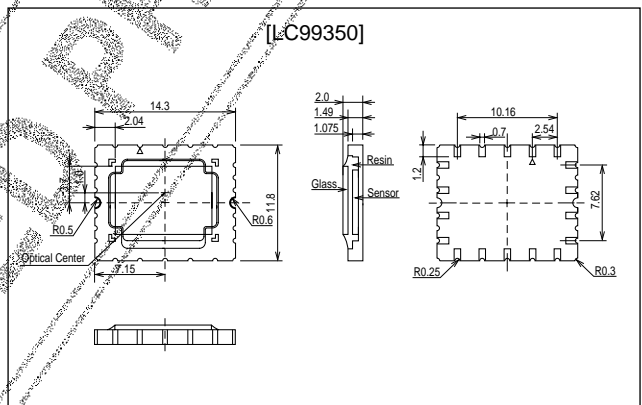
**Image Sensor Element Structure**

- Effective pixels [Total pixels]: 1296 × 864 [1392 × 888] (H×V)
- Number of optical blacks:  
Horizontal: 84 at the front, 12 at the rear  
Vertical direction: 12 at the top, 12 at the bottom
- Dummy bits: Horizontal: 6 pixels
- Unit cell size: 4.5 μm × 4.5 μm (H×V)
- Primary color mosaic filters (RGB)
- Parallel gate CCD sensor

- Consists of a 1392 × 888-pixel imaging block and a 1392 × 296-pixel storage block
- Three-phase drive used for the imaging and storage blocks, and 2-phase drive for the horizontal transfer block
- Built-in high-sensitivity output amplifier

**Package Dimensions**

unit: mm

**3250**

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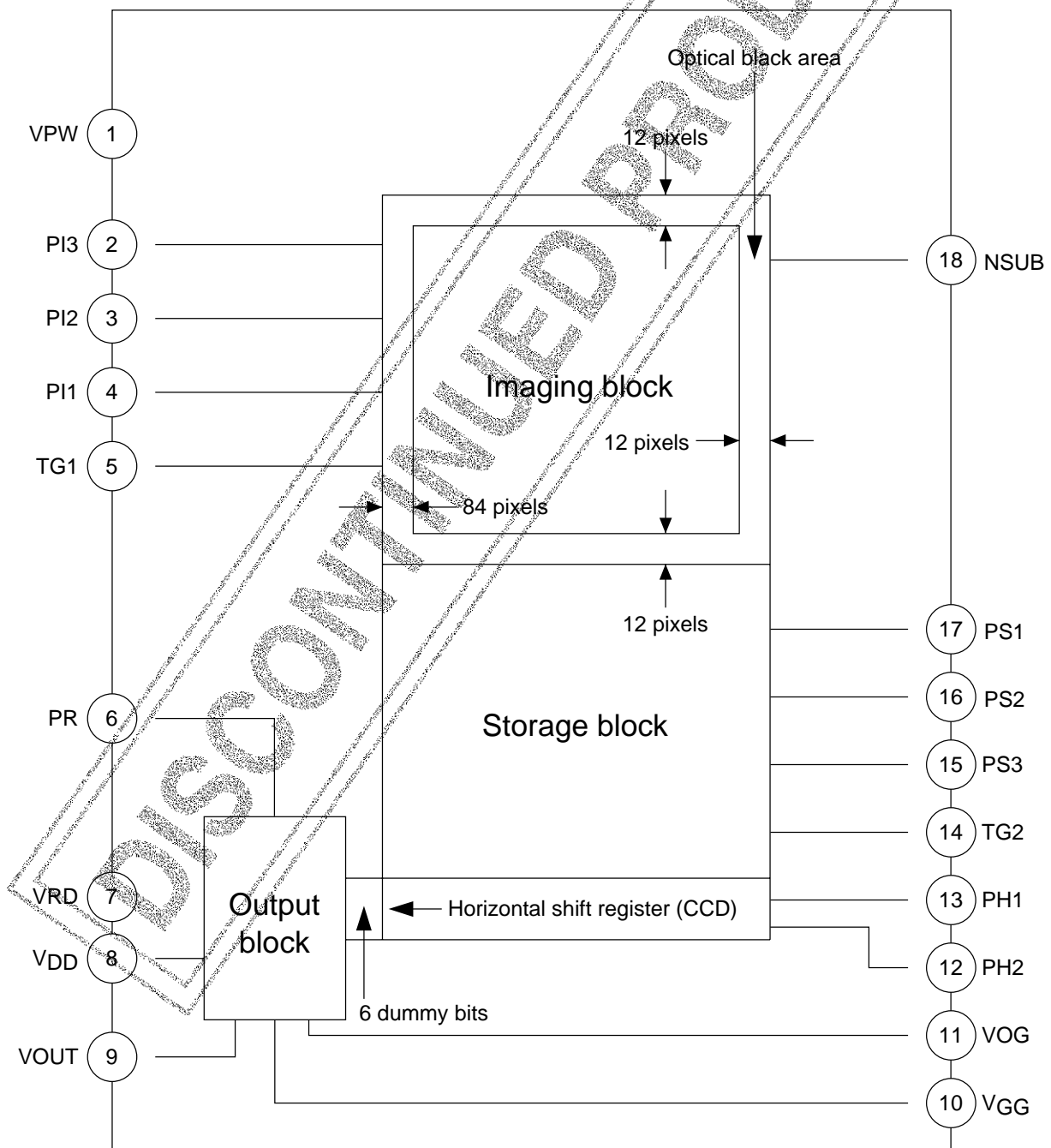
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Specifications

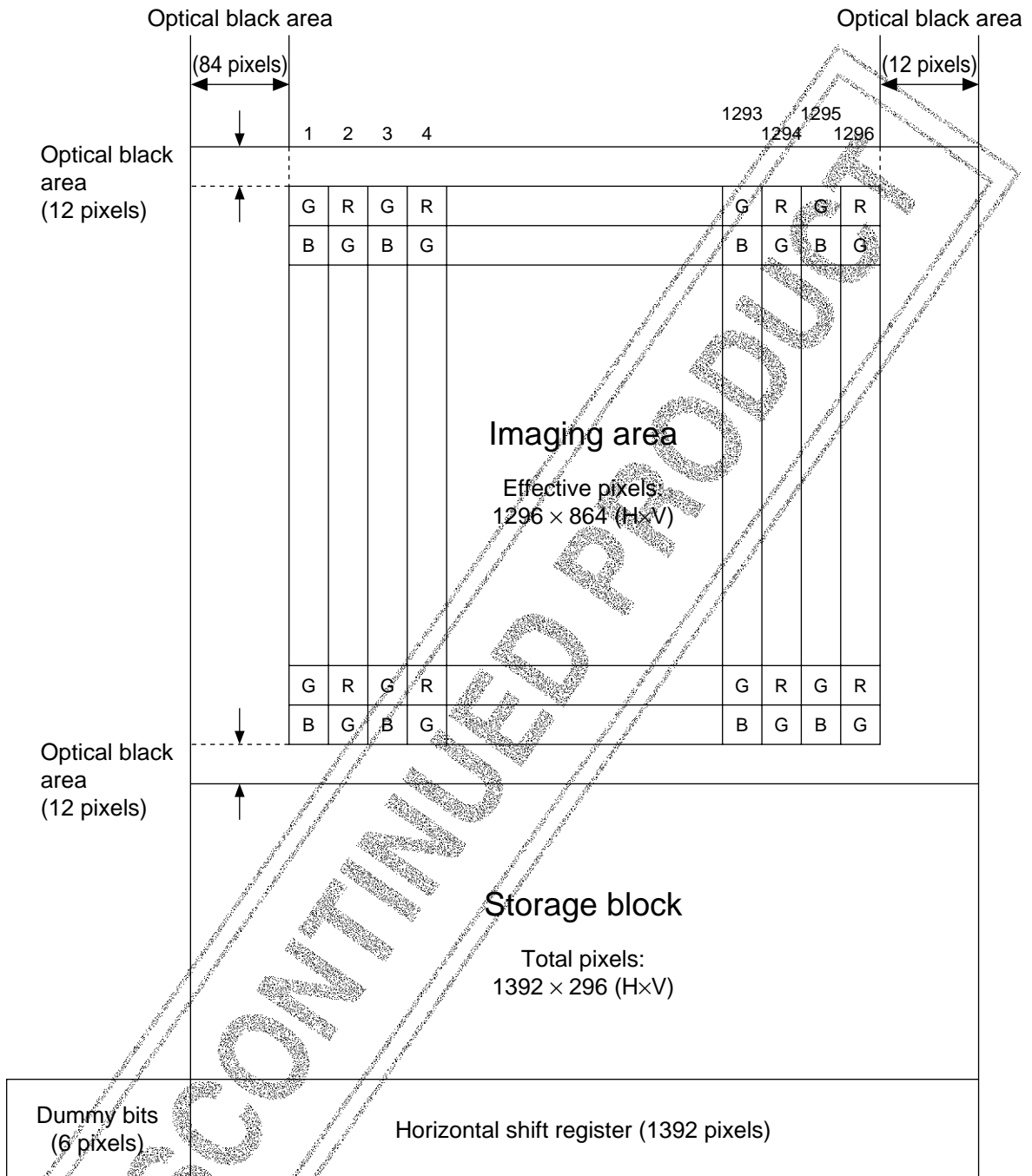
### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}, V_{RD}$	$V_{PW} = 0\text{ V}$	-0.3 to +15	V
Load gate voltage	$V_{GG}$	$V_{PW} = 0\text{ V}$	-0.3 to +3	V
N substrate p-well voltage		NSUB-PW: $V_{PW} = 0\text{ V}$	-0.3 to +35	V
N substrate imaging and storage block voltage		NSUB-PI1 to PI3, PS1 to PS3: $V_{PW} = 0\text{ V}$	-0.3 to +35	V
Horizontal block clock and reset gate voltage		Horizontal clock pin and PR: $V_{PW} = 0$	-0.3 to +15	V
Clock voltage		Clock pins other than the above: $V_{PW} = 0$	-15 to +15	V
Pin voltage		Pins other than the above	-0.3 to +10	V
Operating temperature	$T_{opr}$		-10 to +60	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-30 to +80	$^\circ\text{C}$

### Block diagram

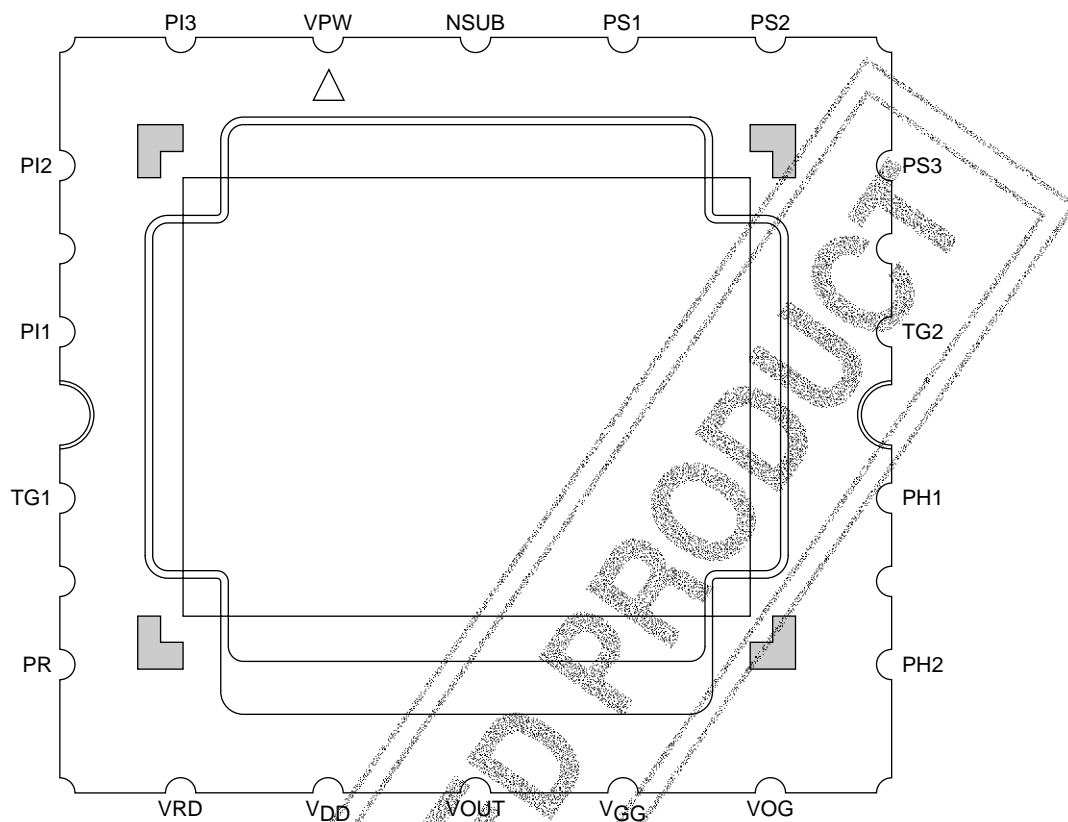


Pixel Arrangement



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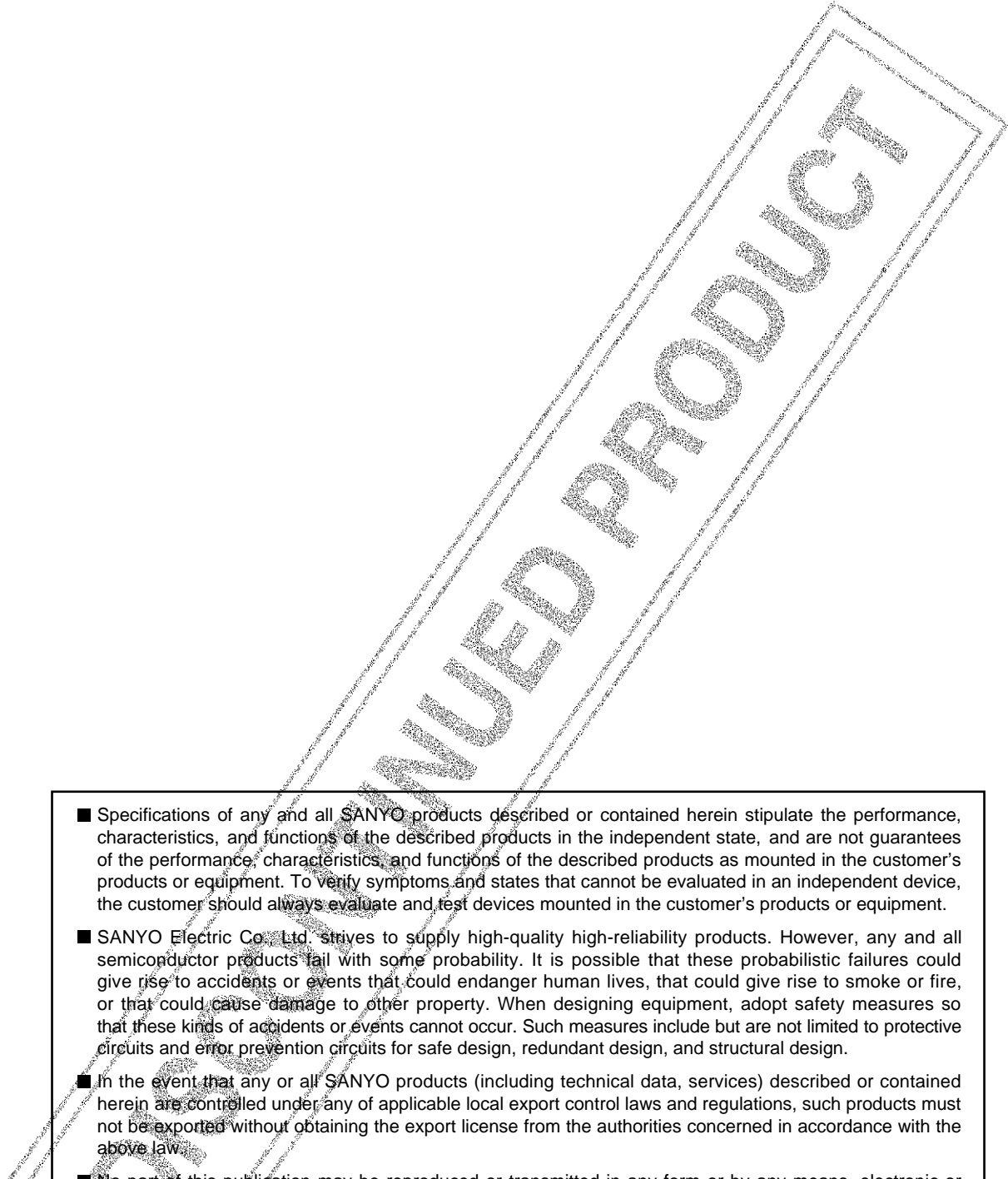
Pin Arrangement



A12672

Pin Functions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VPW	P-well	18	NSUB	N substrate
2	PI3	Imaging block clock	17	PS1	Storage block clock
3	PI2		16	PS2	
4	PI1		15	PS3	
5	TG1	Transfer gate	14	TG2	Transfer gate
6	PR	Reset gate	13	PH1	Horizontal block clock
7	VRD	Reset drain	12	PH2	
8	VDD	Supply voltage	11	VOG	CCD output gate
9	VOUT	CCD output	10	VGG	Load gate

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