SED1743

- **CMOS 160-bit LCD Common Driver**
- **Low Power**

■ DESCRIPTION

The SED1743 is an LCD common driver for high-resolution dot-matrix panels, which incorporates 160 row driver outputs. It is designed for use in conjunction with the SED1742 and SED1744 column drivers.

The SED1743 features a wide range of LCD drive voltages. The upper and lower drive voltages, V_0 and V_5 are independent of the chip supplies. This enables the LCD drive bias voltages to be supplied from an external source. As a result, the SED1743 is compatible with a large range of LCD panels.

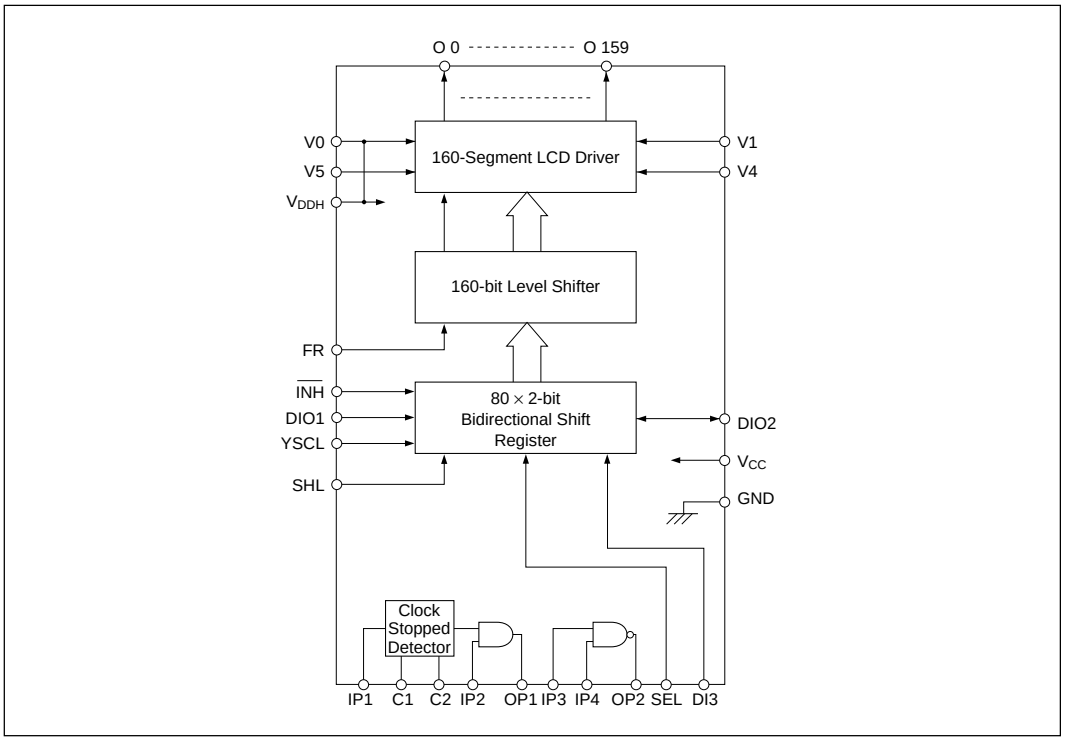
The SED1743 uses a daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1743 operates from a 2.7 to 5.5V supply and is available in both chip packages and tape-carrier packages (TCPs).

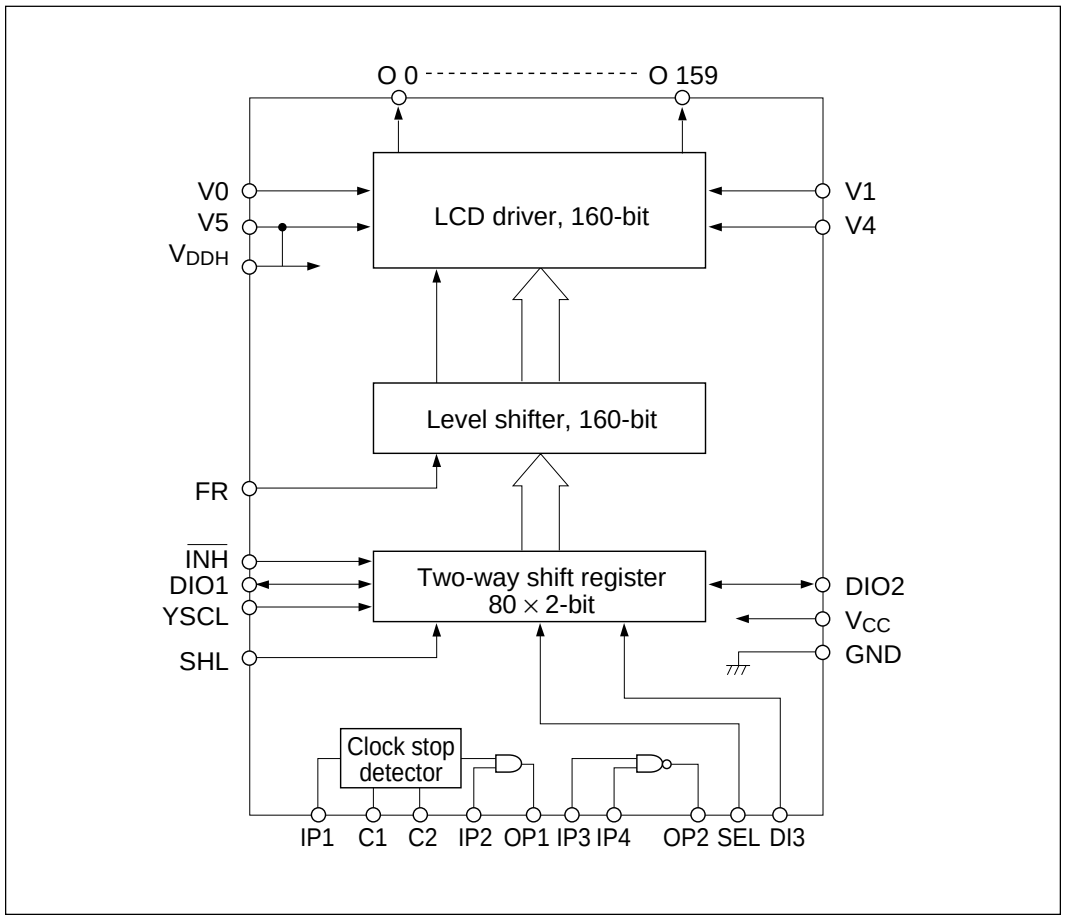
■ FEATURES

- 160 (80 × 2) LCD common drive outputs
- Pin-selectable output shift direction
- Adjustable LCD drive voltages
- Duty cycles up to 1/480
- Zero-bias display disable function
- Silicon-gate CMOS technology
- 1 kΩ typical output impedance
- 14 to 40V LCD drive voltages
- 2.7 to 5.5V supply
- Chip (SED1743D_{1B}) or tape-carrier (SED1743T_{0A}) packages

■ SYSTEM BLOCK DIAGRAM



■ **BLOCK DIAGRAM**



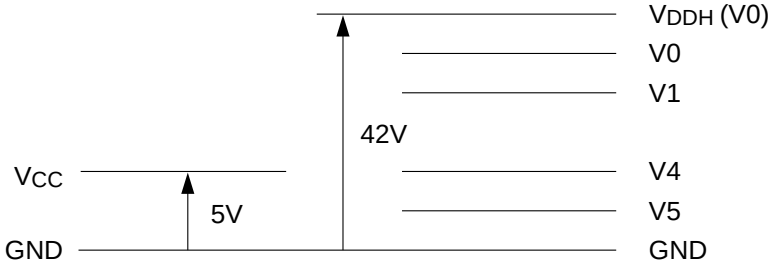
■ **PIN DESCRIPTION**

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Q'ty</th></tr>
<tr><td>O0 to 159</td><td>O</td><td>Common (row) output for liquid crystal display</td><td>160</td></tr>
<tr><td>DIO2
DIO1</td><td>I/O</td><td>DI01 ans DI02 are data onput/output to a bi-directional shift register; either one can be selected as input or output by setting. 80 × 2-bit two-way shift register scan pulse SHL input sets the terminal to input or output. The output varies at the YSCL trailing edge. The DI3 is the input terminal of the scan pulse when 80 × 2 configuration is used.</td><td>3</td></tr>
<tr><td>SEL</td><td>I</td><td>Shift register mode selection input
H: 80 × 2 (DI3 input) L: 160, also connect DI3 = GND</td><td>1</td></tr>
<tr><td>YSCL</td><td>I</td><td>Serial data shift clock input; negative edge triggered</td><td>1</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction select input
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">O (Output shift direction)</th><th colspan="2">DIO</th></tr>
<tr><th>DIO1</th><th>DIO2</th></tr>
<tr><td>L</td><td>0 → 159</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>159 → 0</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>Common drive signal polarity select input</td><td>1</td></tr>
<tr><td>V_{CC}, GND</td><td>Power Source</td><td>Logic power source. GND: 0 V; V_{CC}: +3 V, +5 V</td><td>2</td></tr>
<tr><td>V5, V4, V1, V0 and V_{DDH}</td><td>Power Source</td><td>Liquid crystal drive power source GND: 0 V; V_{DDH}: 8V to 42V
V_{DDH} (V0) ≥ V1 ≥ 8/9 V_{DDH}, 1/9 V_{DDH} ≥ V4 ≥ V5 ≥ GND</td><td>5</td></tr>
<tr><td>$\overline{INH}$</td><td>I</td><td>Display blanking input
Low-level input sets all the common outputs to V5 level.</td><td>1</td></tr>
<tr><td>IP1</td><td>I</td><td>Stop detector clock input</td><td>1</td></tr>
<tr><td>IP2</td><td>I</td><td>Signal input to be AND-ed with the stop detect output, equipped with internal pull-down resistor</td><td>1</td></tr>
<tr><td>C1</td><td>O</td><td>1st charge hold terminal, Capacitor externally mounted between GND</td><td>1</td></tr>
<tr><td>C2</td><td>O</td><td>2nd charge hold terminal, Capacitor and resistor externally mounted between GND</td><td>1</td></tr>
<tr><td>OP1</td><td>O</td><td>Clock stop detector output</td><td>1</td></tr>
<tr><td>IP3</td><td>I</td><td>NAND gate input internal pull-down resistor</td><td>1</td></tr>
<tr><td>IP4</td><td>I</td><td>NAND gate input</td><td>1</td></tr>
<tr><td>OP2</td><td>O</td><td>NAND gate output</td><td>1</td></tr>
<tr><td>DI3</td><td>I</td><td>Scan pulse input when 2 × 80 mode</td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range (1)	V_{CC}	–0.3 to +7.0	V
Supply voltage for LCD	V_{DDH}	–0.3 to +45.0	V
Supply voltage for LCD (3)	V0, V1, V4, V5	GND –0.3 to V_{DDH} +0.3	V
Input voltage (4)	V_I	GND –0.3 to V_{CC} +0.3	V
Output voltage	V_O	GND –0.3 to V_{CC} +0.3	V
EIO output current	I_{O1}	20	mA
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature 1 (2)	$T_{stg\ 1}$	–65 to +150	°C
Storage temperature 2 (2)	$T_{stg\ 2}$	–55 to +100	°C



Notes: 1. The voltage is based at GND = 0 V.
2. The storage temperature 1 is specified for a single chip and the storage temperature 2 is for TCP mounting.
3. Voltage V0, V1 and V4 should satisfy the condition: V_{DDH} (V0) ≥ V1 ≥ V4 ≥ V5 ≥ GND.
4. **CAUTION**: The LSI may be externally broken if the logic system power source floats or decreases below V_{CC}=2.6 V while voltage is applied to the liquid crystal drive system power source. Special care should betaken for the power source sequence when turning the system power on and off.

● Recommended Operating Conditions

T_a = 25°C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	5	V
Segment driver supply voltage range	V_{DDH}	14 to 40	V

T_a = 25°C

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{CC}	3	V
Segment driver supply voltage range	V_{DDH}	14 to 28	V

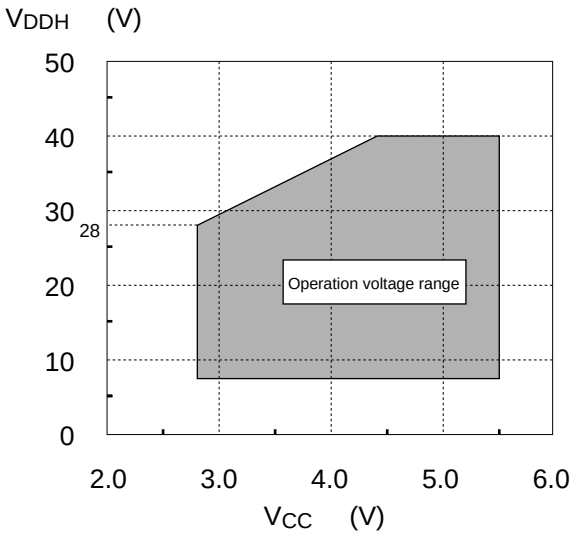
● **DC Electrical Characteristics**

(Unless otherwise specified, GND=V5=0V, V_{CC}= +5.0V ±10%, T_a= –20 to 75°C)

Parameter	Symbol	Condition		Terminal	Min	Typ	Max	Unit
Logic supply voltage (1)	V_{CC}			V_{CC}	2.7	5.0	5.5	V
Operation voltage recommended	V_{DDH}			V_{DDH}	8.0	—	42	V
Common driver supply voltage	V_{DDH} (V0)	Function		V_{DDH}	8.0	—	42	V
Common driver supply voltage	V1	Value recommended		V1	8/9V_{DDH}	—	—	V
Common driver supply voltage	V4, V5	Value recommended		V4	GND	—	1/9V_{DDH}	V
High level input voltage	V_{IH}	V_{CC} = 3.0 to 5.5 V		DIO1, DIO2, DI3, IP1 to 4, SEL, FR, YSCL, SHL, $\overline{INH}$	0.8V_{CC}	—	—	V
Low level input voltage	V_{IL}				—	—	0.2V_{CC}	V
High level output voltage	V_{OH}	V_{CC} = 3 to 5.5 V	I_{OH} = –0.3 mA	DIO1, DIO2	V_{CC} –0.4	—	—	V
Low level output voltage	V_{OL}		I_{OL} = 0.3 mA	OP1, OP2	—	—	0.4	V
Low–level input leakage current	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}		DI3, SEL, FR, YSCL, SHL, $\overline{INH}$	—	—	2.0	µA
High-level input leakage current	I_{IH}	V_{IN} ≤ V_{CC}		IP2, IP3	40	80	180	µA
Input/Output leak current	$I_{LI/O}$	GND ≤ V_{IN} ≤ V_{CC}		DIO1, DIO2	—	—	5.0	µA
Static current	I_{GND}	V_{DDH} = 14.0 to 40.0 V V_{IH} = V_{CC}, V_{IL} = GND		GND	—	—	25	µA
Output resistance	R_{COM}	ΔVON = 0.5V condition recommended	V_{DDH}=+30.0V	O0 to O159	—	0.65	2.0	kΩ
			V_{DDH}=+20.0V		—	0.7	2.1	
Average operation current consumed (1)	I_{CC}	V_{CC} = +5.0 V, V_{IH} = V_{CC}, V_{IL} = GND, f_{XSCL} =33.6 kHz, f_{FR} =70 Hz; Input data: 1/480, No load		V_{CC}	—	9	20	µA
		V_{CC} = +3.0 V Other condition: Same as V_{CC} = 5V			—	6	10	
Average operation current consumed (2)	I_{DDH}	V_{DDH} = V0 = +30.0 V, V1 = +28.0 V, V4 = +2.0 V, V5 = +0.0 V, V_{CC} = +5.0 V; Other condition: same as I_{CC}		V_{DDH}	—	4	25	µA
Input capacitance	C_I	Freq.=1 MHz, T_a = 25°C Single chip		DI3, IP1 TO 4, SEL, FR, YSCL, SHL, INH	—	—	8	pF
I/O terminal capacity	$C_{I/O}$			DIO1, DIO2	—	—	15	pF

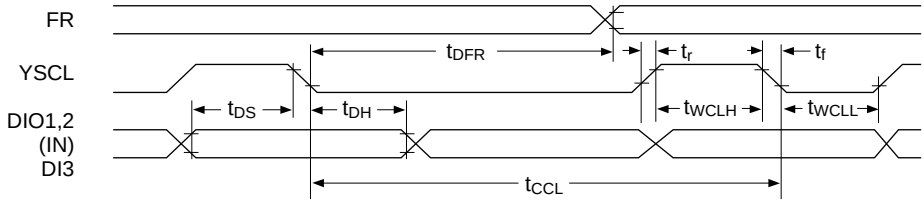
● **Operation Voltage Range V_{CC}–V_{DDH}**

The maximum LCD supply voltage, V_{DDH}, depends on V_{CC} as shown in the following figure. Specify the V_{DDH} voltage within the V_{CC}–V_{DDH} operation.



● **AC Electrical Characteristics**

○ **Input Timing Characteristics**



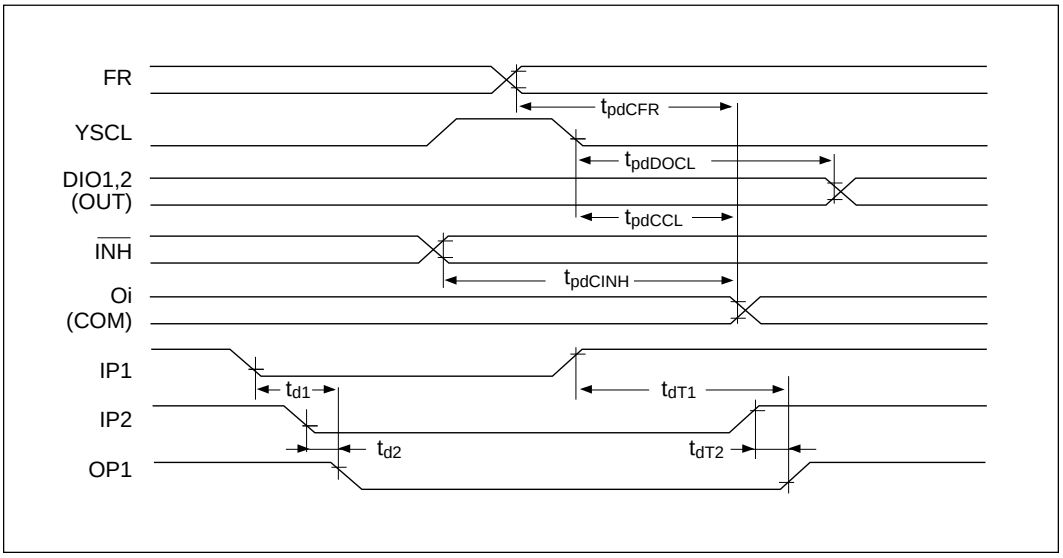
(V_{CC} = 5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL cycle	t_{CCL}		400	—	—	ns
YSCL high-level pulse width	t_{WCLH}		60	—	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		40	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
FR delay allowance time	t_{DFR}		–300	—	+300	ns
Input signal rise time	t_r		—	—	50	ns
Input signal breaking time	t_f		—	—	50	ns

(V_{CC} = 3.0 to 4.5 V, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL cycle	t_{CCL}		800	—	—	ns
YSCL high-level pulse width	t_{WCLH}		80	—	—	ns
YSCL low-level pulse width	t_{WCLL}		660	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		50	—	—	ns
FR delay allowance time	t_{DFR}		–400	—	400	ns
Input signal rise time	t_r		—	—	100	ns
Input signal breaking time	t_f		—	—	100	ns

○ **Output Timing Characteristics**



(V_{CC} = +5.0 V ±10%, V_{DDH} = 40.0 V)

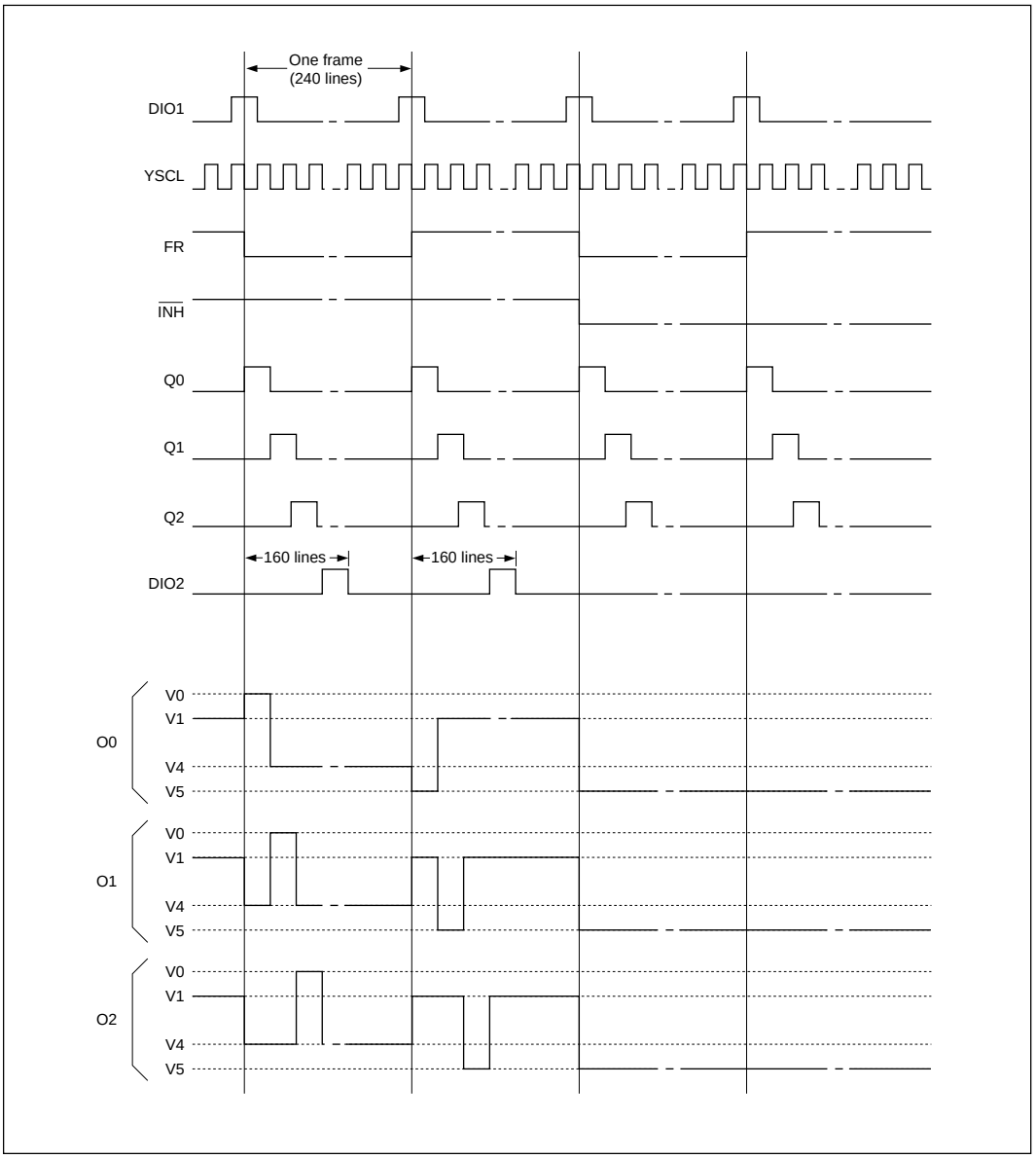
Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL → DIO output delay time	t_{pdDOCL}	C_L = 15 pF	—	—	100	ns
YSCL → COM output delay time	t_{pdCCL}	V_{DDH} = 14.0 to 40.0 V C_L = 100 pF	—	—	160	ns
$\overline{INH}$ → COM output delay time	t_{pdCINH}		—	—	160	ns
FR → COM output delay time	t_{pdCFR}		—	—	160	ns
IP1 → OP1 output delay time	t_{d1}	C_L = 15 pF	—	—	4C2R2	ns
IP1 → OP1 output release time	t_{dT1}		—	—	2 × YD cycle	ns
IP2 → OP1 output delay time	t_{d2}		—	—	100	ns
IP2 → OP1 output release time	t_{dT2}		—	—	100	ns

(V_{CC} = 3.0 to 4.5 V, V_{DDH} = 140.0 to 28.0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
YSCL → DIO output delay time	t_{pdDOCL}	C_L = 15 pF	—	—	200	ns
YSCL → COM output delay time	t_{pdCCL}	V_{DDH} = 14.0 to 40.0 V C_L = 100 pF	—	—	300	ns
$\overline{INH}$ → COM output delay time	t_{pdCINH}		—	—	300	ns
FR → COM output delay time	t_{pdCFR}		—	—	300	ns
IP1 → OP1 output delay time	t_{d1}	C_L = 15 pF	—	—	4C2R2	ns
IP1 → OP1 output release time	t_{dT1}		—	—	2 × YD cycle	ns
IP2 → OP1 output delay time	t_{d2}		—	—	200	ns
IP2 → OP1 output release time	t_{dT2}		—	—	200	ns

Note: YD: Scan Start Pulse
For C2R2, see 11. Clock stop detector circuit.

- **Timing Diagrams**
  - 1/240 Duty Cycle



■ FUNCTIONAL DESCRIPTION

● Shift Register

The shift register is a bi-directional shift register, where the shift direction is selected by SHL. The effect of SHL on the shift direction and on the input data sequence is shown in the following table.

Data Sequence and Shift Direction

SHL	LCD Outputs							Shift Direction	
	O159	O158	O157	...	O2	O1	O0	DIO1	DIO2
L	a	b	c	...	x	y	z	Input	Output
H	z	y	x	...	c	b	a	Output	Input

SEL is used to select the operating mode of the shift register. When SEL is HIGH, 2×80 mode is selected. When SEL is LOW, 1×160 mode is selected.

● Level Shifter

The level shifter converts the logic-level signals from the latch into the LCD driver input voltage levels.

● LCD Drivers

The LCD drivers generate the AC LCD drive waveforms. The output voltages are determined by the polarity of the FR signal, as shown in the following table.

Driver Output Voltage

$\overline{INH}$	Input Data	FR	Output Voltage
H	H	H	V5
		L	V0 (V_{DDH})
	L	H	V1
		L	V4
L	X	X	V5

X = don't care

■ APPLICATION NOTES

● Voltage Levels

The recommended method of generating the LCD drive voltages, V0 to V5, is with a voltage divider between V_{DDH} and V_{GND}, buffered with voltage followers.

The lower drive level, V5, is not necessarily at V_{GND}, and separate pins are used for the voltage levels when op-amps are used. A maximum voltage differential between V5 and V_{GND} of 2.5V is recommended since the driver efficiency decreases as the differential increases. Connect V5 to GND when not using op-amps.

The resistances of the voltage divider resistors should be as low as possible and within power supply constraints.

Note that fluctuations in I_{DDH} can cause dips in the V_{DDH} supply. The device will be damaged if the voltage dips below the point where the relationship V_{DDH} (V0) ≥ V1 ≥ V4 ≥ V5 ≥ V_{GND} breaks down. A stabilized power supply may be required when using the resistor network.

- **Clock Monitor**

The LCD panel can be damaged if a DC signal is applied to the segments. This situation can occur when the AC drive clock stops while power is applied to the display. The clock monitor circuit detects this condition and sends OP1 LOW. If OP1 is connected to INH, the display is protected from damage.

- **Power-Up and Power-Down Precautions**

As the driver circuitry operates at high voltage, care should be taken when applying and removing power to the SED1743 to prevent damage. If the driver supply is applied when the logic supply is either not connected or below 2.9V, excess current will flow into the SED1742 and damage the device. Normal operation is guaranteed if the correct power-up and power-down sequences are followed.

Power-Up Sequence:

Power should be applied to V_{CC} before, or at the same time as, power is applied to the driver circuitry.

Power-Down Sequence:

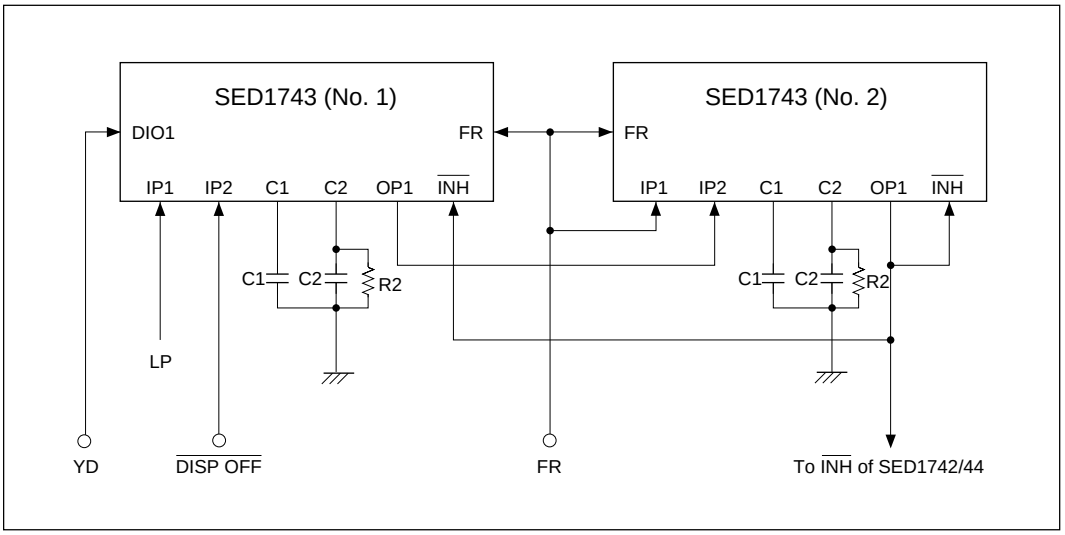
Power should be removed from V_{CC} after, or at the same time as, power is removed from the driver circuitry.

The SED1743 can also be damaged if the LCD output drivers start operating before the driver supplies stabilize. $\overline{INH}$ should be held LOW to hold the driver outputs at V5 until the driver supplies have stabilized.

As an additional protective measure, insert a fast-blow fuse in series with the driver supply.

- **Clock Monitor Circuit**

The clock monitor circuit sets OP1 LOW whenever the clock signals from the controller stops. Connecting OP1 to $\overline{INH}$ ensures that DC does not flow into the LCD panel.



R2 is typically several MΩ and C1 and C2 are determined while monitoring OP1. C1 should be much larger than C2. Typical values under various signal conditions are shown in the following table.

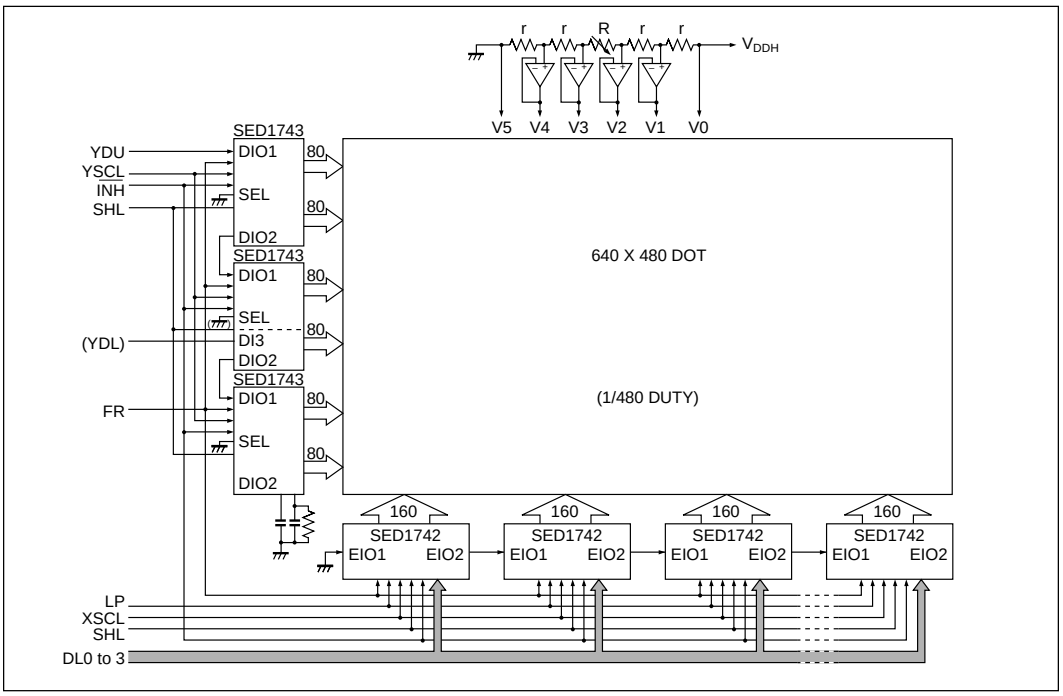
Input Signal	C1	C2	R2
LP = IP1	0.1 µF	.01 ~ .1µF	3.3 MΩ
FR = IP1	0.1 µF	.01 ~ .1µF	3.3 MΩ

Notes: YD: tc = 17.8 ms, duty = 0.14%
LP: tc = 40.4 ms, duty = 0.35%
FR: tc = 3.53 ms, duty = 50%

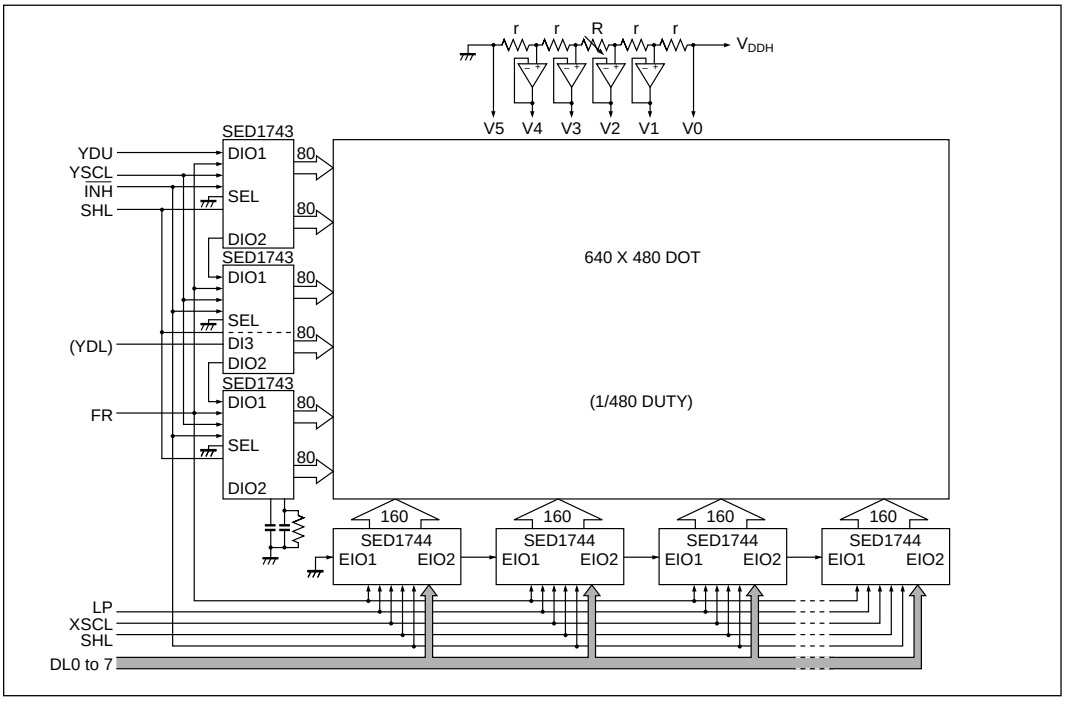
When the clock monitor feature is not required, tie IP1, IP2, IP3 and C2 LOW, and leave OP1, OP2 and C1 OPEN.

■ CIRCUIT DIAGRAM FOR REFERENCE

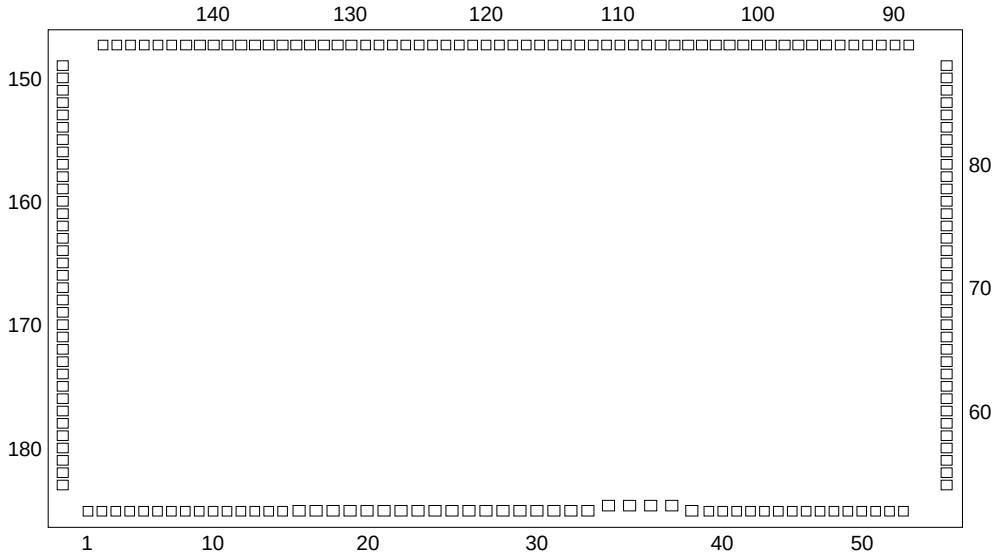
(Combination of SED1742 with SED1743)



(Combination of SED1744 with SED1743)



■ **PAD LAYOUT FOR SED1742/3/4 (D_{1B} Version)**



Chip Size ..... 7.30mm × 4.48mm
Pad Pitch ..... 108µm (Min.)
Chip Thickness ..... 525µm ± 25µm

1) Au Bump

Bump Size A	72µm × 93µm ± 4µm	(Pad Nos. 1~15, 39~183)
Bump Size B	93µm × 106µm ± 4µm	(Pad Nos. 16~33, 38)
Bump Size C	93µm × 93µm ± 4µm	(Pad Nos. 34~37)

Bump Height 17 ~ 28µm

■ PAD COORDINATES

Pad No.	Pin Name	X	Y
1	NC	–3228	–2064
2	NC	–3120	–2064
3	NC	–3012	–2064
4	NC	–2903	–2064
5	NC	–2795	–2064
6	NC	–2687	–2064
7	NC	–2578	–2064
8	NC	–2470	–2064
9	NC	–2362	–2064
10	NC	–2253	–2064
11	NC	–2145	–2064
12	NC	–2037	–2064
13	NC	–1929	–2064
14	NC	–1820	–2064
15	NC	–1712	–2064
16	DIO2	–1550	–2058
17	DIO1	–1417	–2058
18	GND	–1284	–2058
19	SEL	–1151	–2058
20	OP1	–1018	–2058
21	C1	–885	–2058
22	IP1	–752	–2058
23	C2	–619	–2058
24	IP2	–486	–2058
25	DI3	–353	–2058
26	IP3	–220	–2058
27	SHL	–87	–2058
28	YSCL	46	–2058
29	IP4	179	–2058
30	INH	312	–2058
31	OP2	445	–2058
32	VCC	578	–2058
33	FR	711	–2058
34	V5	872	–2026
35	V4	1034	–2026
36	V1	1195	–2026
37	V0	1357	–2026
38	VDDH	1550	–2058
39	NC	1712	–2064
40	NC	1820	–2064

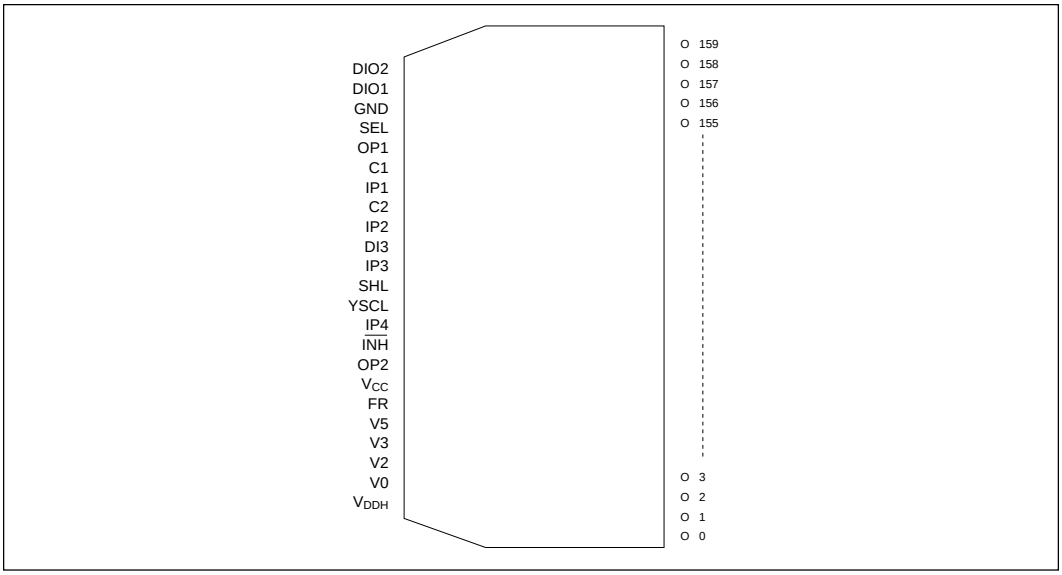
Pad No.	Pin Name	X	Y
41	NC	1929	–2064
42	NC	2037	–2064
43	NC	2145	–2064
44	NC	2253	–2064
45	NC	2362	–2064
46	NC	2470	–2064
47	NC	2578	–2064
48	NC	2687	–2064
49	NC	2795	–2064
50	NC	2903	–2064
51	NC	3012	–2064
52	NC	3120	–2064
53	NC	3228	–2064
54	NC	3474	–1841
55	NC	3474	–1733
56	NC	3474	–1625
57	NC	3474	–1516
58	NC	3474	–1408
59	NC	3474	–1300
60	NC	3474	–1191
61	NC	3474	–1083
62	NC	3474	–975
63	NC	3474	–866
64	NC	3474	–758
65	NC	3474	–650
66	NC	3474	–542
67	NC	3474	–433
68	NC	3474	–325
69	O0	3474	–217
70	O1	3474	–108
71	O2	3474	0
72	O3	3474	108
73	O4	3474	217
74	O5	3474	325
75	O6	3474	433
76	O7	3474	542
77	O8	3474	650
78	O9	3474	758
79	O10	3474	866
80	O11	3474	975

Pad No.	Pin Name	X	Y
81	O12	3474	1083
82	O13	3474	1191
83	O14	3474	1300
84	O15	3474	1408
85	O16	3474	1516
86	O17	3474	1625
87	O18	3474	1733
88	O19	3474	1841
89	O20	3195	2064
90	O21	3087	2064
91	O22	2978	2064
92	O23	2870	2064
93	O24	2762	2064
94	O25	2653	2064
95	O26	2545	2064
96	O27	2437	2064
97	O28	2328	2064
98	O29	2220	2064
99	O30	2112	2064
100	O31	2004	2064
101	O32	1895	2064
102	O33	1787	2064
103	O34	1679	2064
104	O35	1570	2064
105	O36	1462	2064
106	O37	1354	2064
107	O38	1245	2064
108	O39	1137	2064
109	O40	1029	2064
110	O41	921	2064
111	O42	812	2064
112	O43	704	2064
113	O44	596	2064
114	O45	487	2064
115	O46	379	2064
116	O47	271	2064
117	O48	162	2064
118	O49	54	2064
119	O50	–54	2064
120	O51	–162	2064

Pad No.	Pin Name	X	Y
121	O52	–271	2064
122	O53	–379	2064
123	O54	–487	2064
124	O55	–596	2064
125	O56	–704	2064
126	O57	–812	2064
127	O58	–921	2064
128	O59	–1029	2064
129	O60	–1137	2064
130	O61	–1245	2064
131	O62	–1354	2064
132	O63	–1462	2064
133	O64	–1570	2064
134	O65	–1679	2064
135	O66	–1787	2064
136	O67	–1895	2064
137	O68	–2004	2064
138	O69	–2112	2064
139	O70	–2220	2064
140	O71	–2328	2064
141	O72	–2437	2064
142	O73	–2545	2064
143	O74	–2653	2064
144	O75	–2762	2064
145	O76	–2870	2064
146	O77	–2978	2064
147	O78	–3087	2064
148	O79	–3195	2064
149	O80	–3474	1841
150	O81	–3474	1733
151	O82	–3474	1625
152	O83	–3474	1516
153	O84	–3474	1408
154	O85	–3474	1300
155	O86	–3474	1191
156	O87	–3474	1083
157	O88	–3474	975
158	O89	–3474	866
159	O90	–3474	758
160	O91	–3474	650

Pad No.	Pin Name	X	Y
161	O92	–3474	542
162	O93	–3474	433
163	O94	–3474	325
164	O95	–3474	217
165	O96	–3474	108
166	O97	–3474	0
167	O98	–3474	–108
168	O99	–3474	–217
169	NC	–3474	–325
170	NC	–3474	–433
171	NC	–3474	–542
172	NC	–3474	–650
173	NC	–3474	–758
174	NC	–3474	–866
175	NC	–3474	–975
176	NC	–3474	–1083
177	NC	–3474	–1191
178	NC	–3474	–1300
179	NC	–3474	–1408
180	NC	–3474	–1516
181	NC	–3474	–1625
182	NC	–3474	–1733
183	NC	–3474	–1841

■ TAPE CARRIER PACKAGE – PINOUT



■ TAPE CARRIER PACKAGE – DIMENSIONS