

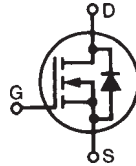
CoolMOS™ Power MOSFET IXKC 40N60C

in ISOPLUS220™ Package

Electrically Isolated Back Surface

Low $R_{DS(on)}$, High Voltage, CoolMOS™ Superjunction MOSFET

Preliminary Data Sheet



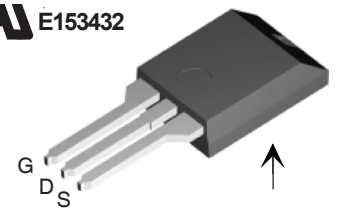
$$V_{DSS} = 600 \text{ V}$$

$$I_{D25} = 28 \text{ A}$$

$$R_{DS(on)} = 96 \text{ m}\Omega$$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	600	V
V_{GS}	Continuous	± 20	V
I_{D25}	$T_C = 25^\circ\text{C}$; Note 1	28	A
I_{D90}	$T_C = 90^\circ\text{C}$; Note 1	19	A
$I_{D(RMS)}$	Package lead current limit	45	A
E_{AS}	$I_o = 10\text{A}$, $T_C = 25^\circ\text{C}$	690	mJ
E_{AR}	$I_o = 20\text{A}$	1	mJ
P_D	$T_C = 25^\circ\text{C}$	250	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +125	$^\circ\text{C}$
T_L	1.6 mm (0.062 in.) from case for 10 s	300	$^\circ\text{C}$
V_{ISOL}	RMS leads-to-tab, 50/60 Hz, $t = 1$ minute	2500	V~
F_C	Mounting force	11 ... 65 / 2.4 ... 11	N/lb
Weight		3	g

ISOPLUS220™
E153432



Isolated back surface*

G = Gate, D = Drain,
S = Source

* Patent pending

Features

- Silicon chip on Direct-Copper-Bond substrate
 - High power dissipation
 - Isolated mounting surface
 - 2500V electrical isolation
- 3rd generation CoolMOS™ power MOSFET
 - High blocking capability
 - Low on resistance
 - Avalanche rated for unclamped inductive switching (UIS)
- Low thermal resistance due to reduced chip thickness
- Low drain to tab capacitance (<30pF)

Applications

- Switched Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- Power Factor Correction (PFC)
- Welding
- Inductive Heating

Advantages

- Easy assembly: no screws or isolation foils required
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = I_{D90}$, Note 3 $V_{GS} = 10 \text{ V}$, $I_D = I_{D90}$, Note 3 $T_J = 125^\circ\text{C}$		80 230	96 mΩ mΩ
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 2 \text{ mA}$	3.5		5.5 V
I_{DSS}	$V_{DS} = V_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$		20	2 μA μA
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			± 200 nA

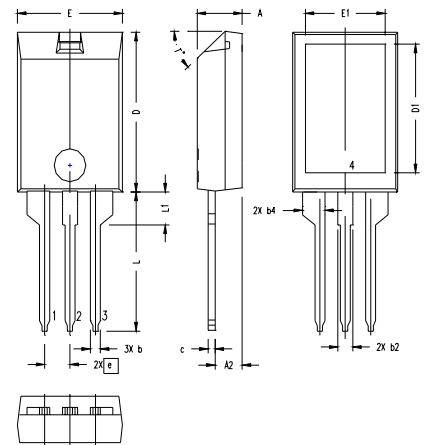
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Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
$Q_{g(\text{on})}$	$V_{GS} = 10\text{ V}, V_{DS} = 350\text{ V}, I_D = 40\text{ A}$		158	nC
Q_{gs}			42	nC
Q_{gd}			92	nC
$t_{d(\text{on})}$	$V_{GS} = 10\text{ V}, V_{DS} = 380\text{ V}$ $I_D = 40\text{ A}, R_G = 1.8\ \Omega$		20	ns
t_r			55	ns
$t_{d(\text{off})}$			60	ns
t_f			10	ns
R_{thJC}			0.5	K/W
R_{thCH}		0.30		K/W

Reverse Correction		Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
Symbol	Test Conditions	min.	typ.	max.
V_{SD}	$I_F = 20\text{ A}, V_{GS} = 0\text{ V}$ Note 3	0.8	1.2	V

Note: 1. MOSFET chip capability
 2. Intrinsic diode capability
 3. Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$

ISOPLUS 220LV Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5*	47.5*

Notes:

1. Lead 1 = Gate
2. Lead 2 = Drain
3. Lead 3 = Source
4. Back surface 4 is electrically isolated from leads 1, 2 & 3

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more	4,835,592	4,881,106	5,017,508	5,049,961	5,187,117	5,486,715	6,306,728B1	6,259,123B1
	4,850,072	4,931,844	5,034,796	5,063,307	5,237,481	5,381,025	6,404,065B1	6,162,665