DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD789405A, 789406A, 789407A, 789415A, 789416A, 789417A

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A are products in the μPD789407A and 789417A subseries (for driving LCD) of the 78K/0S series.

In addition to these products, a flash memory model, μPD78F9418A, that can operate at the same voltage as the mask-ROM models, and various development tools are also under development.

For a detailed description of their functions, refer to the following User's Manuals:

μPD789407A, 789417A Subseries User's Manual : Planned to be published
78K/0S Series User's Manual – Instructions : U11047E

FEATURES

- **ROM/RAM capacity**

Item / Part Number	Program Memory (ROM)	Data Memory	
		Internal high-speed RAM	LCD display RAM
μPD789405A, 789415A	12 K bytes	512 × 8 bits	28 × 8 bits
μPD789406A, 789416A	16 K bytes		
μPD789407A, 789417A	24 K bytes		

- Instruction execution time variable from high speed (0.4 μs at main system clock frequency of 5.0 MHz) to super low speed (122 μs at subsystem clock frequency of 32.768 kHz)
- I/O port: 43 pins
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode selectable
- LCD controller/driver
  - Segment signal: 28 pins MAX.
  - Common signal: 4 pins MAX.
  - 1/2- or 1/3-bias selectable
- 8-bit A/D converter: 7 channels (μPD789407A subseries)
- 10-bit A/D converter: 7 channels (μPD789417A subseries)
- Timer: 6 channels
  - 16-bit timer/counter : 1 channel
  - 8-bit timer/event counter : 2 channels
  - 8-bit timer/counter : 1 channel
  - Watch timer : 1 channel
  - Watchdog timer : 1 channel
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATION FIELDS

APS compact cameras, blood pressure gauges, rice cookers, etc.

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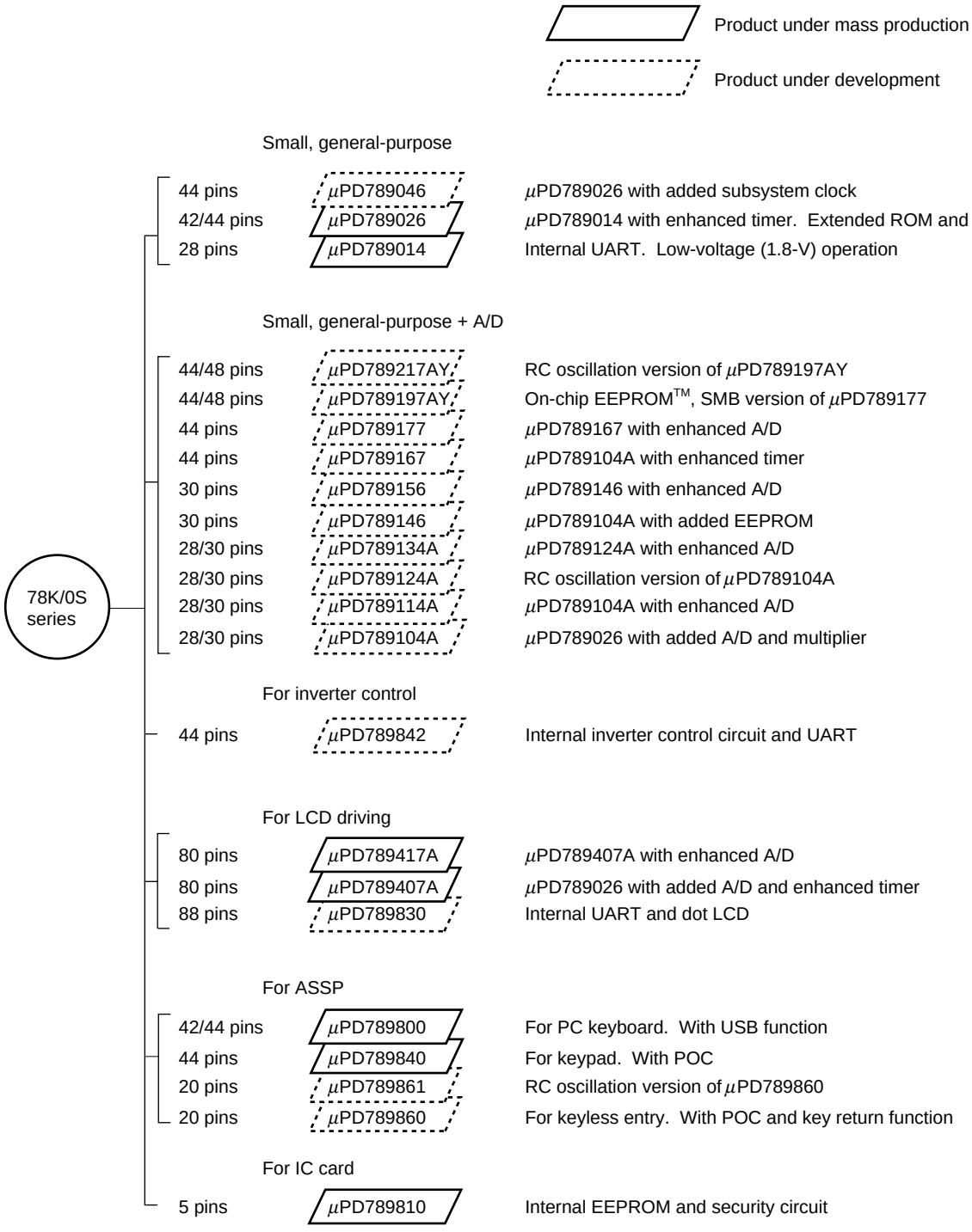
ORDERING INFORMATION

Part Number	Package
μPD7898405AGC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD7898405AGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD7898405AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD7898406AGC-×××-8BT	80-pin plastic QFP (14 x 14 mm)
μPD7898406AGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD7898406AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD7898407AGC-×××-8BT	80-pin plastic QFP (14 x 14 mm)
μPD7898407AGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD7898407AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD7898415AGC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD7898415AGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD7898415AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD7898416AGC-×××-8BT	80-pin plastic QFP (14 x 14 mm)
μPD7898416AGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD7898416AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD7898417AGC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD7898417AGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD7898417AGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)

Remark ××× indicates ROM code suffix.

DEVELOPMENT OF 78K/0S SERIES

The product development of the 78K/0S series is shown below. Subseries names are shown enclosed in a solid or dotted line.



The major differences between subseries are shown below.

Subseries Name / Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
			8-bit	16-bit	Watch	WDT						
Small, general-purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART:1 ch)	34 pins	1.8 V	–
	μPD789026	4 K-16 K			–							
	μPD789014	2 K-4 K	2 ch	–						22 pins		
Small, general-purpose + A/D	μPD789217AY	16 K-24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART : 1 ch, SMB : 1 ch)	31 pins	1.8 V	RC oscillation version, internal EEPROM
	μPD789197AY											Internal EEPROM
	μPD789177								1 ch (UART: 1 ch)			–
	μPD789167						8 ch	–				
	μPD789156	8 K-16 K	1 ch		–		–	4 ch		20 pins		Internal EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K-8 K						4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
For inverter control	μPD789842	8 K-16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30 pins	4.0 V	–
For LCD driving	μPD789417A	12 K-24 K	3 ch	1 ch	1 ch	1 ch	–	7 ch	1 ch (UART: 1 ch)	43 pins	1.8 V	–
	μPD789407A						7 ch	–				
	μPD789830	24 K	1 ch				–			30 pins	2.7 V	
ASSP	μPD789800	8 K	2 ch	1 ch	–	1 ch	–	–	2 ch (USB: 1 ch)	31 pins	4.0 V	–
	μPD789840						4 ch		1 ch	29 pins	2.8 V	
	μPD789861	4 K		–			–		–	14 pins	1.8 V	RC oscillation version
	μPD789860											–
For IC card	μPD789810	6 K	–	–	–	1 ch	–	–	–	1 pin	2.7 V	Internal EEPROM

Note 10-bit timer: 1 channel

FUNCTIONAL OUTLINE

Item		μPD789405A μPD789415A	μPD789406A μPD789416A	μPD789407A μPD789417A
Internal memory	ROM	12K bytes	16K bytes	24K bytes
	High-speed RAM	512 bytes		
	LCD display RAM	28 bytes		
Minimum instruction execution time		0.4 μs/1.6 μs (main system clock: 5.0 MHz) 122 μs (subsystem clock: 32.768 kHz)		
General-purpose register		8 bits × 8 registers		
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.		
I/O port		Total : 43 pins • CMOS input : 7 pins • CMOS I/O : 32 pins • N-ch open-drain (12 V) : 4 pins		
A/D converter		• 8-bit resolution × 7 channels (μPD789407A subseries) • 10-bit resolution × 7 channels (μPD789417A subseries)		
Comparator		Timer output controllable		
Serial interface		3-wire serial I/O mode/UART mode selectable: 1 channel		
LCD controller/driver		• Segment signal output : 28 pins MAX • Common signal output : 4 pins MAX • 1/2 or 1/3 bias selectable		
Timer		• 16-bit timer/counter : 1 channel • 8-bit timer/counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel		
Timer output		2 pins		
Vectored interrupt source	Maskable	Internal: 12, external: 4		
	Non-maskable	Internal: 1		
Supply voltage		V_{DD} = 1.8 to 5.5 V		
Operating temperature		T_A = –40 to +85 °C		
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)		

TABLE OF CONTENTS

1. PIN CONFIGURATION (Top View)

- 80-pin plastic QFP (14 x 14 mm)

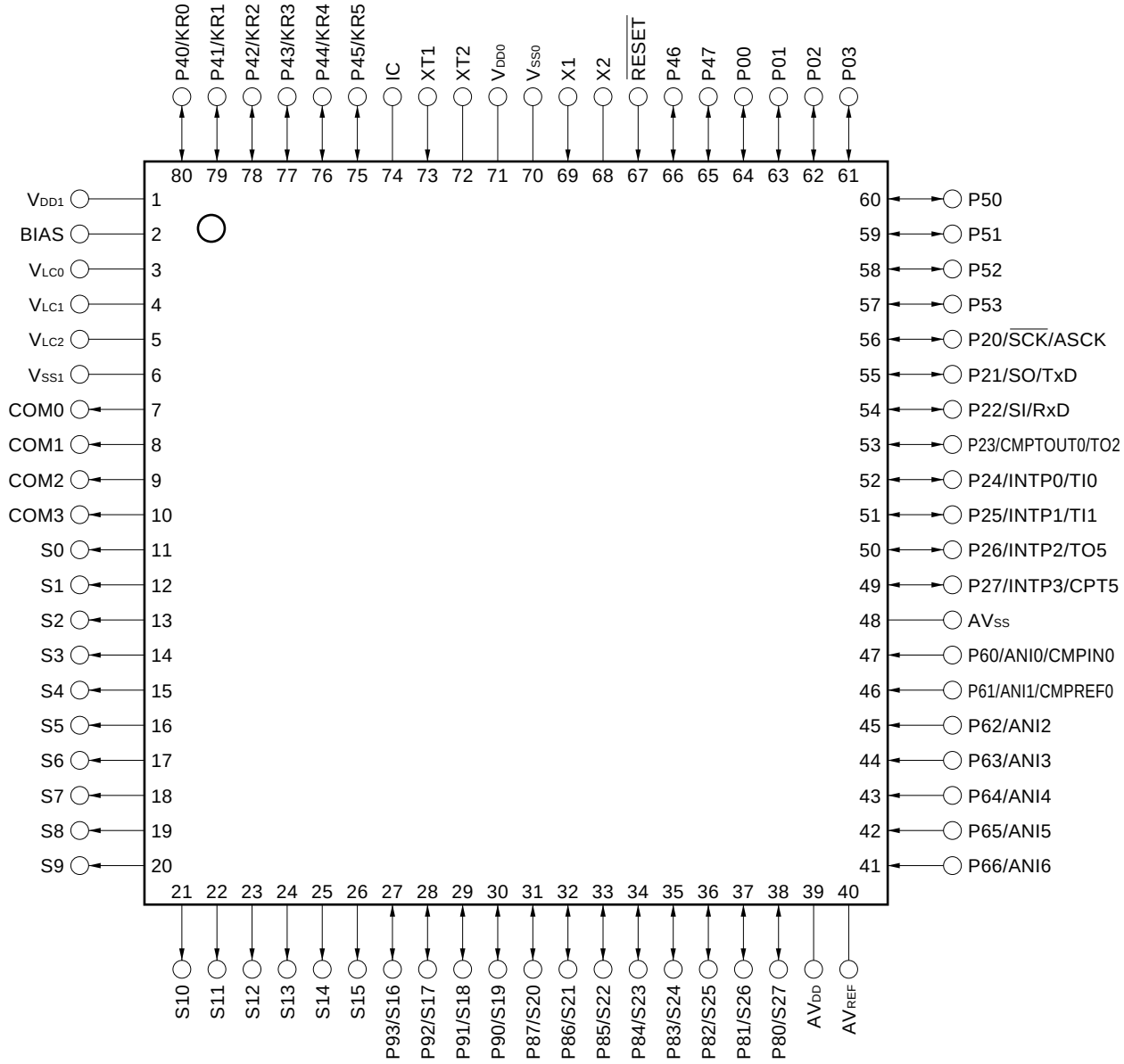
μPD789405AGC-×××-8BT
μPD789406AGC-×××-8BT
μPD789407AGC-×××-8BT
μPD789415AGC-×××-8BT
μPD789416AGC-×××-8BT
μPD789417AGC-×××-8BT

- 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)

μPD789405AGK-×××-BE9
μPD789406AGK-×××-BE9
μPD789407AGK-×××-BE9
μPD789415AGK-×××-BE9
μPD789416AGK-×××-BE9
μPD789417AGK-×××-BE9

- 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)

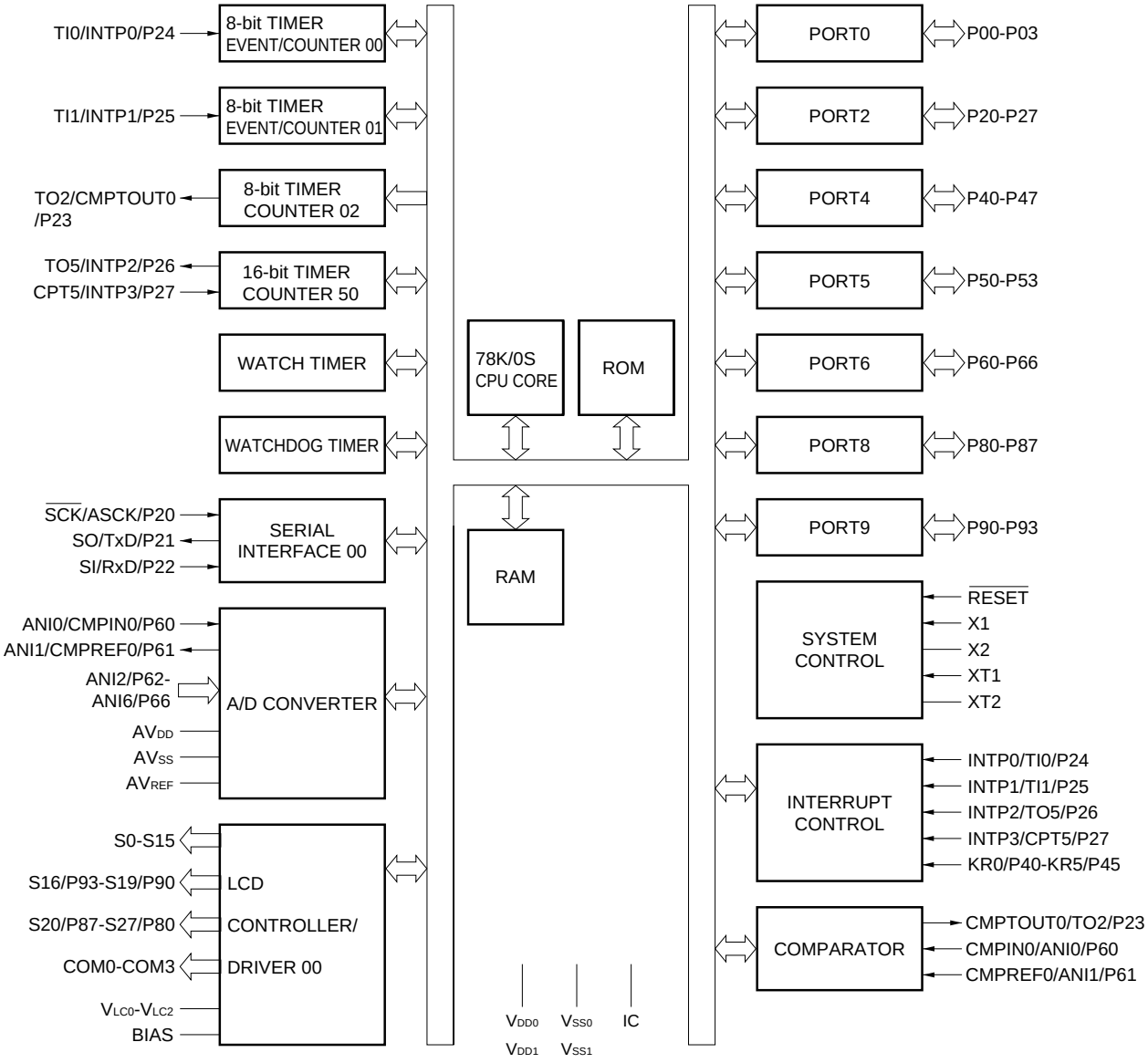
μPD789405AGK-×××-9EU
μPD789406AGK-×××-9EU
μPD789407AGK-×××-9EU
μPD789415AGK-×××-9EU
μPD789416AGK-×××-9EU
μPD789417AGK-×××-9EU



Caution Directly connect the IC (Internally Connected) pins to the V_{SS0} or V_{SS1} pin.

ANI0-ANI6 : Analog Input
ASCK : Asynchronous Serial Input
AV_{DD} : Analog Power Supply
AV_{REF} : Analog Reference Voltage
AV_{SS} : Analog Ground
BIAS : LCD Power Supply Bias Control
CMPIN0 : Comparator Input
CMPREF0 : Comparator Reference
CMPTOUT0 : Comparator Output
COM0-COM3 : Common Output
CPT5 : Capture Trigger Input
IC : Internally Connected
INTP0-INTP3 : Interrupt from Peripherals
KR0-KR5 : Key Return
P00-P03 : Port0
P20-P27 : Port2
P40-P47 : Port4
P50-P53 : Port5
P60-P66 : Port6
P80-P87 : Port8
P90-P93 : Port9
$\overline{RESET}$: Reset
RxD : Receive Data
S0-S27 : Segment Output
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output
TI0, TI1 : Timer Input
TO2, TO5 : Timer Output
TxD : Transmit Data
V_{DD0}, V_{DD1} : Power Supply
V_{LC0}-V_{LC2} : LCD Power Supply
V_{SS0}, V_{SS1} : Ground
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM capacity differs depending on the model.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	At Reset	Multiplexed by:
P00-P03	I/O	Port 0. 4-bit I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.	Input	–
P20	I/O	Port 2. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.	Input	$\overline{\text{SCK}}$/ASCK
P21				SO/TxD
P22				SI/RxD
P23				CMPTOUT0/TO2
P24				INTP0/TI0
P25				INTP1/TI1
P26				INTP1/TO5
P27				INTP3/CPT5
P40-P45	I/O	Port 4. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.	Input	KR0-KR5
P46, P47				–
P50-P53	I/O	Port 5. 4-bit N-ch open-drain I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected by mask option.	Input	–
P60	Input	Port 6. 7-bit input port.	Input	ANI0/CMPIN0
P61				ANI1/CMPREF0
P62-P66				ANI2-ANI6
P80-P87	I/O	Port 8. 8-bit I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.	Input	S27-S20
P90-P93	I/O	Port 9. 4-bit I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.	Input	S19-S16

3.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Function	At Reset	Multiplexed by:
INTP0	Input	External interrupt input whose valid edge can be specified (rising, falling, or both rising and falling edges)	Input	P24/TI0
INTP1				P25/TI1
INTP2				P26/TO5
INTP3				P27/CPT5
KR0-KR5	Input	Key return signal detection	Input	P40-P45
SI	Input	Serial data input of serial interface	Input	P22/RxD
SO	Output	Serial data output of serial interface	Input	P21/TxD
$\overline{SCK}$	I/O	Serial clock input/output of serial interface	Input	P20/ASCK
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK}$
RxD	Input	Serial data input for asynchronous serial interface	Input	P22/SI
TxD	Output	Serial data output for asynchronous serial interface	Input	P21/SO
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P24/INTP0
TI1	Input	External count clock input to 8-bit timer (TM01)	Input	P25/INTP1
TO2	Output	8-bit timer (TM02) output	Input	P23/CMPTOUT0
TO5	Output	16-bit timer (TM50) output	Input	P26/INTP2
CPT5	Input	Capture edge input	Input	P27/INTP3
CMPTOUT0	Output	Comparator output	Input	P23/TO2
CMPIN0	Input	Comparator input	Input	P60/ANI0
CMPREF0	Input	Comparator reference voltage input	Input	P61/ANI1
ANI0	Input	Analog input for A/D converter	Input	P60/CMPIN0
ANI1				P61/CMPREF0
ANI2-ANI6				P62-P66
AV_{REF}	–	Reference voltage for A/D converter	–	–
AV_{SS}	–	Ground for A/D converter	–	–
AV_{DD}	–	Analog power for A/D converter	–	–
S0-S15	Output	Segment signal output of LCD controller/driver	Output	–
S16-S19			Input	P93-P90
S20-S27				P87-P80
COM0-COM3	Output	Common signal output of LCD controller/driver	Output	–
V_{LC0}-V_{LC2}	–	LCD driving voltage	–	–
BIAS	–	Supply voltage for LCD driving	–	–
X1	Input	Connection of crystal for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connection of crystal for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–

3.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Function	At Reset	Multiplexed by:
V_{DD0}	–	Positive power supply for ports	–	–
V_{DD1}	–	Positive power supply (except ports)	–	–
V_{SS0}	–	Ground for ports	–	–
V_{SS1}	–	Ground (except ports)	–	–
IC	–	Internally connected. Must be directly connected to V_{SS0} or V_{SS1}.	–	–

3.3 I/O Circuit Type of Each Pin and Recommended Connections of Unused Pins

Table 3-1 shows the I/O circuit type of each pin and recommended connections of unused pins.
For the configuration of the circuit of each type, refer to Figure 3-1.

Table 3-1. I/O Circuit Type of Each Pin and Recommended Connections of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00-P03	5-H	I/O	Input : Individually connected to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via resistor. Output : Open.
P20/$\overline{SCK}$/ASCK	8-C		
P21/SO/TxD			
P22/SI/RxD			
P23/CMPTOUT0/TO2	10-B		
P24/INTP0/TI0	8-C		
P25/INTP1/TI1			
P26/INTP2/TO5			
P27/INTP3/CPT5			
P40/KR0-P45/KR5			
P46, P47	5-H		
P50-P53	13-U		Input : Individually connected to V_{DD0} or V_{DD1} via resistor. Output : Open.
P60/ANI0/CMPIN0	9-D	Input	Directly connected to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
P61/ANI1/CMPREF0			
P62/ANI2-P66/ANI6	9-C		
P80/S27-P87/S20	17-F	I/O	Input : Individually connected to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via resistor. Output : Open.
P90/S19-P93/S16			
S0-S15	17-B	Output	Open.
COM0-COM3	18-A		
V_{LC0}-V_{LC2}	–	–	
BIAS			Open (If all V_{LC0} through V_{LC2} are unused, however, individually connect them to V_{SS0} or V_{SS1} via resistor).
XT1		Input	Connected to V_{SS0} or V_{SS1}.
XT2		–	Open.
$\overline{RESET}$	2	Input	–
IC	–	–	Directly connected to V_{SS0} or V_{SS1}.

Figure 3-1. I/O Circuit Type of Each Pin (1/2)

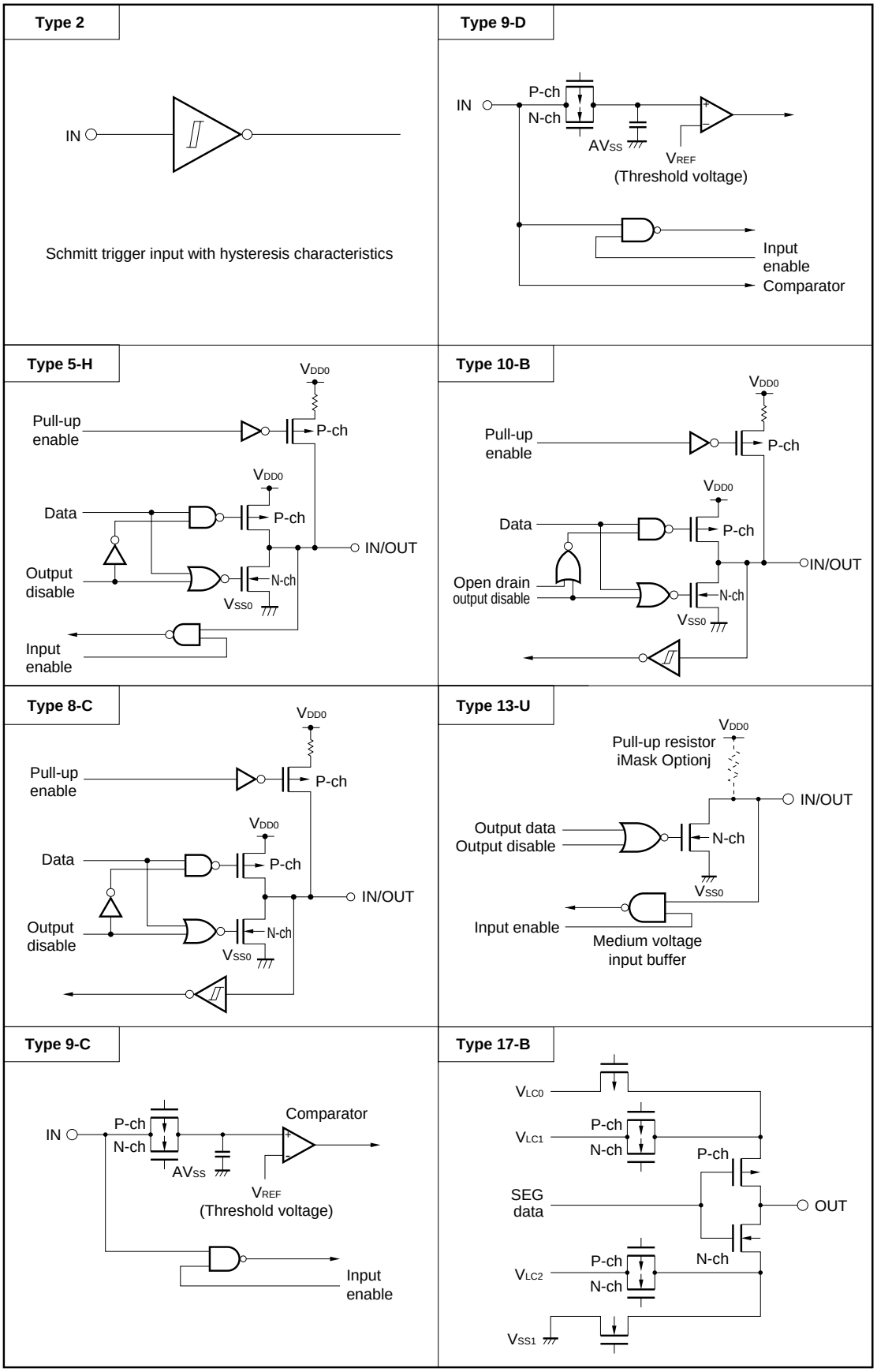
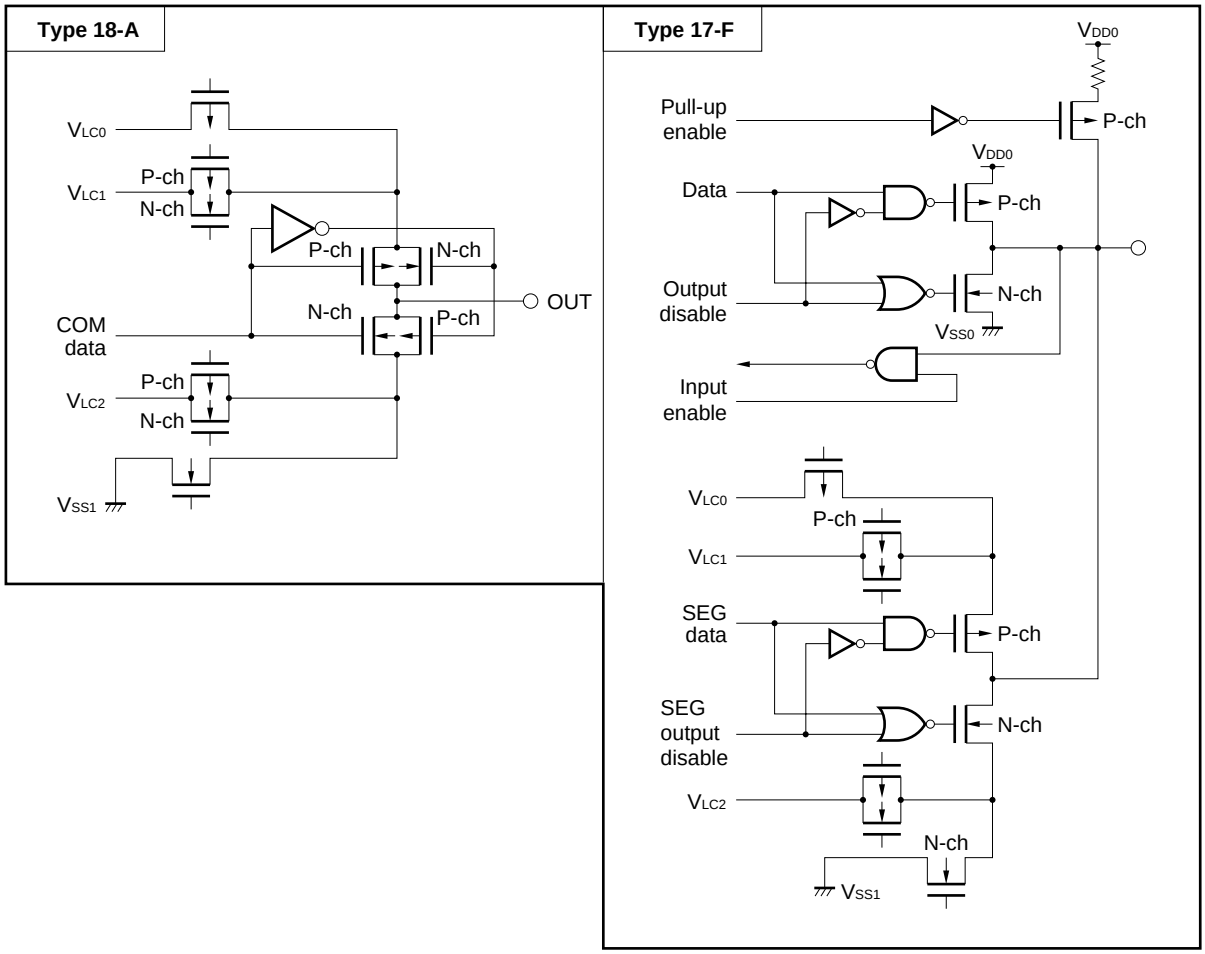


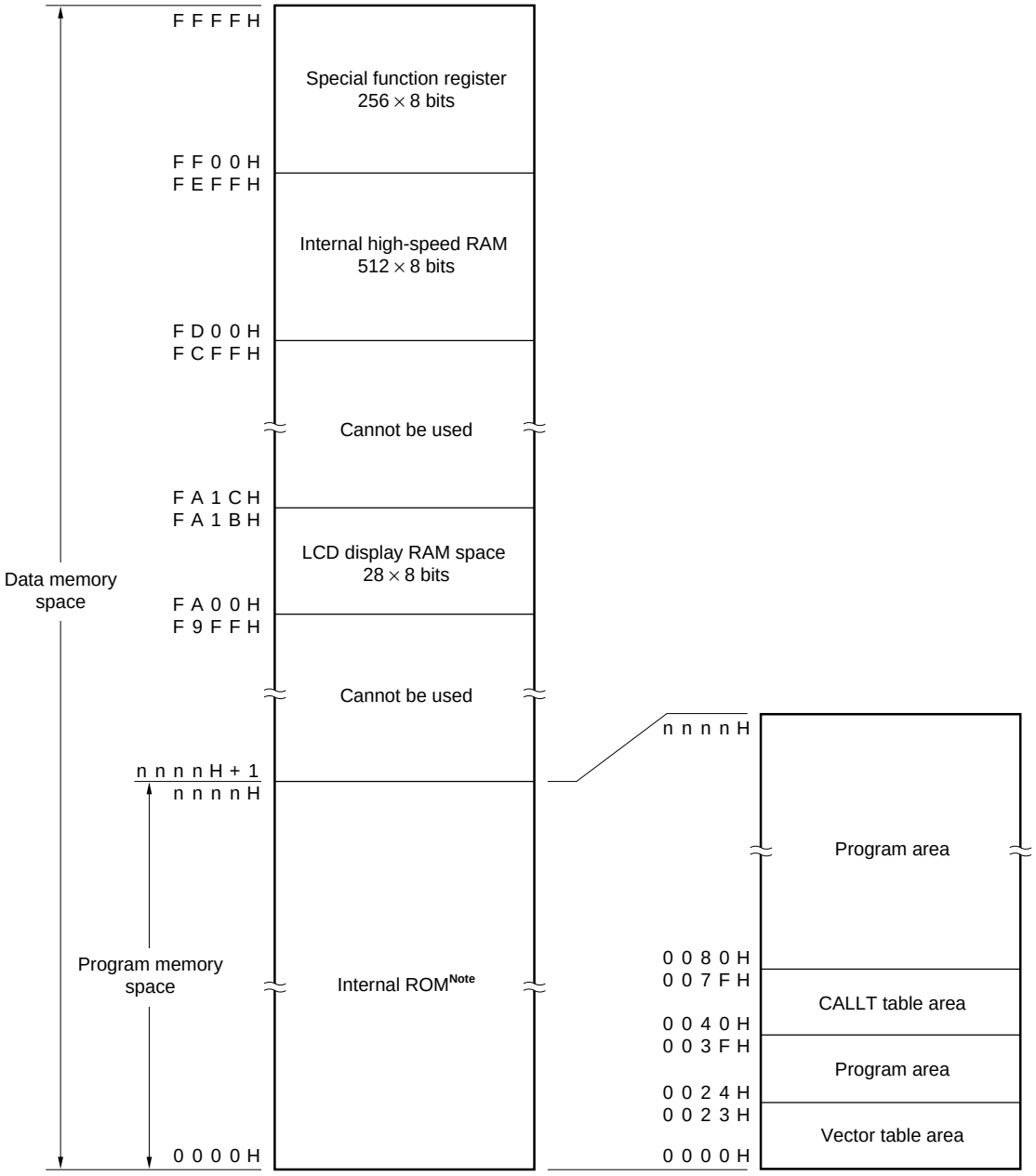
Figure 3-1. I/O Circuit Type of Each Pin (2/2)



4. MEMORY SPACE

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A can access 64K bytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The internal memory capacity differs depending on the model (refer to the table below).

Part Number	Internal ROM End Address nnnnH
μPD789405A, 789415A	2FFFH
μPD789406A, 789416A	3FFFH
μPD789407A, 789417A	5FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following I/O ports are available:

- CMOS I/O : 32 pins
- CMOS input : 7 pins
- N-ch open-drain I/O : 4 pins

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00-P03	I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.
Port 2	P20-P27	I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.
Port 4	P40-P47	I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.
Port 5	P50-P53	I/O port. Can be set in input or output mode in 1-bit units. Internal pull-up resistor can be connected by mask option.
Port 6	P60-P66	Input port
Port 8	P80-P87	I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.
Port 9	P90-P93	I/O port. Can be set in input or output mode in 1-bit units. When used as input port, internal pull-up resistor can be connected via software.

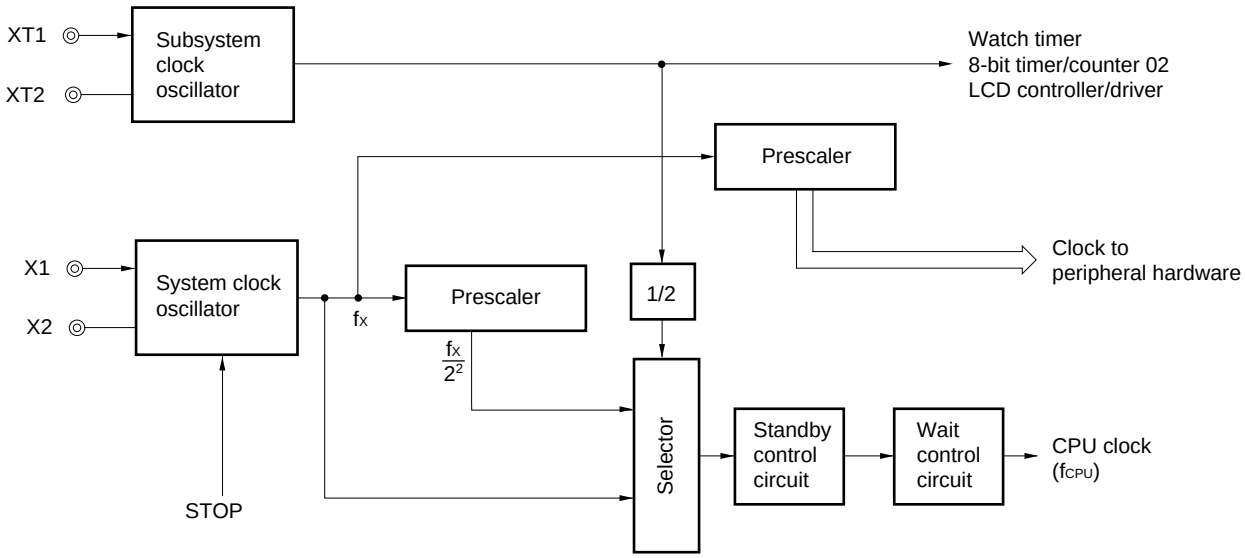
5.2 Clock Generation Circuit

A circuit that generates a system clock is provided.

Moreover, the minimum instruction execution time can be changed as follows:

- 0.4 μs/1.6 μs (main system clock: 5.0 MHz)
- 122 μs (subsystem clock: 32.768 kHz)

Figure 5-1. Block Diagram of Clock Generation Circuit



5.3 Timer

The following six timer channels are provided:

- 16-bit timer/counter (TM50) : 1 channel
- 8-bit timers/event counters (TM00 and TM01) : 2 channels
- 8-bit timer/counter (TM02) : 1 channel
- Watch timer (WT) : 1 channel
- Watchdog timer (WTM) : 1 channel

Table 5-2. Timer Operation

		TM50	TM00	TM01	TM02	WT	WTM
Operation mode	Interval timer	1 channel	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	–	1 channel	1 channel	–	–	–
Function	Timer output	1 output	1 output	1 output	1 output	–	–
	Square wave output	–	1 output	1 output	1 output	–	–
	Interrupt request	1	1	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer/Counter 50

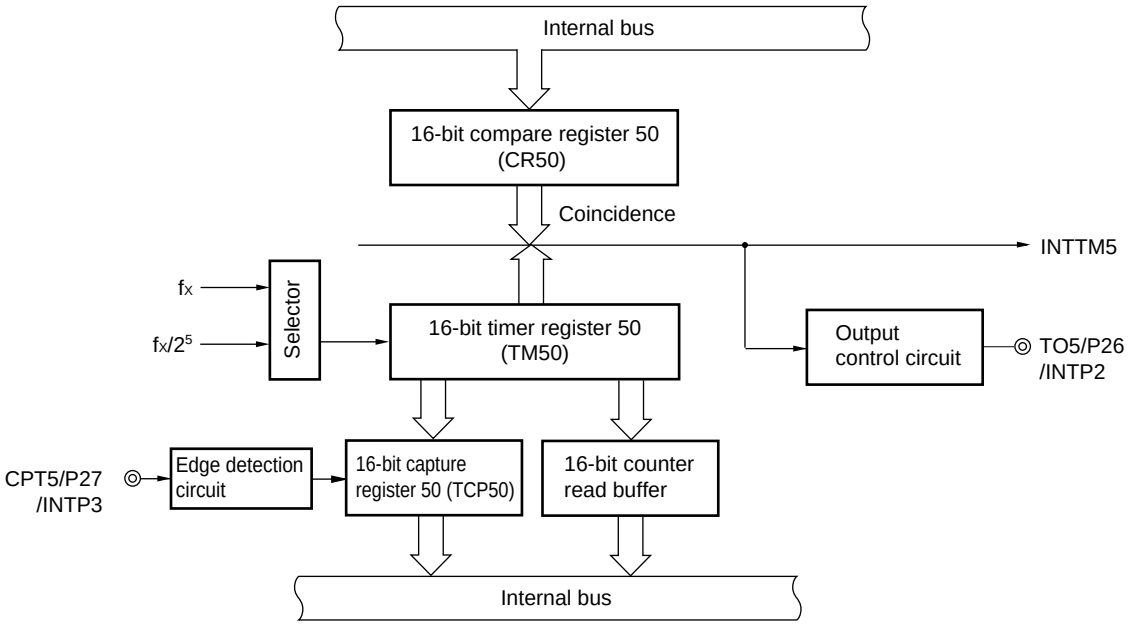


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 00

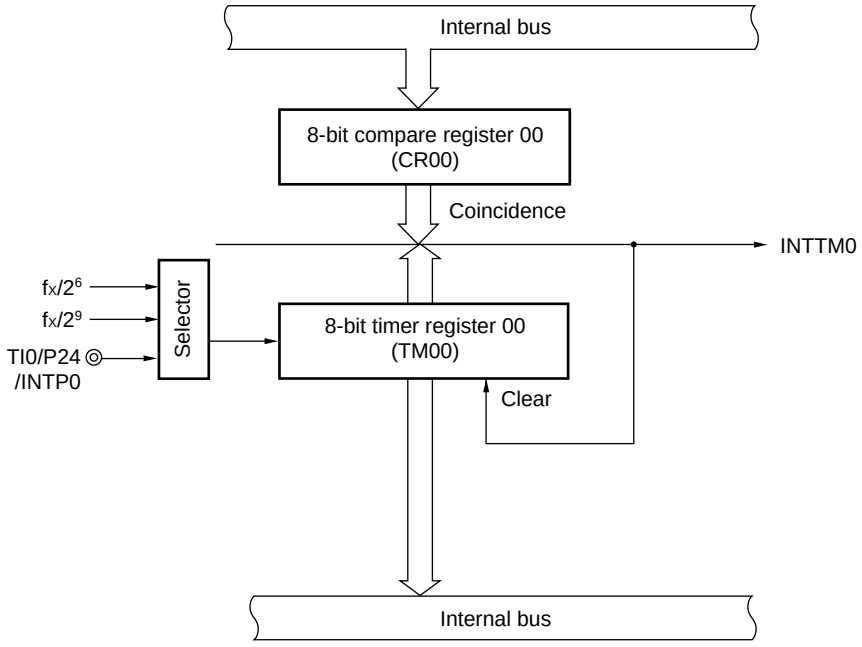


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 01

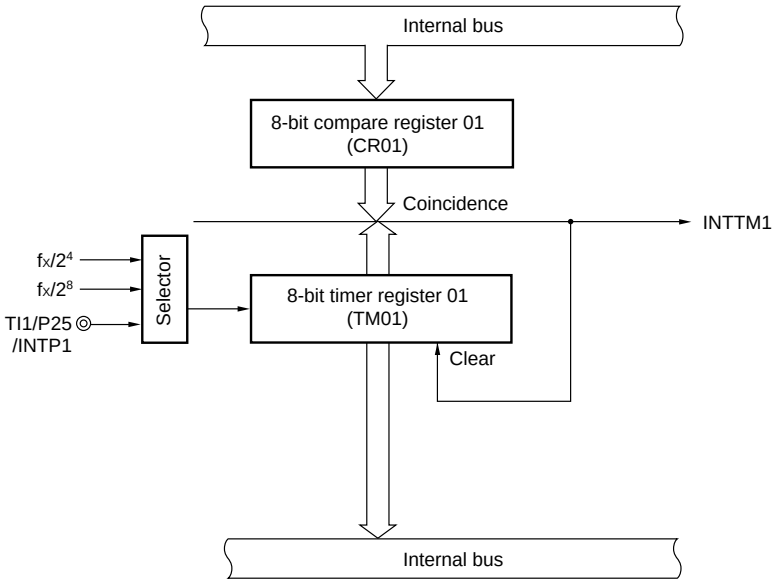


Figure 5-5. Block Diagram of 8-Bit Timer/Counter 02

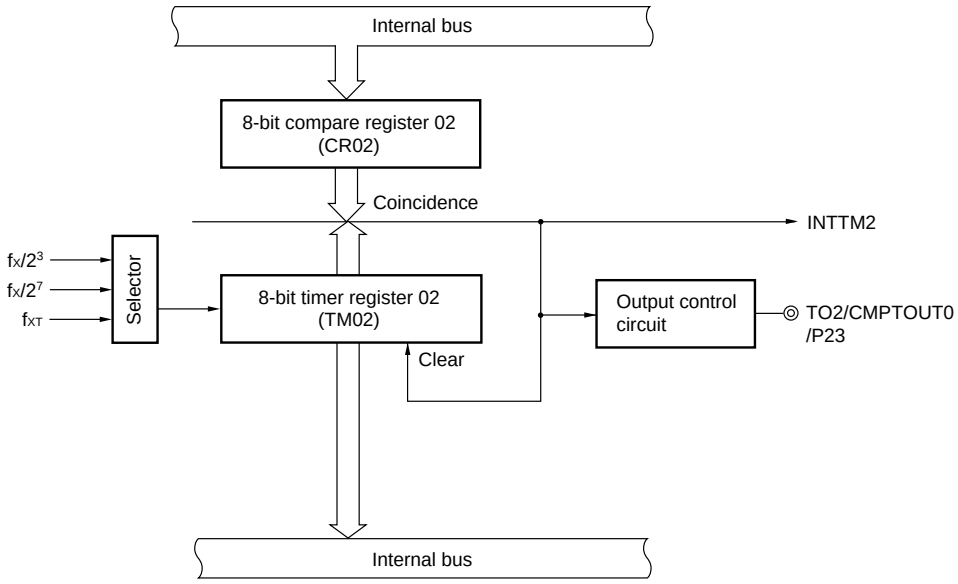


Figure 5-6. Block Diagram of Watch Timer

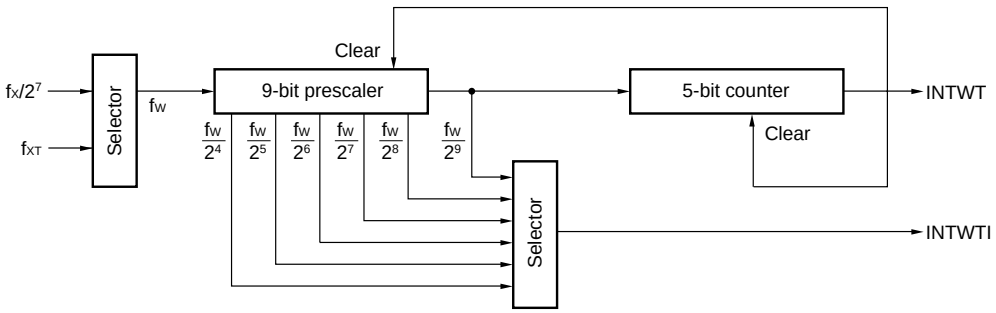
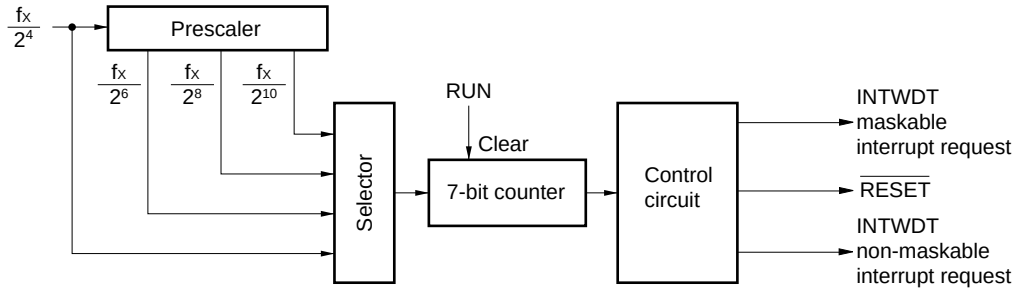


Figure 5-7. Block Diagram of Watchdog Timer



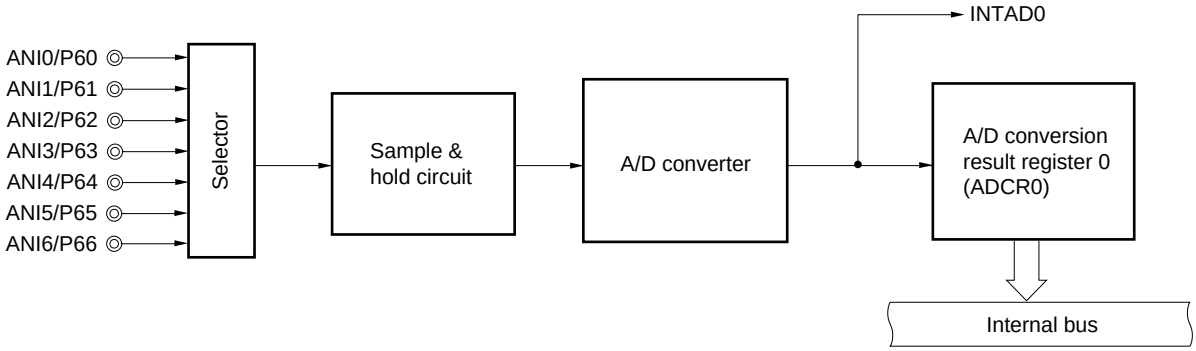
5.4 A/D Converter

The resolution of the A/D converter differs depending on the model as follows:

- 8-bit A/D converter ... μPD789407A subseries
- 10-bit A/D converter ... μPD789417A subseries

A/D conversion can be started only by means of a software start.

Figure 5-8. Block Diagram of A/D Converter

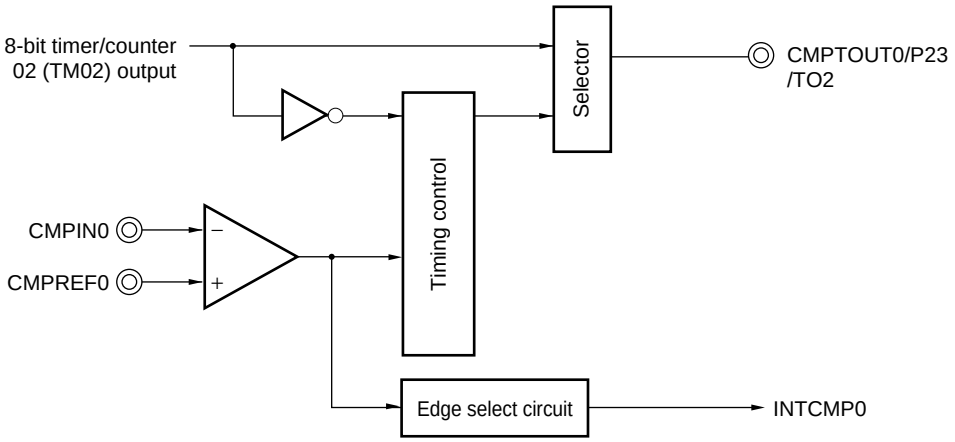


5.5 Comparator

A comparator with the following functions is provided:

- The input voltage of the reference voltage input pin (CMPREF0) is compared with the input voltage of the comparator input pin (CMPIN0). The result of the comparison can be read by using a memory manipulation instruction.
- The output of the comparator can be used to generate an interrupt request signal (INTCMP0).
- If CMPREF0 > CMPIN0, the output signal of the 8-bit timer/counter 02 (TM02) is output to the CMPTOUT0 pin.

Figure 5-9. Block Diagram of Comparator



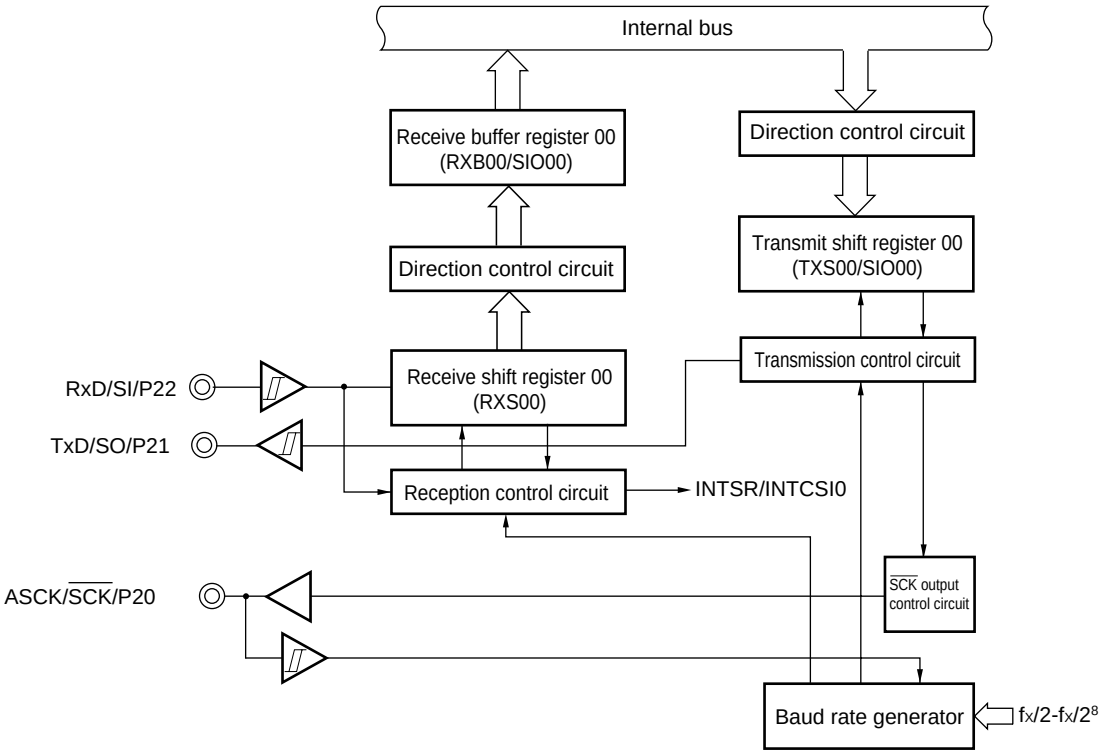
5.6 Serial Interface

One serial interface channel, serial interface 00, is provided.

Serial interface 00 has the following two modes:

- 3-wire serial I/O mode : MSB/LSB first selectable
- Asynchronous serial interface (UART) mode : Dedicated internal baud generator

Figure 5-10. Block Diagram of Serial Interface

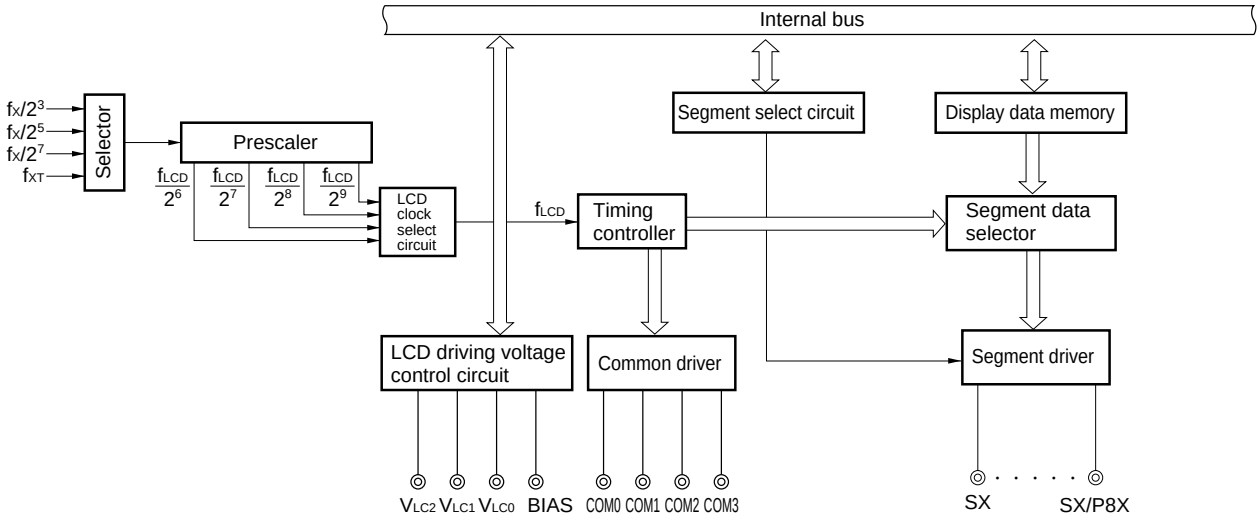


5.7 LCD Controller/Driver

An LCD controller/driver with the following functions is provided:

- Five display modes selectable
- Four frame frequencies selectable in each display mode
- Twelve segment signal output pins can be used as I/O port pins in 2-pin units (P80/S27 through P87/S20 and P90/S19 through P93/S16).
- A divider resistor for generating LCD driving voltage can be provided by mask option.

Figure 5-11. Block Diagram of LCD/Controller Driver



6. INTERRUPT FUNCTIONS

The following two types of interrupt functions and a total of 17 interrupt sources are available.

- Non-maskable : 1
- Maskable : 16

Table 6-1. Interrupt Sources

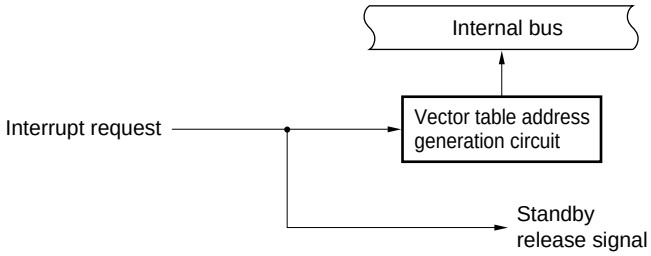
Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Detection of input edge of pin	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR00	End of UART reception of serial interface 00	Internal	000EH	(B)
		INTCSI00	End of 3-wire SIO transfer/reception of serial interface 00			
	6	INTST00	End of UART transmission of serial interface 00		0010H	
	7	INTWT	Watch timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM00	Coincidence signal generation of 8-bit timer/event counter 00		0016H	
	10	INTTM01	Coincidence signal generation of 8-bit timer/event counter 01		0018H	
	11	INTTM02	Coincidence signal generation of 8-bit timer/counter 02		001AH	
	12	INTTM50	Coincidence signal generation of 16-bit timer/counter 50		001CH	
	13	INTKR00	Detection of key return signal	External	001EH	(C)
	14	INTAD0	A/D conversion end signal	Internal	0020H	(B)
	15	INTCMP0	Comparator signal		0022H	

Notes 1. If two or more maskable interrupts occur at the same time, they are processed according to these priorities. Priority 0 is the highest, while 15 is the lowest.

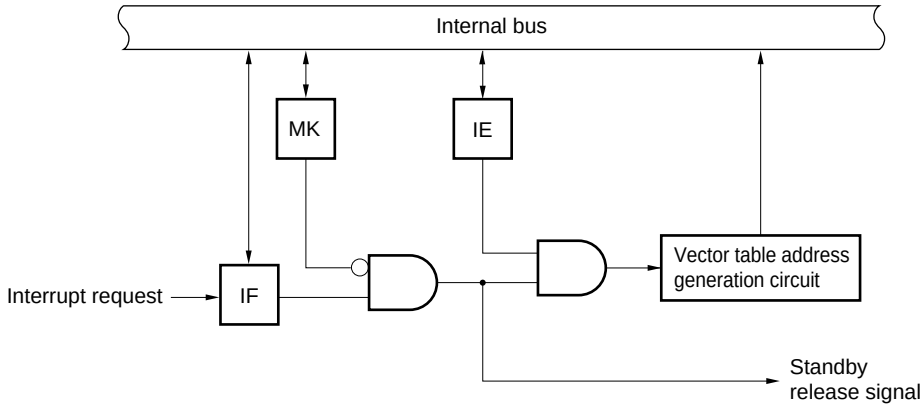
2. (A) through (C) in Basic Configuration Type correspond to (A) through (C) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function

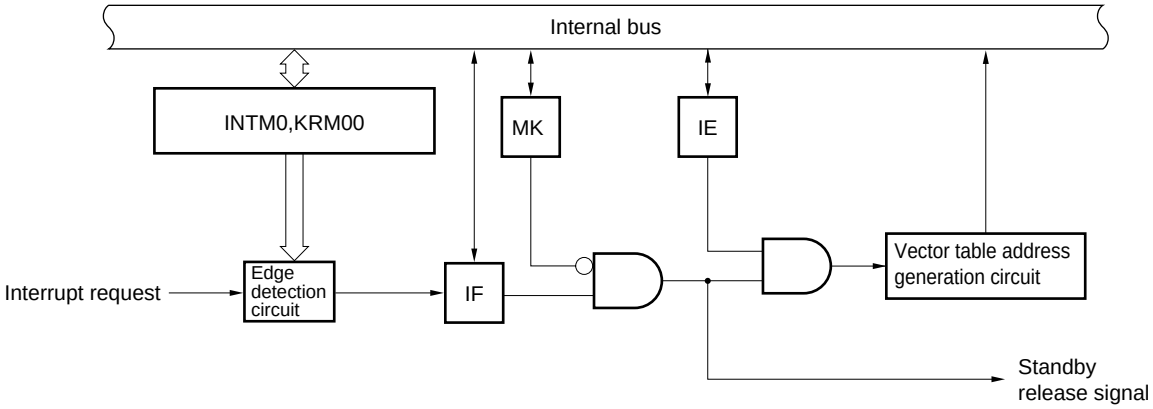
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



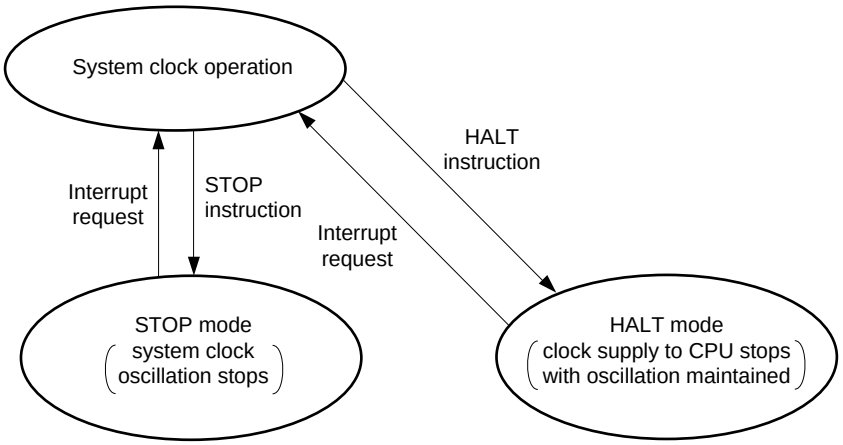
INTM0 : External interrupt mode register 0
KRM00 : Key return mode register 00
IF : Interrupt request flag
IE : Interrupt enable flag
MK : Interrupt mask flag

7. STANDBY FUNCTION

The standby function is used to lower the current consumption and can be used in the following two modes:

- HALT mode: In this mode, the operation of the CPU clock is stopped. By using this mode together with the normal operation mode to operate the system intermittently, the average current consumption can be reduced.
- STOP mode: In this mode, the oscillation of the system clock is stopped, so that all internal operations based on the system clock are stopped and the current consumption is minimized.

Figure 7-1. Standby Function



8. RESET FUNCTION

The microcontroller can be reset in the following two ways:

- External reset by using the $\overline{\text{RESET}}$ pin
- Internal reset by detecting hang-up of watchdog timer

9. MASK OPTION

The μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A have the following mask options:

- Mask option of P50 through P53
  Connection of a pull-up resistor can be selected.

- Mask option of V_{LC0} through V_{LC2} pins and BIAS pin
  Connection of divider resistor for LCD driving can be selected.

For the values of the pull-up resistor and divider resistor for LCD driving, refer to **11. ELECTRICAL SPECIFICATIONS**.

10. OUTLINE OF INSTRUCTION SET

This section shows a list of the instructions of the μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A.

10.1 Conventions

10.1.1 Operand Formats and Syntax

One or more operands are written in the operand field of each instruction in accordance with the operand format and syntax of that instruction (for details, refer to **the assembler specifications**). If two or more operands are shown, select one of them. The uppercase characters, and the symbols #, !, $, [, and] are keywords and must be written as shown. The meanings of these symbols are as follows:

- # : Specifies immediate data.
- ! : Specifies an absolute address.
- $: Specifies a relative address.
- [ ] : Specifies an indirect address.

To specify immediate data, write an appropriate value or label. When using a label, be sure to use the symbols #, !, $, [, and].

The register syntax operands r and rp can be specified as either a function name (such as X, A, and C) or an absolute name (such as R0, R1, and R1 as shown in the parentheses in the table below).

Table 10-1. Operand Formats and Syntax

Format	Syntax
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH Immediate data or label
saddrp	FE20H to FF1FH Immediate data or label (even address only)
addr16	0000H to FFFFH Immediate data or label (even address only when 16-bit data transfer instruction is used)
addr5	0040H to 007FH Immediate data or label (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

10.1.2 Explanation of symbols in operation field

A : A register; 8-bit accumulator
X : X register
B : B register
C : C register
D : D register
E : E register
H : H register
L : L register
AX : AX register pair; 16-bit accumulator
BC : BC register pair
DE : DE register pair
HL : HL register pair
PC : Program counter
SP : Stack pointer
PSW : Program status word
CY : Carry flag
AC : Auxiliary carry flag
Z : Zero flag
IE : Interrupt request enable flag
NMIS : Non-maskable interrupt processing flag
( ) : Contents of memory addressed by address or register contents in ( )
X_H, X_L : High-order 8 bits and low-order 8 bits of 16-bit register
∧ : Logical product (AND)
∨ : Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
$\overline{\quad}$: Inverted data
addr16 : 16-bit immediate data or label
jdisp8 : Signed 8-bit data (displacement value)

10.1.3 Explanation of symbols in flag operation field

(Blank) : Not affected
0 : Cleared to 0
1 : Set to 1
× : Set or cleared depending on result
R : Previously saved value is stored.

10.2 Operation List

Mnemonic	Operand	Bytes	Clocks	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r←byte			
	saddr, #byte	3	6	(saddr)←byte			
	sfr, #byte	3	6	sfr←byte			
	A, r Note 1	2	4	A←r			
	r, A Note 1	2	4	r←A			
	A, saddr	2	4	A←(saddr)			
	saddr, A	2	4	(saddr)←A			
	A, sfr	2	4	A←sfr			
	sfr, A	2	4	sfr←A			
	A, !addr16	3	8	A←(addr16)			
	!addr16, A	3	8	(addr16)←A			
	PSW, #byte	3	6	PSW←byte	×	×	×
	A, PSW	2	4	A←PSW			
	PSW, A	2	4	PSW←A	×	×	×
	A, [DE]	1	6	A←(DE)			
	[DE], A	1	6	(DE)←A			
	A, [HL]	1	6	A←(HL)			
	[HL], A	1	6	(HL)←A			
	A, [HL+byte]	2	6	A←(HL+byte)			
	[HL+byte], A	2	6	(HL+byte)←A			
XCH	A, X	1	4	A↔X			
	A, r Note 2	2	6	A↔r			
	A, saddr	2	6	A↔(saddr)			
	A, sfr	2	6	A↔(sfr)			
	A, [DE]	1	8	A↔(DE)			
	A, [HL]	1	8	A↔(HL)			
	A, [HL+byte]	2	8	A↔(HL+byte)			
MOVW	rp, #word	3	6	rp←word			
	AX, saddrp	2	6	AX←(saddrp)			
	saddrp, AX	2	8	(saddrp)←AX			
	AX, rp Note 3	1	4	AX←rp			
	rp, AX Note 3	1	4	rp←AX			
XCHW	AX, rp Note 3	1	8	AX↔rp			

Notes 1. Except r = A

2. Except r = A, X

3. rp = BC, DE, or HL only

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY←A+byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte	×	×	×
	A, r	2	4	A, CY←A+r	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)	×	×	×
ADDC	A, #byte	2	4	A, CY←A+byte+CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte+CY	×	×	×
	A, r	2	4	A, CY←A+r+CY	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)+CY	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)+CY	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)+CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)+CY	×	×	×
SUB	A, #byte	2	4	A, CY←A–byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte	×	×	×
	A, r	2	4	A, C←A–r	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)	×	×	×
	A, !addr16	3	8	A, CY← A–(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)	×	×	×
SUBC	A, #byte	2	4	A, CY←A–byte–CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte–CY	×	×	×
	A, r	2	4	A, CY←A–r–CY	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)–CY	×	×	×
	A, !addr16	3	8	A, CY←A–(addr16)–CY	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)–CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)–CY	×	×	×
AND	A, #byte	2	4	A←A∧byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∧byte	×		
	A, r	2	4	A←A∧r	×		
	A, saddr	2	4	A←A∧(saddr)	×		
	A, !addr16	3	8	A←A∧(addr16)	×		
	A, [HL]	1	6	A←A∧(HL)	×		
	A, [HL+byte]	2	6	A←A∧(HL+byte)	×		

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A←A∨byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∨byte	×		
	A, r	2	4	A←A∨r	×		
	A, saddr	2	4	A←A∨ (saddr)	×		
	A, !addr16	3	8	A←A∨(addr16)	×		
	A, [HL]	1	6	A←A∨(HL)	×		
	A, [HL+byte]	2	6	A←A∨(HL+byte)	×		
XOR	A, #byte	2	4	A←A⊻byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)⊻byte	×		
	A, r	2	4	A←A⊻r	×		
	A, saddr	2	4	A←A⊻(saddr)	×		
	A, !addr16	3	8	A←A⊻(addr16)	×		
	A, [HL]	1	6	A←A⊻(HL)	×		
	A, [HL+byte]	2	6	A←A⊻(HL+byte)	×		
CMP	A, #byte	2	4	A–byte	×	×	×
	saddr, #byte	3	6	(saddr)–byte	×	×	×
	A, r	2	4	A–r	×	×	×
	A, saddr	2	4	A–(saddr)	×	×	×
	A, !addr16	3	8	A–(addr16)	×	×	×
	A, [HL]	1	6	A–(HL)	×	×	×
	A, [HL+byte]	2	6	A–(HL+byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY←AX+word	×	×	×
SUBW	AX, #word	3	6	AX, CY←AX–word	×	×	×
CMPW	AX, #word	3	6	AX–word	×	×	×
INC	r	2	4	r←r+1	×	×	
	saddr	2	4	(saddr)←(saddr)+1	×	×	
DEC	r	2	4	r←r–1	×	×	
	saddr	2	4	(saddr)←(saddr)–1	×	×	
INCW	rp	1	4	rp←r–1			
DECW	rp	1	4	rp←rp–1			
ROR	A, 1	1	2	(CY, A_7←A_0, A_{m-1}←A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0←A_7, A_{m+1}←A_m) × 1			×
RORC	A, 1	1	2	(CY←A_0, A_7←CY , A_{m-1}←A_m) × 1			×
ROLC	A, 1	1	2	(CY←A_7, A_0←CY , A_{m+1}←A_m) × 1			×

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit)←1			
	sfr. bit	3	6	sfr. bit←1			
	A. bit	2	4	A. bit←1			
	PSW. bit	3	6	PSW. bit←1	×	×	×
	[HL]. bit	2	10	(HL). bit←1			
CLR1	saddr. bit	3	6	(saddr. bit)←0			
	sfr. bit	3	6	sfr. bit←0			
	A. bit	2	4	A. bit←0			
	PSW. bit	3	6	PSW. bit←0	×	×	×
	[HL]. bit	2	10	(HL). bit←0			
SET1	CY	1	2	CY←1			1
CLR1	CY	1	2	CY←0			0
NOT1	CY	1	2	CY←$\overline{CY}$			×
CALL	!addr16	3	6	(SP−1)←(PC+3)$_H$, (SP−2)←(PC+3)$_L$, PC←addr16, SP←SP−2			
CALLT	[addr5]	1	8	(SP−1)←(PC+1)$_H$, (SP−2)←(PC+1)$_L$, PC$_H$←(00000000, addr5+1), PC$_L$←(00000000, addr5), SP←SP−2			
RET		1	6	PC$_H$, (SP+1), PC$_L$←(SP), SP←SP+2			
RETI		1	8	PC$_H$, (SP+1), PC$_L$←(SP), PSW←(SP+2), SP←SP+3, NMIS←0	R	R	R
PUSH	PSW	1	2	(SP−1)←PSW, SP←SP−1			
	rp	1	4	(SP−1)←rp$_H$, (SP−2)←rp$_L$, SP←SP−2			
POP	PSW	1	4	PSW←(SP), SP←SP+1	R	R	R
	rp	1	6	rp$_H$←(SP+1), rp$_L$← (SP), SP←SP+2			
MOVW	SP, AX	2	8	SP←AX			
	AX, SP	2	6	AX←SP			
BR	!addr16	3	6	PC←addr16			
	$addr16	2	6	PC←PC+2+jdisp8			
	AX	1	6	PC$_H$←A, PC$_L$←2			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 1	
BNC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 0	
BZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 1	
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B←B–1, then PC←PC+2+jdisp8 if B≠0	
	C, $addr16	2	6	C←C–1, then PC←PC+2+jdisp8 if C≠0	
	saddr, $addr16	3	8	(saddr)←(saddr)–1, then PC←PC+3+jdisp8 if (saddr)≠0	
NOP		1	2	No Operation	
EI		3	6	IE←1 (Enable Interrupt)	
DI		3	6	IE←0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

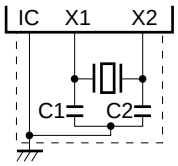
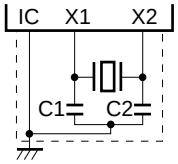
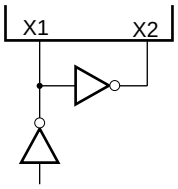
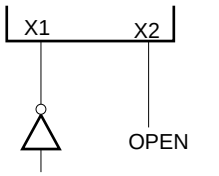
Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$		−0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le V_{DD} + 0.3\ V$			
	AV_{REF}	$AV_{REF} \le AV_{DD} + 0.3\ V$			
Input voltage	V_{I1}	Pins other than P50 through P53		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P50-P53	N-ch open drain	−0.3 to +13	V
			With pull-up resistor connected	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin		−10	mA
		Total of all pins		−30	mA
Low-level output current	I_{OL}	1 pin		30	mA
		Total of all pins		160	mA
Operating temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Remark Unless otherwise specified, the characteristics of a pin multiplexed with a port pin are the same as the port pin.

Main System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_{XT})[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} has reached MIN. of oscillation start voltage			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)[Note 1]	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. These parameters indicate only the characteristics of the oscillator. For the instruction execution time, refer to **AC Characteristics**.

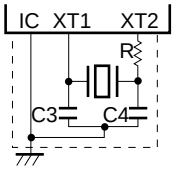
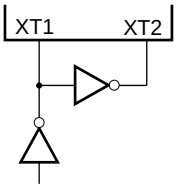
2. This is the time required for oscillation to stabilize after reset has been cleared or the STOP mode has been released. Use a resonator that stabilizes within the specified oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire the portion enclosed by the dotted line in the above figures as follows to avoid adverse influence due to wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Keep away from a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as V_{SS0}.**
- **Do not ground the wiring to a pattern through which a high current flows.**
- **Do not extract any signal from the oscillator.**

2. Make sure in software that the specified oscillation stabilization time has elapsed before the main system clock is selected again if the main system clock has been stopped and the subsystem clock is being used.

Subsystem clock oscillator characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Condition	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		14.3		15.6	μs

Notes 1. These parameters indicate only the characteristics of the oscillator. For the instruction execution time, refer to **AC Characteristics**.

2. This is the time required for oscillation to stabilize after reset has been cleared or the STOP mode has been released. Use a resonator that stabilizes within the specified oscillation wait time.

Cautions 1. When using the main system clock oscillator, wire the portion enclosed by the dotted line in the above figures as follows to avoid adverse influence due to wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Keep away from a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as V_{SS0}.**
- **Do not ground the wiring to a pattern through which a high current flows.**
- **Do not extract any signal from the oscillator.**

2. The subsystem clock oscillator is designed to have a low amplification factor in order to lower the current consumption. Consequently, it is more susceptible to noise than the main system clock oscillator. Therefore, utmost care must be exercised in wiring when using the subsystem clock oscillator.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Condition			MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}	Per pin					–1	mA
		Total of all pins					–15	mA
Low-level output current	I_{OL}	Per pin					10	mA
		Total of all pins					80	mA
High-level input voltage	V_{IH1}	P00-P03, P46, P47, P60-P66, P80-P87, P90-P93		V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
					0.9 V_{DD}		V_{DD}	V
	V_{IH2}	P50-P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		12	V
					0.9 V_{DD}		12	V
			with pull-up resistor connected	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
					0.9 V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20-P27, P40-P45		V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
					0.9 V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2			V_{DD}–0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	P00-P03, P46, P47, P60-P66, P80-P87, P90-P93		V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
					0		0.1 V_{DD}	V
	V_{IL2}	P50-P53		V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
					0		0.1 V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20-P27, P40-P45		V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
					0		0.1 V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2			0		0.1	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA			V_{DD}–1.0			V
		I_{OH} = –100 μA			V_{DD}–0.5			V
Low-level output voltage	V_{OL1}	Pins other than P50-P53		V_{DD} = 4.5 to 5.5 V I_{OL} = 10 mA			1.0	V
				I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50-P53		V_{DD} = 4.5 to 5.5 V I_{OL} = 10 mA			1.0	V
				I_{OL} = 1.6 mA			0.4	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}		Pins other than P50-P53, X1, X2, XT1, and XT2			3	μA
	I_{LIH2}			X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 12 V		P50-P53 (N-ch open drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V		Pins other than P50-P53, X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}			X1, X2, XT1, XT2			–20	μA
	I_{LIL3}			P50-P53 (N-ch open drain)			–3[Note]	μA

Note If a pull-up resistor is not connected to P50 through P53 (specified by mask option), and if P50 through P53 are set in the input mode, a low-level input leakage current of –30 μA (MAX) flows only for the duration of one cycle time if an instruction to read P50 through P53 is executed. Otherwise, the leakage current –3 μA (MAX.).

Remark Unless otherwise specified, the characteristics of a pin multiplexed with a port pin are the same as the port pin.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level output leakage current	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistance	R_1	VIN = 0 V, pins other than P50-P53		50	100	200	kΩ
Mask option pull-up resistance	R_2	VIN = 0 V, P50-P53		15	30	60	kΩ
Supply current	I_{DD1} Note 1	5.0-MHz crystal oscillation Operation mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.0	4.0	mA
			V_{DD} = 3.0 V ±10% Note 5		0.6	1.2	mA
			V_{DD} = 2.0 V ±10% Note 5		0.3	0.6	mA
	I_{DD2} Note 1	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		1.1	2.2	mA
			V_{DD} = 3.0 V ±10% Note 5		0.4	0.8	mA
			V_{DD} = 2.0 V ±10% Note 5		0.2	0.4	mA
	I_{DD3} Note 1	32.768-kHz crystal oscillation Operation mode Note 3 (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	90	μA
			V_{DD} = 3.0 V ±10%		9	50	μA
			V_{DD} = 2.0 V ±10%		4	25	μA
	I_{DD4} Note 1	32.768-kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	25	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5} Note 1	32.768-kHz crystal oscillation STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			V_{DD} = 3.0 V ±10%, T_A = 25 °C		0.05	3.0	μA
			V_{DD} = 2.0 V ±10%		0.05	3.0	μA
	I_{DD6} Notes 1, 2	5.0-MHz crystal oscillation A/D operation mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%		2.6	6.0	mA
			V_{DD} = 3.0 V ±10%		1.2	3.6	mA
			V_{DD} = 2.0 V ±10%		0.9	2.7	mA

Notes 1. Excluding AV_{REF}, A/D operation ON (ADCS0 (bit 7 of A/D converter mode register 0 (ADM0) = 1) current, AV_{DD} current, and port current (including current flowing through the internal pull-up resistor).

2. For the current flowing into AV_{REF}, refer to **8-Bit A/D Converter Characteristics** and **10-Bit A/D Converter Characteristics**.

3. When main system clock is stopped

4. In high-speed mode (when processor clock control register (PCC) is set to 00H)

5. In low-speed mode (when PCC = 02H)

Remark Unless otherwise specified, the characteristics of a pin multiplexed with a port pin are the same as the port pin.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.2 to 5.5 V)

LCD Characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAON20 = 1		2.2		V_{DD}	V
		VAON20 = 0 Note 1	At 1/3 bias	2.7		V_{DD}	V
			At 1/2 bias	3.0		V_{DD}	V
LCD divider resistance Note 2	R_{LCD1}			100	200	400	kΩ
	R_{LCD2}			10	20	40	kΩ
LCD output voltage deviation Note 3 (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$	0		±0.2	V
LCD output voltage deviation Note 3 (segment)	V_{ODS}	I_O = ±1 μA	2.2 V ≤ V_{LCD} ≤ V_{DD} $V_{LCD2} = V_{LCD} \times 1/3$ Note 1	0		±0.2	V

Notes 1. T_A = –10 to +85 °C in the normal mode (VAON20 = 0)

2. R_{LCD1}, R_{LCD2}, or no divider resistor can be selected by mask option.

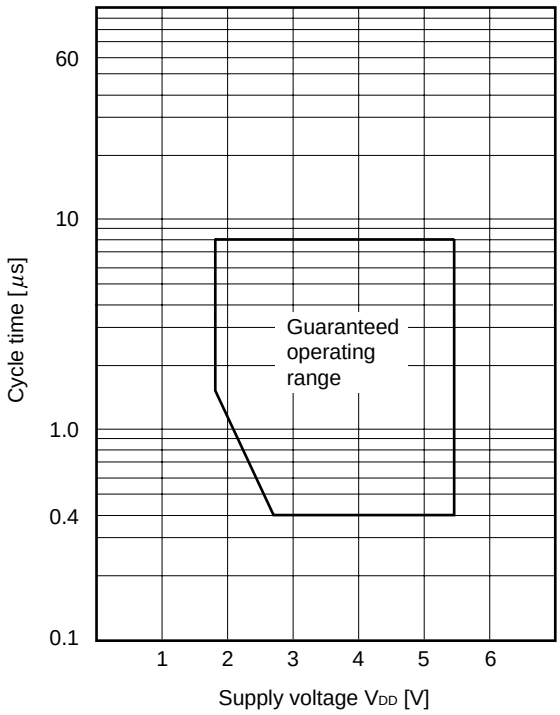
3. Voltage deviation is the voltage difference between the ideal value of a segment or the common output (V_{LCDn}: n = 0 to 2) and output voltage.

AC Characteristics

(1) Basic operation (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	With main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
				1.6		8	μs
		With subsystem clock		114	122	125	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI0, TI1 input high- and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
Interrupt input high- and low-level widths	t_{INTH}, t_{INTL}	INTP0-INTP3		10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs

T_{CY} vs V_{DD} (Main system clock)



(2) Serial interface

(a) Three-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level widths	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI setup time (vs $\overline{SCK}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI hold time (vs $\overline{SCK}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$↓→SO output delay time	t_{KSO1}	R = 1kΩ	V_{DD} = 2.7 to 5.5 V	0		250	ns
		C = 100 pF[Note]		0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(b) Three-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
				3500			ns
$\overline{SCK}$ high- and low-level widths	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI setup time (vs $\overline{SCK}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI hold time (vs $\overline{SCK}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$↓→SO output delay time	t_{KSO2}	R = 1kΩ	V_{DD} = 2.7 to 5.5 V	0		300	ns
		C = 100 pF[Note]		0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

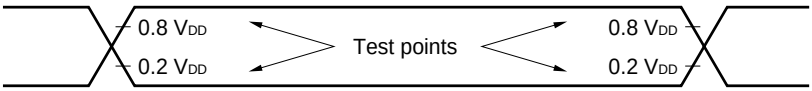
(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

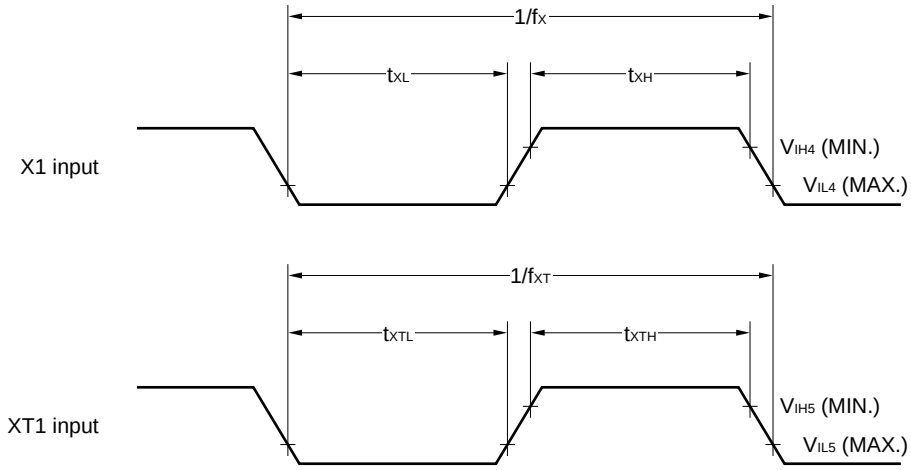
(d) UART mode (external clock input)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
			3500			ns
ASCK high- and low-level widths	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK rise and fall times	t_R, t_F				1	μs

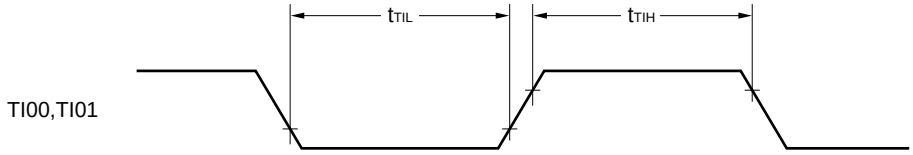
AC Timing Test Points (Except X1 and XT1 input)



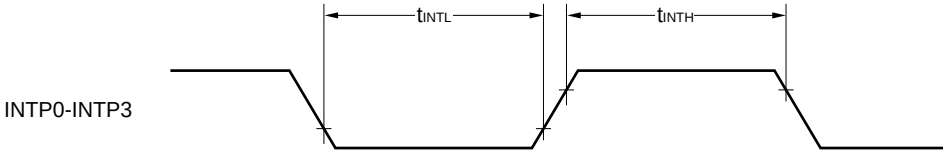
Clock Timing



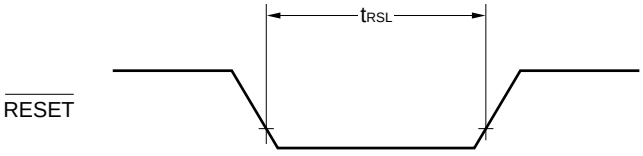
TI Timing



Interrupt Input Timing

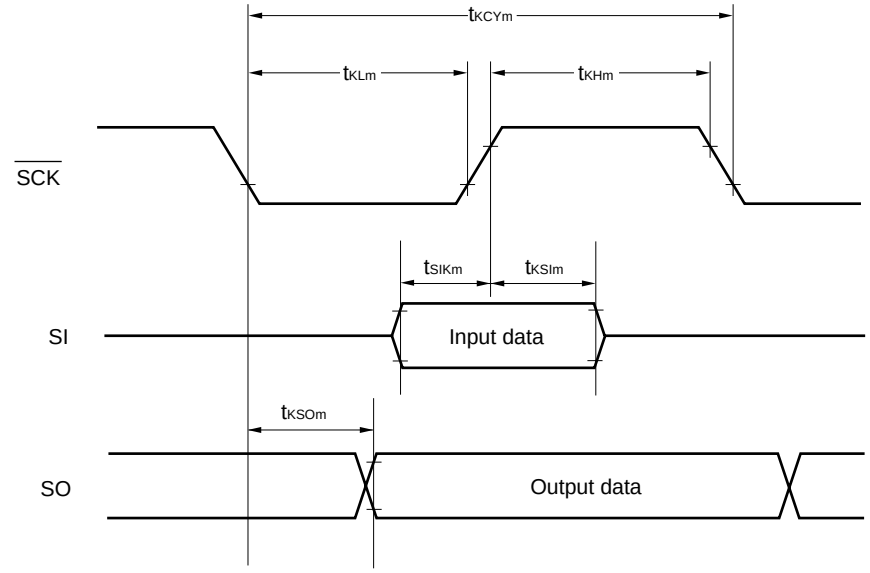


$\overline{\text{RESET}}$ Input Timing



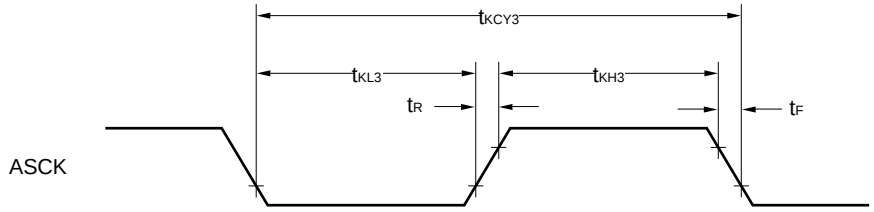
Serial Transfer Timing

Three-Wire Serial I/O Mode:



Remark m = 1 or 2

UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD789405A, 789406A, 789407A)

(T_A = –40 to +85 °C, 1.8 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
				±0.8	±1.2	%FSR
Conversion time	t_{CONV}	2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
			28		100	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{ADREF}		20	40		kΩ

Note The quantized error (±0.2%) is not included.

10-Bit A/D Converter Characteristics (μPD789415A, 789416A, 789417A)

(T_A = –40 to +85 °C, 1.8 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Total error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error[Note]	AINL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error[Note]	AINL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Non-integral linearity[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Non-differential linearity[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{ADREF}		20	40		kΩ

Note The quantized error (±0.05%) is not included.

Comparator Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog input range	V_{CIN}		0		V_{DD}	V
Reference voltage input range	V_{CREF}	V_{DD} = 2.7 to 5.5 V	1.35	1.6	1.85	V
			1.35	1.4	1.45	V
Accuracy					±100	mV

Low-Voltage Data Retention Characteristics of Data Memory in STOP Mode (T_A = –40 to +85 °C)

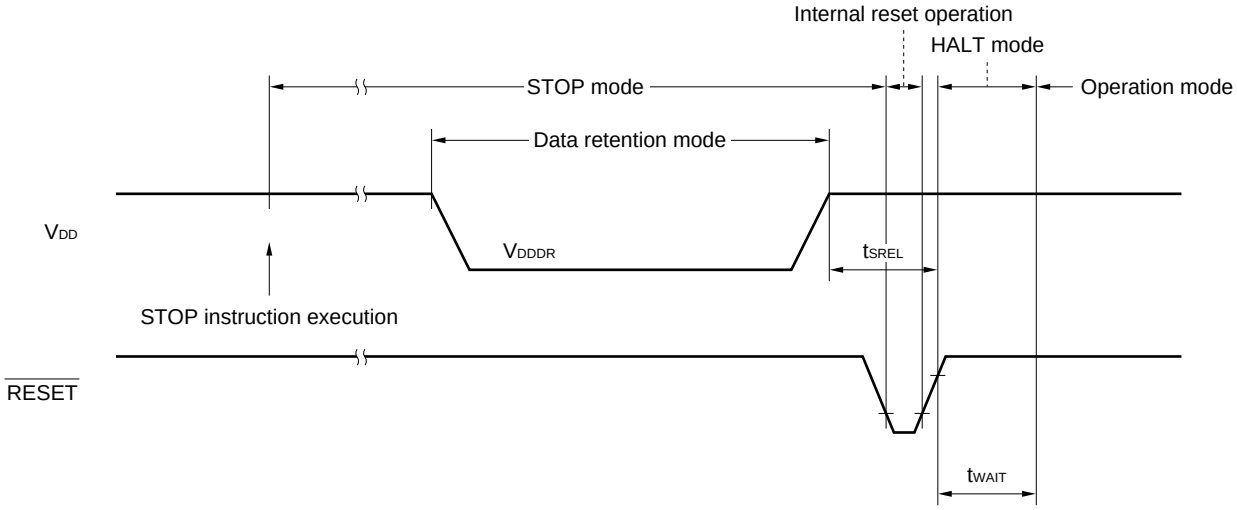
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Released by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time after oscillation has started during which the CPU is stopped to prevent unstable operation.

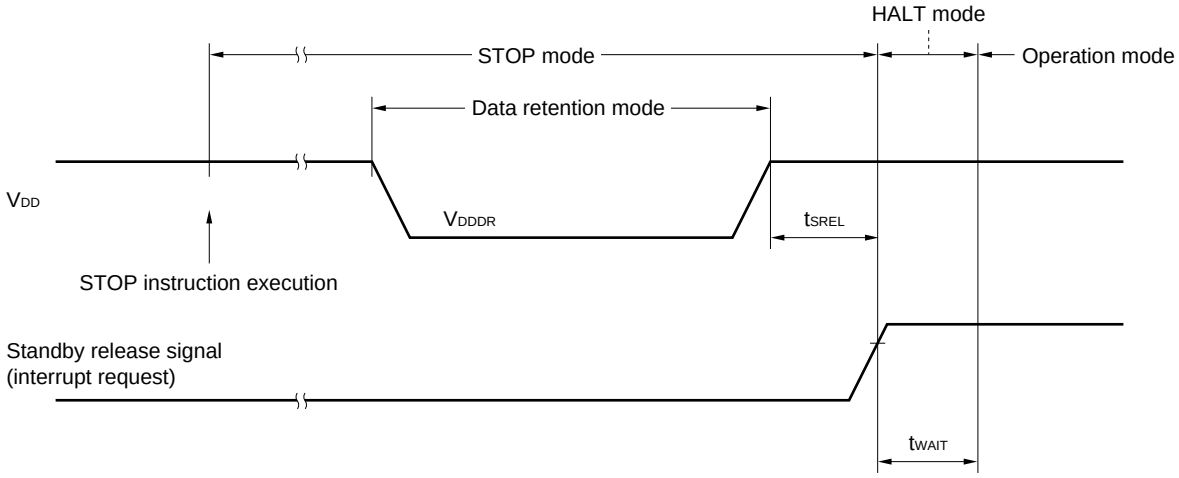
2. $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected by using bits 0 through 2 (OSTS0 through OSTS2) of the oscillation stabilization time select register (OSTS).

Remark fx: Main system clock oscillation frequency

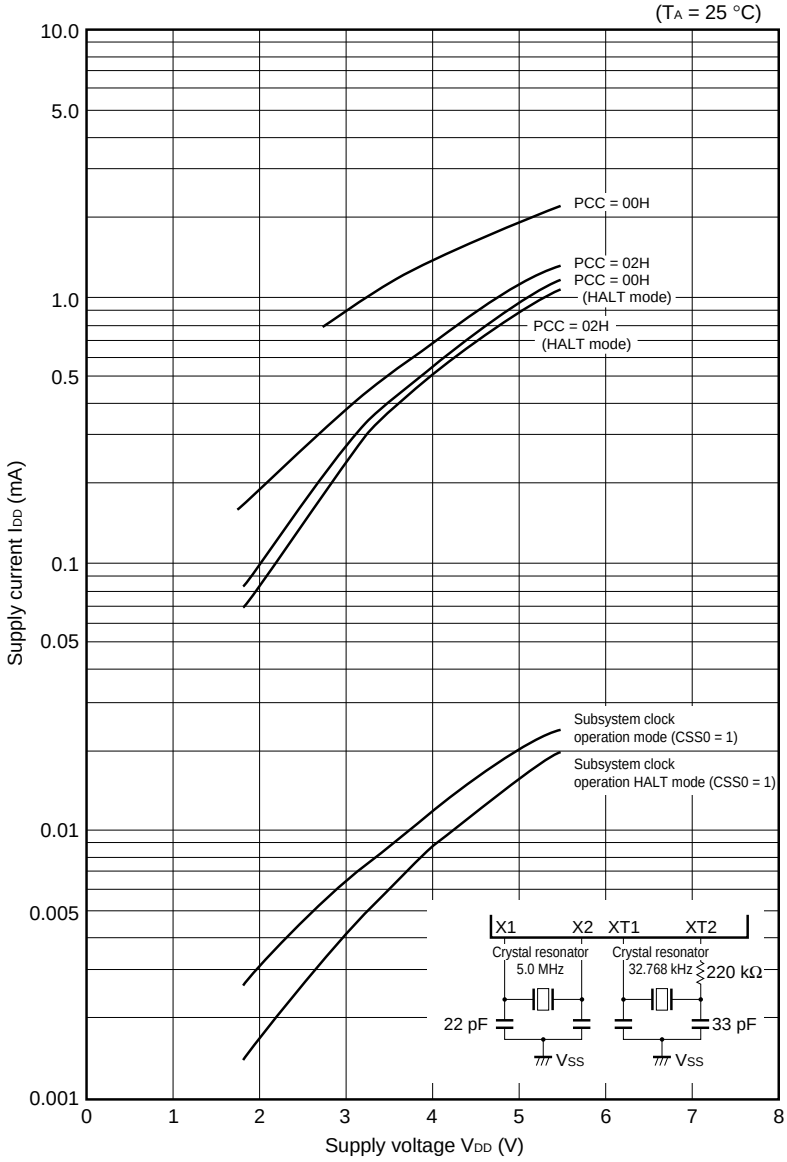
Data Retention Timing (Releasing STOP mode by $\overline{\text{RESET}}$)



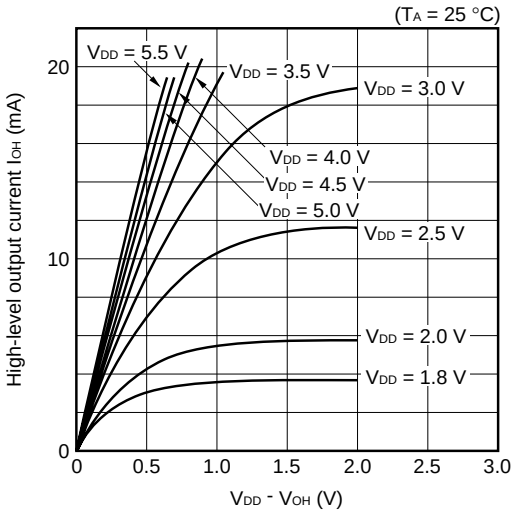
Data Retention Timing (Standby release signal: Releasing STOP mode by interrupt signal)



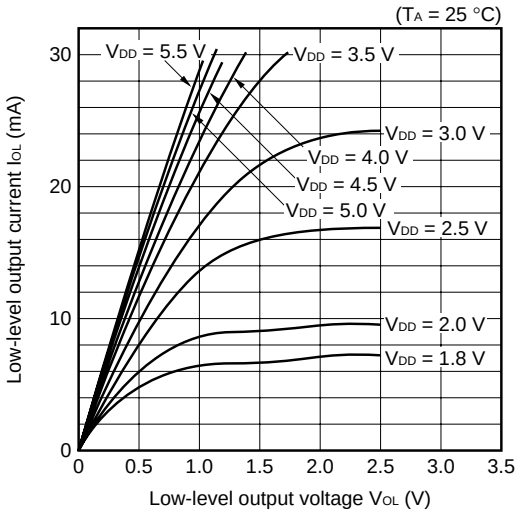
12. CHARACTERISTIC CURVE



IOH vs VDD - VOH

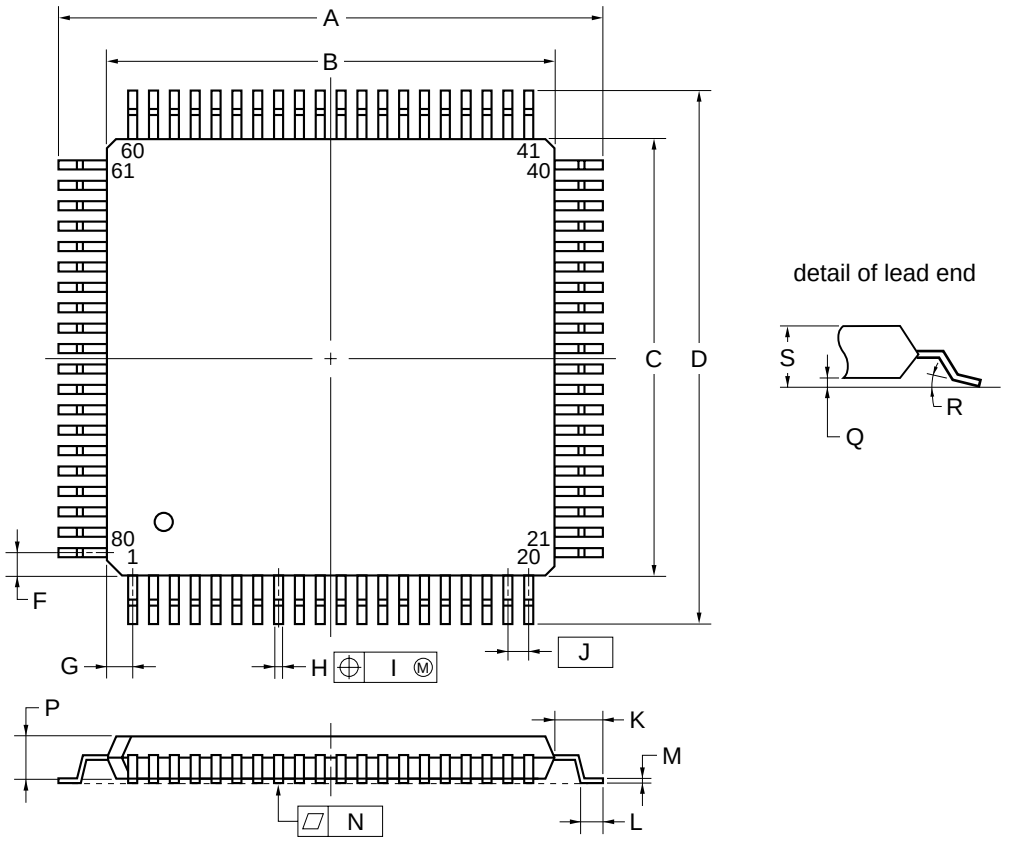


IOL vs VOL



13. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×14)



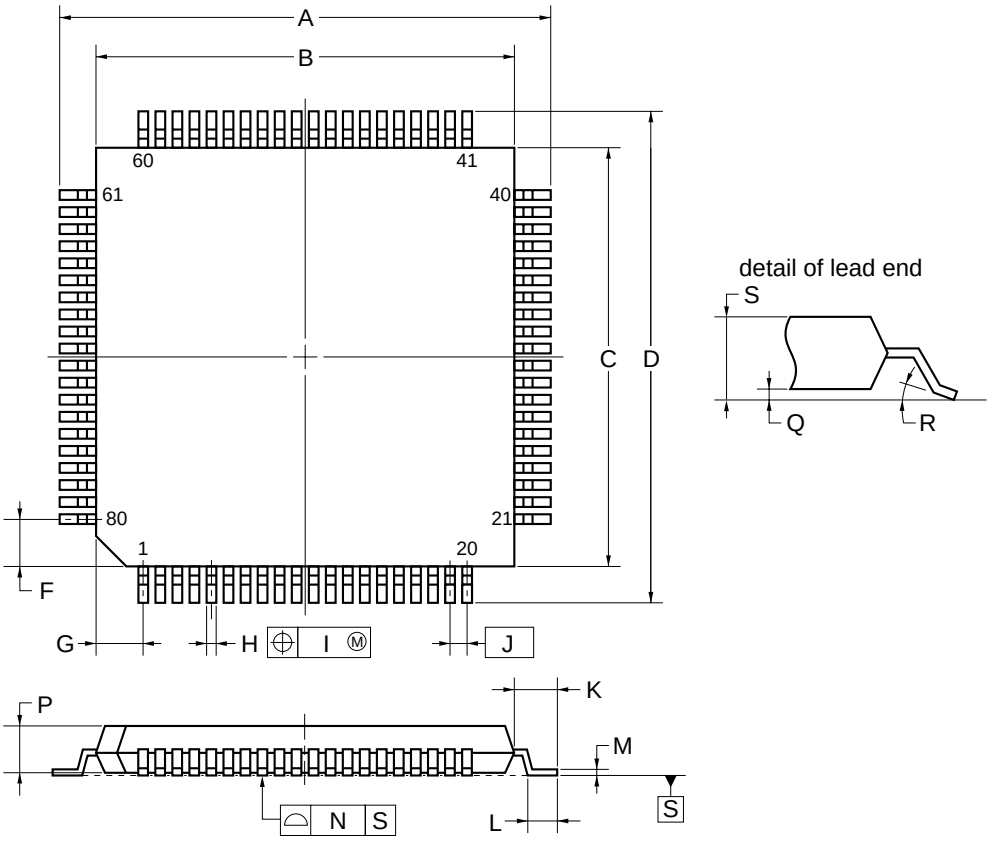
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (12x12)



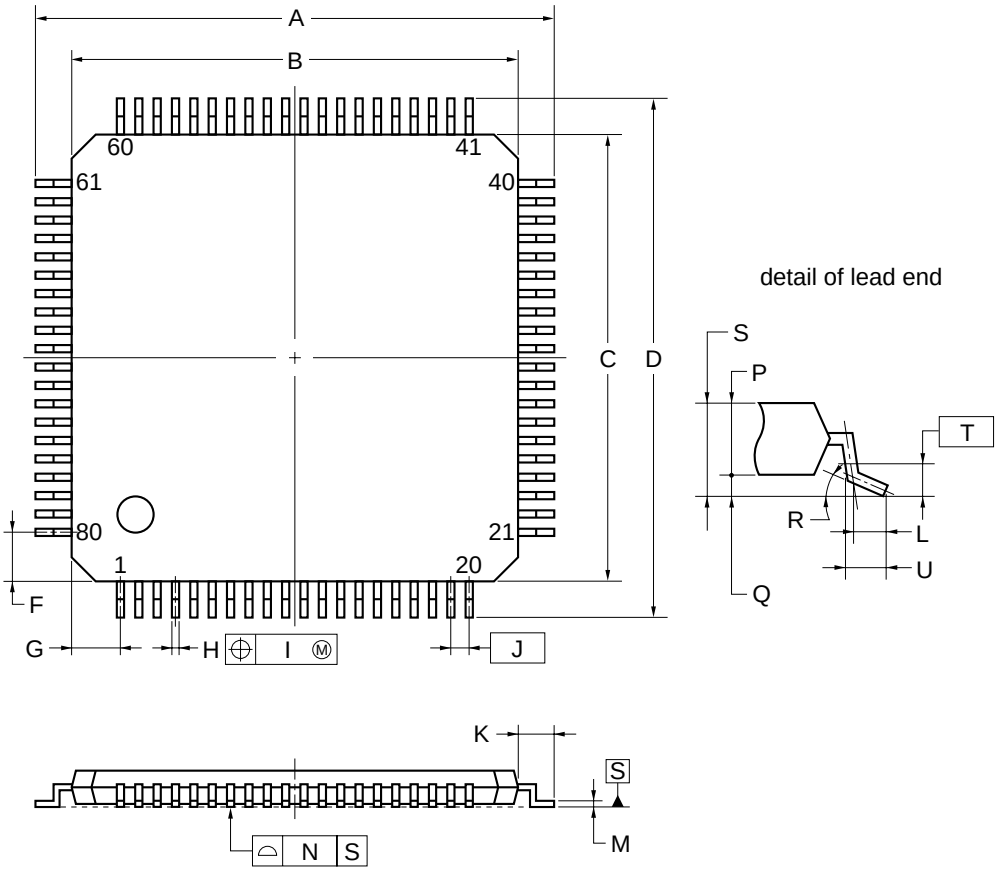
NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.00±0.20
B	12.00±0.20
C	12.00±0.20
D	14.00±0.20
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.05±0.07
Q	0.10±0.05
R	5°±5°
S	1.27 MAX.

P80GK-50-BE9-6

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

14. RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder the μPD789405A, 789406A, 789407A, 789415A, 789416A, and 789417A under the following conditions.

For details of the recommended soldering conditions, refer to Information Document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Table 14-1. Soldering Conditions for Surface Mount Type (1/3)

μPD789405AGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD789406AGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD789407AGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD789415AGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD789416AGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)
μPD789417AGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX (210 °C MIN), Number of times: 2 MAX	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX (200 °C MIN), Number of times: 2 MAX	VP15-00-2
Wave soldering	Soldering bath temperature: 260 °C MAX, Time: 10 seconds MAX, Number of times: 1, Preheating temperature: 120 °C MAX (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C MAX, Time: 3 seconds MAX (per side of device)	–

Caution Do not use two or more soldering methods in combination (except partial heating method).

Table 14-1. Soldering Conditions for Surface Mount Type (2/3)

μPD789405AGK-×××-BE9: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD789406AGK-×××-BE9: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD789407AGK-×××-BE9: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD789415AGK-×××-BE9: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD789416AGK-×××-BE9: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)
μPD789417AGK-×××-BE9: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.05 mm)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX (210 °C MIN), Number of times: 2 MAX, Number of days: 3[Note] (After that, prebaking is necessary at 125 °C for 10 hours).	IR35-103-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds MAX (200 °C MIN), Number of times: 2 MAX, Number of days: 3[Note] (After that, prebaking is necessary at 125 °C for 10 hours).	VP15-103-2
Partial heating	Pin temperature: 300 °C MAX, Time: 3 seconds MAX (per side of device)	–

Note The number of days for storage at 25 °C, 65% RH MAX after the dry pack has been opened.

Caution Do not use two or more soldering methods in combination (except pin partial heating method).

Table 14-1. Soldering Conditions for Surface Mount Type (3/3)

μPD789405AGK-×××-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD789406AGK-×××-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD789407AGK-×××-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD789415AGK-×××-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD789416AGK-×××-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)
μPD789417AGK-×××-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12 mm, resin thickness: 1.0 mm)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds MAX (210 °C MIN), Number of times: 2 MAX, Number of days: 3[Note] (After that, prebaking is necessary at 125 °C for 10 hours).	IR35-103-2
Partial heating	Pin temperature: 300 °C MAX, Time: 3 seconds MAX (per side of device)	–

Note The number of days for storage at 25 °C, 65% RH MAX after the dry pack has been opened.

Caution Do not use two or more soldering methods in combination (except pin partial heating method).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for development of a system using the μPD789405A, 789406A, 789407A, 789415A, 789416A, or 789417A.

Language processor software

RA78K0S[Notes 1, 2, 3]	Common assembler package for 78K/0S series
CC78K0S[Notes 1, 2, 3]	Common C compiler package for 78K/0S series
DF789418[Notes 1, 2, 3]	Device file for μPD789407A and 789417A subseries

Flash memory writing tools

FlashproIII (FL-PR3[Note 4], PG-FP3)	Flash programmer for microcontrollers with flash memory
FA-80GC[Note 4]	Flash memory writing adapter for 80-pin plastic QFP (GC-8BT type)
FA-80GK[Note 4]	Flash memory writing adapter for 80-pin plastic TQFP (fine pitch) (GK-BE9 type)
FA-80GK-9EU[Note 4]	Flash memory writing adapter for 80-pin plastic TQFP (fine pitch) (GK-9EU type)
Flashpro III controller	Program provides control from personal computer and supplied with Flashpro III. Runs on Windows™95, etc.

Debugging tools

IE-78K0S-NS in-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power from an AC 100 to 240-V outlet.
IE-70000-98-IF-C interface adapter	Adapter necessary when using a PC-9800 series (except notebook type) as the host machine of the IE-78K0S-NS (supports C bus).
IE-70000-CD-IF-A PC card interface	PC card and interface cable necessary when a notebook type personal computer is used as the host machine of the IE-78K0S-NS (supports PCMCIA socket).
IE-70000-PC-IF-C interface adapter	Adapter necessary when an IBM PC/AT™ or compatible machine is used as the host machine of the IE-78K0S-NS (supports ISA bus).
IE-70000-PCI-IF interface adapter	Adapter necessary when using a personal computer with PCI bus is used as the host machine of the IE-78K0S-NS.
IE-789418-NS-EM1 emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-80GC[Note 4]	Board connecting an in-circuit emulator and target system. For 80-pin plastic QFP (GC-8BT type).
NP-80GK[Note 4]	Board connecting an in-circuit emulator and target system. For 80-pin plastic TQFP (fine pitch) (GK-BE9 and GK-9EU types).
SM78K0S[Notes 1, 2]	Common system simulator for 78K/0S series
ID78K0S-NS[Notes 1, 2]	Common integrated debugger for 78K/0S series
DF789418[Notes 1, 2]	Device file for μPD789407A and 789417A subseries

Real-time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S series

Notes 1. PC-9800 series (MS-DOS™ + Windows) based

2. IBM PC/AT or compatible machine (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEWS-OS™) based

4. This is a product of Naito Densei Machida Mfg. Co., Ltd. (Tel: 044-822-3813). Consult NEC distributors for purchasing.

Remark The RA78K0S, CC78K0S, and SM78K0S are used with the DF789418.

APPENDIX B. RELATED DOCUMENTS

Device-Related Documents

Document Name	Document No.	
	Japanese	English
μPD789405A, 789406A, 789407A, 789415A, 789416A, 789417A Data Sheet	U14024J	This document
μPD78F9418 Preliminary Product Information	U12626J	U12626E
μPD789407A, 789417A Subseries User's Manual	U13952J	Planned to be published
78K/0S Series User's Manual - Instructions	U11047J	U11047E

Documents on Development Tools (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly language	U11599J	U11599E
	Structured assembly language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator, Windows-based	Reference	U11489J	U11489E
SM78K Series System Simulator	External part user open interface specifications	U10092J	U10092E
ID78K0S-NS Integrated Debugger, Windows-based	Reference	U12901J	U12901E
IE-78K0S-NS In-Circuit Emulator		U13549J	U13549E
IE-789418-NS-EM1 Emulation Board		Planned to be published	Planned to be published

Documents on Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0S Series OS MX78K0S	Fundamental	U12938J	U12938E

Other Documents

Document Name	Document No.	
	Japanese	English
Semiconductors Selection Guide Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	–

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Fax: 408-588-6130
800-729-9288

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Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
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Fax: 01908-670-290

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