RC4207

Precision Monolithic Dual Operational Amplifier

Features

- Low Noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Ultra-low V_{OS} – 75 μV
- Ultra-low V_{OS} drift – 1.3 $\mu V/°C$
- Long term V_{OS} stability – 0.2 $\mu V/Mo$
- Low input bias and offset currents – ±5 nA
- High gain – 400 V/mV
- Fits 4558 socket
- Industry standard pinout
- 8-lead mini-DIP

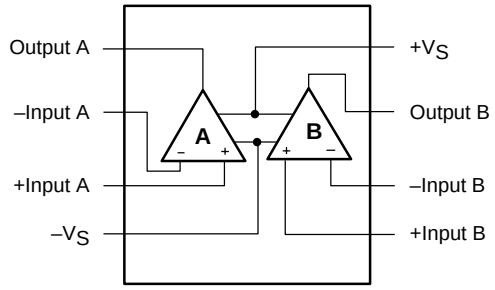
Description

Designed for low level signal conditioning and instrumentation applications, the 4207 is a precision dual amplifier combining excellent DC input specifications with low input noise characteristics. Ultra low input offset voltage, low drift, high CMRR, and low input bias currents serve to reduce input related errors to less than 0.01% in a typical high gain instrumentation amplifier system (A_V = 1000). The 4207 contains two separate amplifiers with a high degree of isolation between them; each is complete requiring no external compensation capacitors or offset nulling potentiometers.

The inherent V_{OS} is typically less than 150 μV, resulting in superior temperature drift, and this low initial offset is further reduced by "Zener-zap" nulling when the wafers are tested.

Advanced thin film and nitride dielectric processing allows the 4207 to achieve its high performance and small size (the 4207 is offered in 8-lead DIPs). The 4207 fits the industry standard 8-lead op amp pin-out.

Block Diagram



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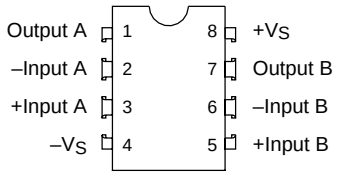
Pin Assignments



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Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter		Min	Typ	Max	Units
Supply Voltage				±18	V
Input Voltage[2]				±18	V
Differential Input Voltage				30	V
Internal Power Dissipation[3]				500	mW
$P_D T_A$ < 50°C				468	mW
Output Short Circuit Duration		Indefinite			
Junction Temperature				125	°C
Storage Temperature		-65		150	°C
Operating Temperature		0		70	°C
Lead Soldering Temperature (60 sec)				300	°C
For T_A > 50°C Derate at			6.25		mW/°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Observe package thermal characteristics.

Operating Conditions

Parameter		Min	Typ	Max	Units
θ_{JA}	Thermal resistance		160		°C/W

Electrical Characteristics

(V_S = ±15V, 0°C ≤ T_A ≤ +70˚C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	μV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.7		μV/°C
Input Offset Current			±2.0	±10		±1.6	±15	nA
Average Input Offset Current Drift			8.0			12		pA/°C
Input Bias Current			±2.0	±10		±3.0	±15	nA
Average Input Bias Current Drift			13			18		pA/°C
Input Voltage Range		±10	±13.5		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	94	120		92	106		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	94	115		92	100		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_{OUT} = ±10V	200	450		75	400		V/mV
Maximum Output Voltage Swing	R_L > 2.0kΩ	±11	±12.6		±11	±12.6		V
Power Consumption	R_L = ∞		150	240		150	240	mW

Electrical Characteristics

(V_S = ±15V, and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			30	75		60	150	μV
Long Term V_{OS} Stability[1]			0.2			0.5		μV/Mo
Input Offset Current			±0.5	±5		±2	±10	nA
Input Bias Current			±0.5	±5		±2	±10	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35			0.35		μVp-p
Input Noise Voltage Density	F_O = 10 Hz		10.3			10.3		$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10			10		
	F_O = 1000 Hz		9.6			9.6		
Input Noise Current	0.1 Hz to 10 Hz		14			14		pA_{p-p}
Input Noise Current Density	F_O = 10 Hz		0.32			0.32		$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14			0.14		
	F_O = 1000 Hz		0.12			0.12		
Input Resistance (Diff. Mode)			60			31		MΩ
Input Resistance (Com. Mode)			200			120		GΩ
Input Voltage Range[4]		±11	±14		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	100	126		94	110		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	110		94	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	400	600		250	400		V/mV
	V_{OUT} = ±1.0V, R_L = 1KΩ, V_S = ±4.0V	200	400		100	200		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/μs
Closed Loop Bandwidth	A_{VOL} = +1.0		1.5			1.5		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		150	200		160	240	mW
	V_S = ±4.0V, R_L = ∞		35	50		48	64	
Crosstalk	DC	126	155		126	155		dB

Notes:

1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Typical Performance Characteristics

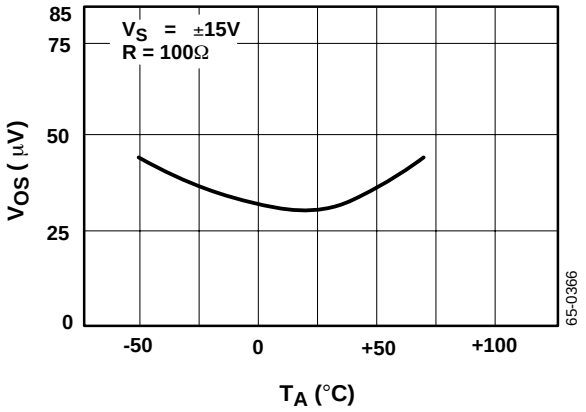


Figure 1. Input Offset Voltage vs. Temperature

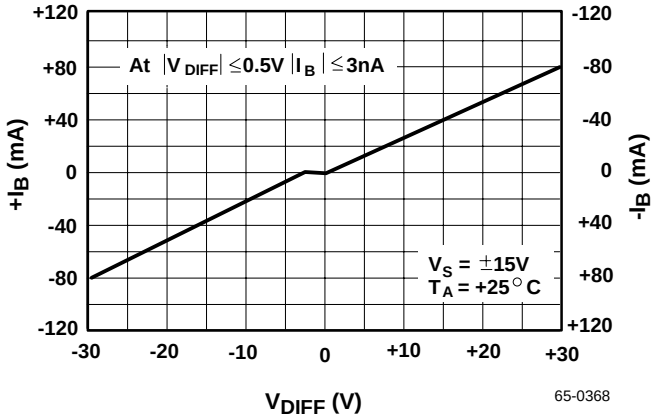


Figure 2. Input Bias Current vs. Differential Input Voltage

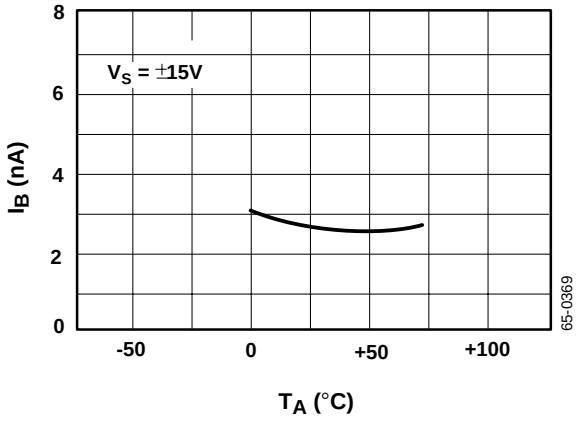


Figure 3. Input Bias Current vs. Temperature

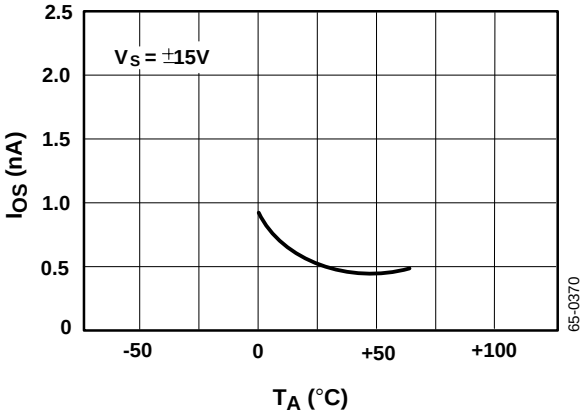


Figure 4. Input Offset Current vs. Temperature

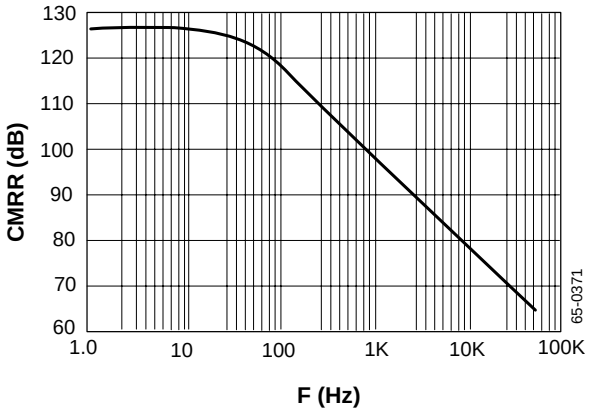


Figure 5. CMRR vs. Frequency

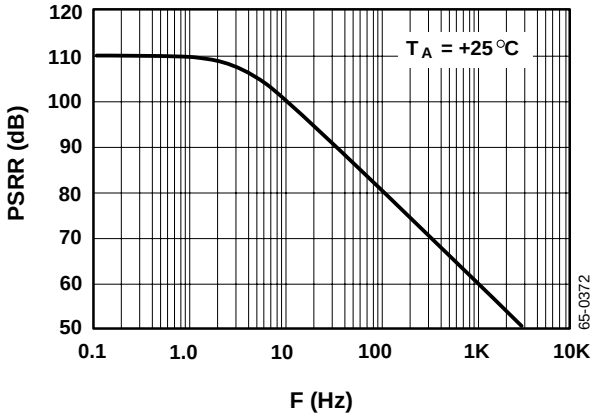


Figure 6. PSRR vs. Frequency

Typical Performance Characteristics (continued)

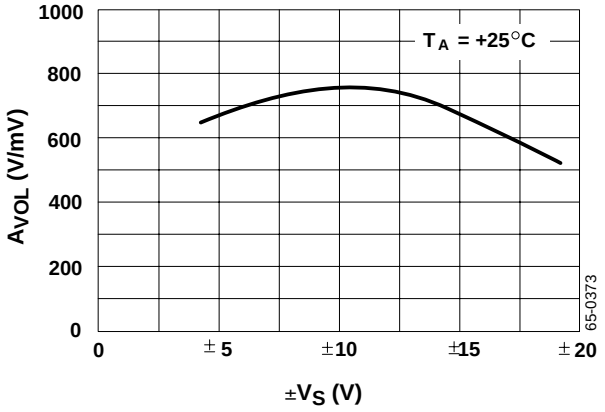


Figure 7. Open Loop Gain vs. Supply Voltage

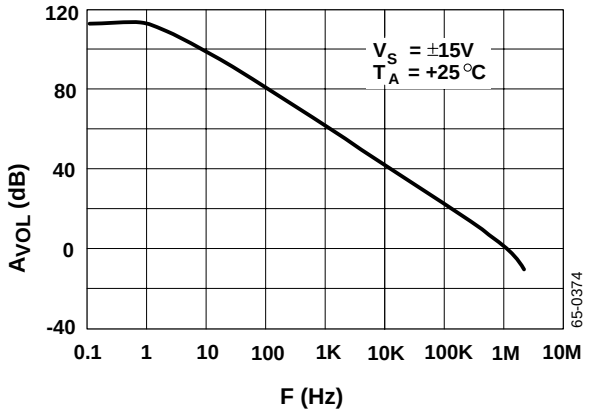


Figure 8. Open Loop Gain vs. Frequency

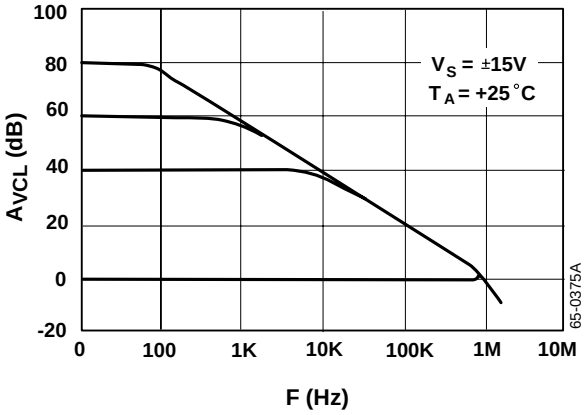


Figure 9. Closed Loop Response for Various Gain Configurations

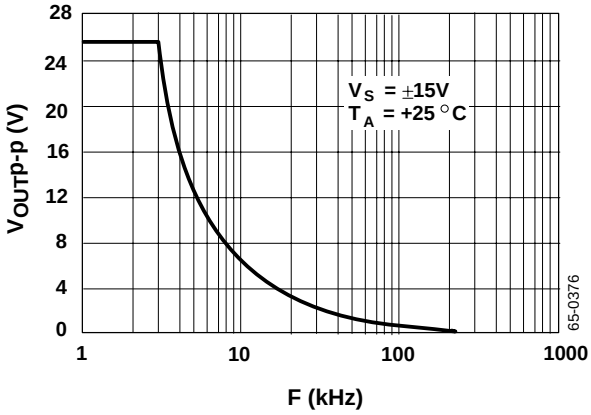


Figure 10. Maximum Undistorted Output vs. Frequency

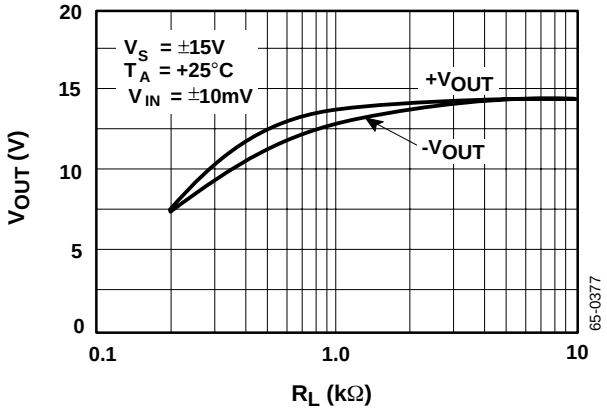


Figure 11. Output Voltage vs. Load Resistance to Ground

Typical Performance Characteristics (continued)

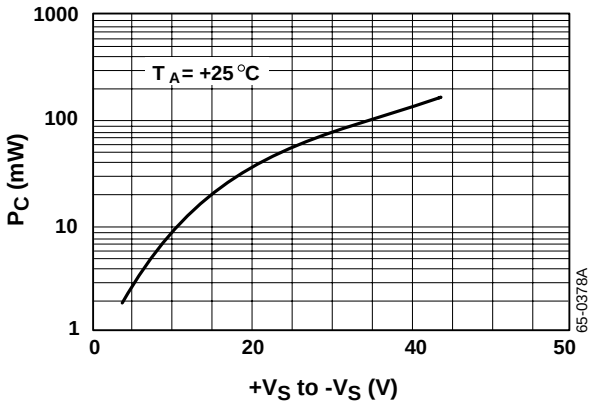


Figure 12. Power Consumption vs. Total Supply Voltage

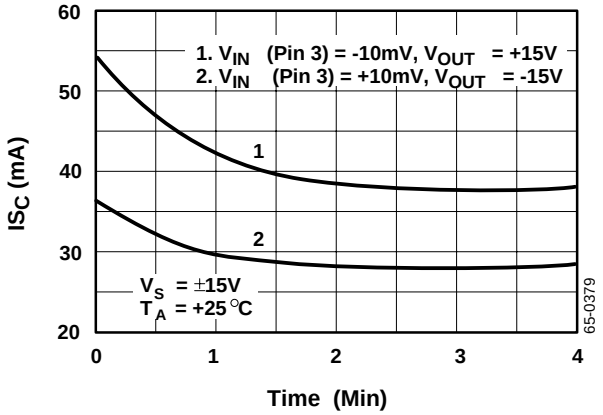


Figure 13. Output Short Circuit Current vs. Time

Typical Applications

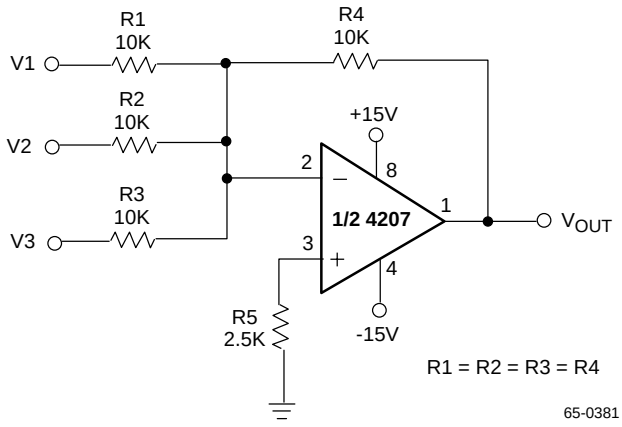


Figure 14. Adjustment-Free Precision Summing Amplifier

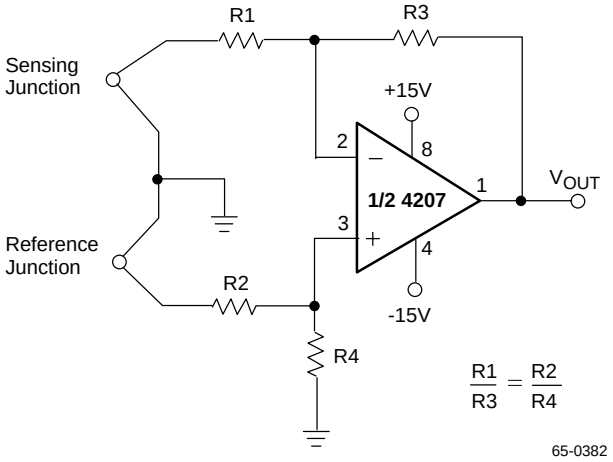


Figure 15. High Stability Thermocouple Amplifier

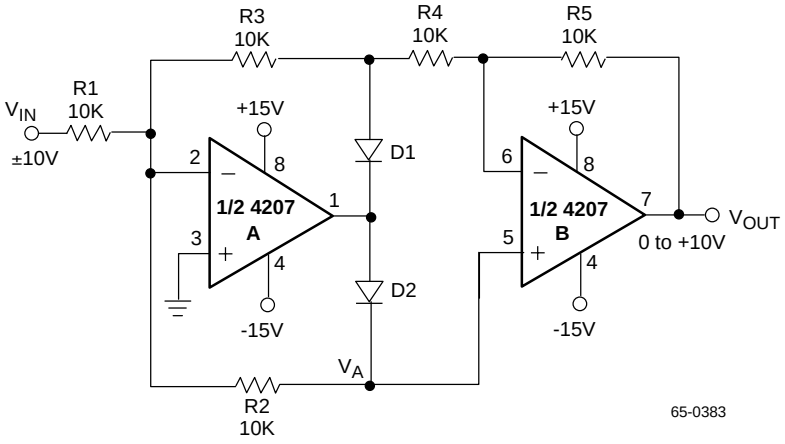
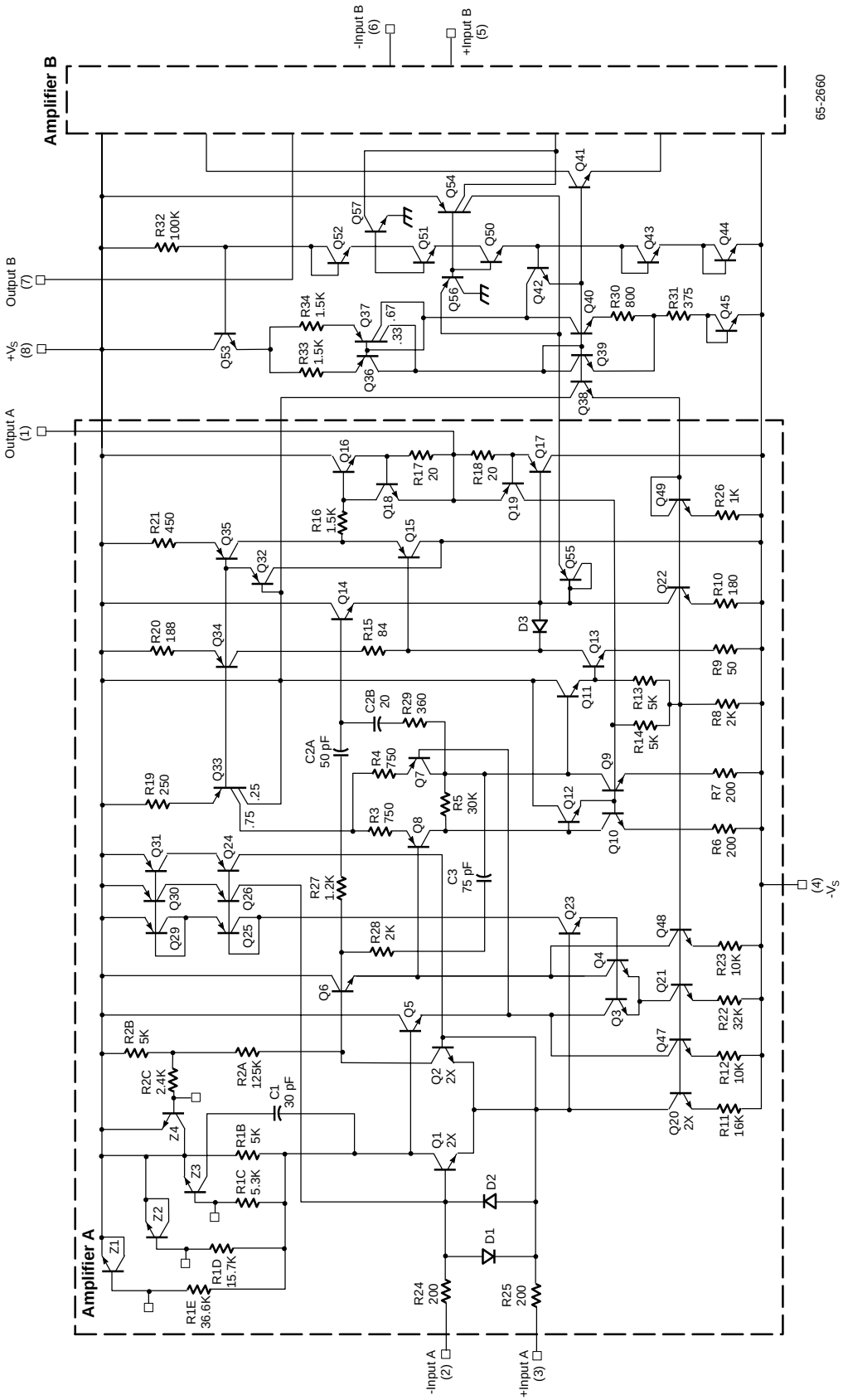


Figure 16. Precision Absolute Value Circuit

Schematic Diagram

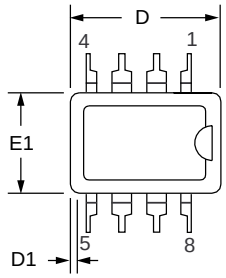


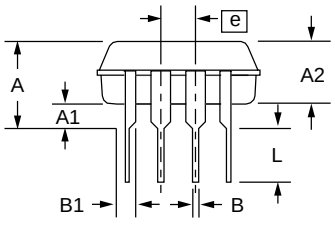
Mechanical Dimensions – 8-Lead Plastic DIP Package

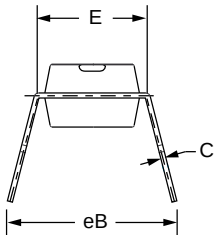
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







Ordering Information

Product Number	Temperature Range	Screening	Package
RC4207FN	0° to +70°C	Commercial	8 Pin Plastic DIP
RC4207GN	0° to +70°C	Commercial	8 Pin Plastic DIP