NEC

MOS INTEGRATED CIRCUIT

μPD789870, 789871

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789870 and μPD789871 are μPD789871 Subseries product (Driving VFD) of the 78K/0S Series.

The μPD789871 Subseries consists of products that incorporate a VFD controller/driver for panel control.

A flash memory version, the μPD78F9872, which can operate in the same power supply voltage range as the mask ROM version, and various development tools are also under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789871 Subseries User's Manual: To be prepared
78K/0S Series User's Manual Instruction: U11047E

FEATURES

- Internal ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory	
		Internal High-Speed RAM	VFD Display RAM
μPD789870	4 KB	512 bytes	96 bytes
μPD789871	8 KB		

- Minimum instruction execution time can be changed from high-speed (0.4 μs: Main system clock 5.0-MHz operation) to ultra-low speed (122 μs: Subsystem clock 32.768-kHz operation)
- I/O ports: 33
- Timers: 5 channels
  - 8-bit remote control: 1 channel
  - 8-bit timer/event counter: 2 channels
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Serial interface: 1 channel
- VFD controller/driver: Total of display outputs: 25
- Power supply voltage : V_{DD} = 2.7 to 5.5 V (in normal operation)
  : V_{DD} = 4.5 to 5.5 V (when VFD is operating)

APPLICATIONS

Products with front panel such as DVD, VCD, S-VCD players etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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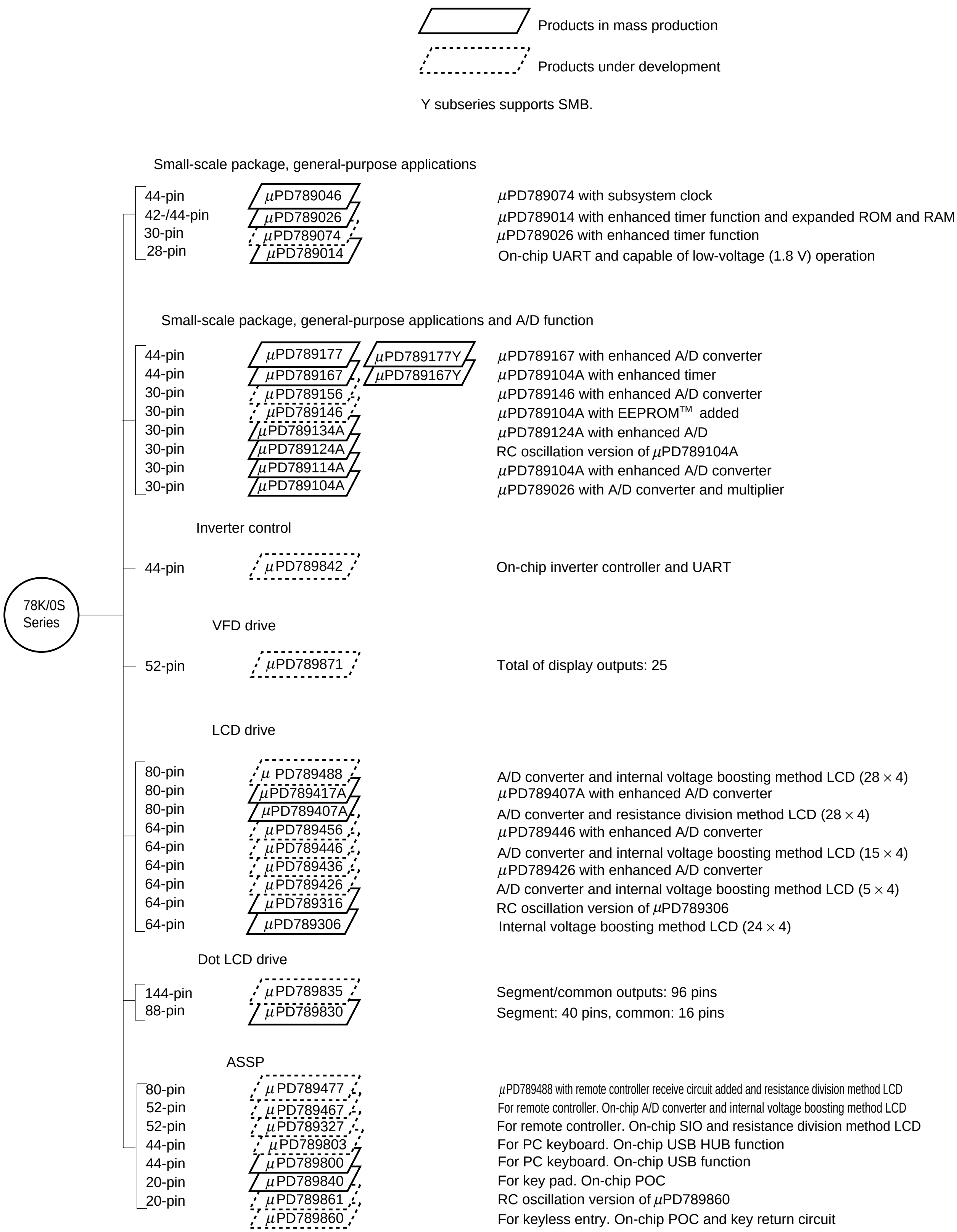
ORDERING INFORMATION

Part Number	Package
μPD789870GB-xxx-8ET	52-pin plastic LQFP (10 × 10)
μPD789871GB-xxx-8ET	52-pin plastic LQFP (10 × 10)

Remark xxx indicates ROM code suffix.

78K/0S SERIES DEVELOPMENT

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major differences between subseries are shown below.

Subseries Name		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
Small, general-purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART:1 ch)	34 pins	1.8 V	–
	μPD789026	4 K-16 K			–							
	μPD789074	2 K to 8 K								24 pins		
	μPD789014	2 K-4 K	2 ch	–						22 pins		
Small, general-purpose + A/D	μPD789177	16 K-24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31 pins	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K-16 K	1 ch		–		–	4 ch		20 pins		Internal EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K-8 K						4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
For inverter control	μPD789842	8 K-16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30 pins	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
For LCD driving	μPD789417A	12 K-24 K	3 ch	1 ch	1 ch	1 ch	–	7 ch	1 ch (UART: 1 ch)	43 pins	1.8 V	–
	μPD789407A						7 ch	–				
	μPD789456	12 K-16 K	2 ch				–	6 ch		30 pins		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40 pins		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16K					–		2 ch (UART: 1 ch)	23 pins		RC oscillation version
	μPD789306											–
For Dot LCD driving	μPD789835	24 K-60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28 pins	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30 pins	2.7 V	
ASSP	μPD789467	4 K-24 K	2 ch	–	1 ch	1 ch	1 ch	–	–	18 pins	1.8 V	Internal LCD
	μPD789327						–		1 ch	21 pins		
	μPD789803	8 K-16 K			–				2 ch (USB: 1 ch, UART: 1 ch)	41 pins	3.6 V	–
	μPD789800	8 K							2 ch (USB: 1 ch)	31 pins	4.0 V	
	μPD789840						4 ch		1 ch	29 pins	2.8 V	
	μPD789861	4 K					–		–	14 pins	1.8 V	RC oscillation version, Internal EEPROM
	μPD789860											Internal EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		μPD789870	μPD789871
Internal memory	Flash memory	4 KB	8 KB
	High-speed RAM	512 bytes	
	VFD display RAM	96 bytes	
Minimum instruction execution time		•0.4/1.6 μs (@ 5.0-MHz operation with main system clock) •122 μs (@ 32.768-kHz operation with subsystem clock)	
General-purpose registers		8 bits × 8 registers	
Instruction set		•16-bit operations •Bit manipulations (set, reset, test)	
I/O ports		Total: 33 •CMOS I/O: 17 •P-ch open-drain I/O: 8 •P-ch open-drain output: 8	
VFD controller/driver		Total of display outputs: 25	
Timers		•8-bit remote control timer: 1 channel •8-bit timer: 2 channel •Watch timer: 1 channel •Watchdog timer: 1 channel	
Serial interface		3-wire serial mode: 1 channel	
Vectored interrupt sources	Maskable	Internal: 8, External: 4	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 2.7 to 5.5 V (in normal mode operation) V_{DD} = 4.5 to 5.5 V (VFD is operating)	
Operating ambient temperature		T_A = –40 to +85°C	
Package		52-pin plastic LQFP (10 × 10)	

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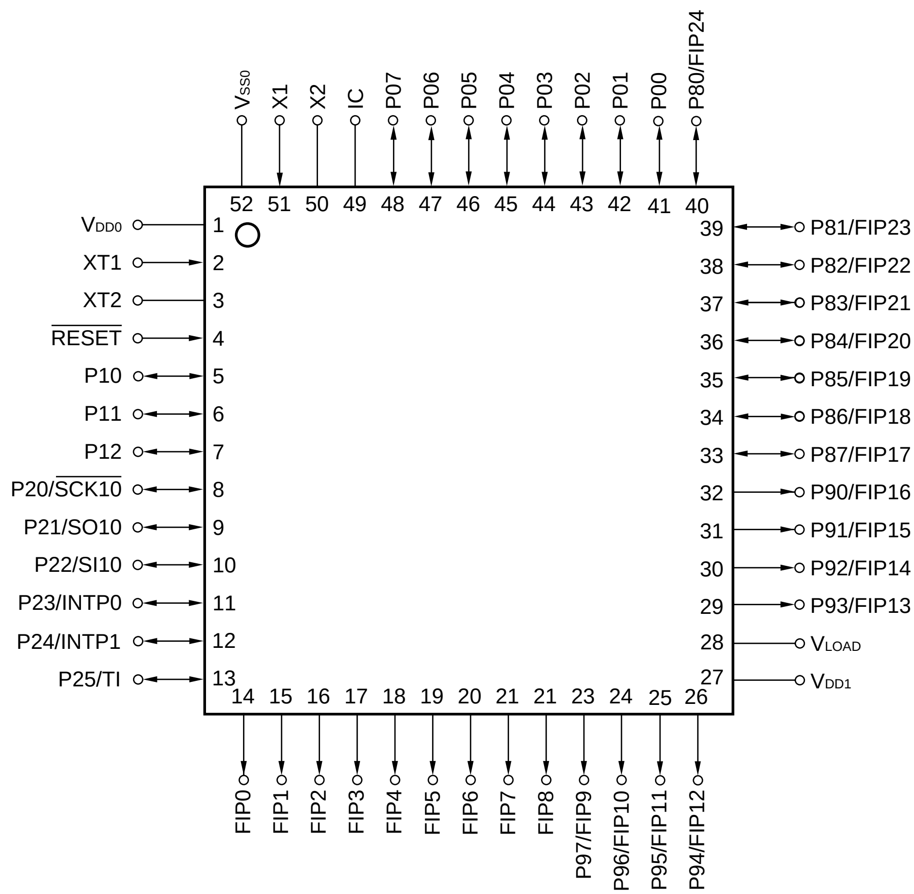
1. PIN CONFIGURATION (TOP VIEW)

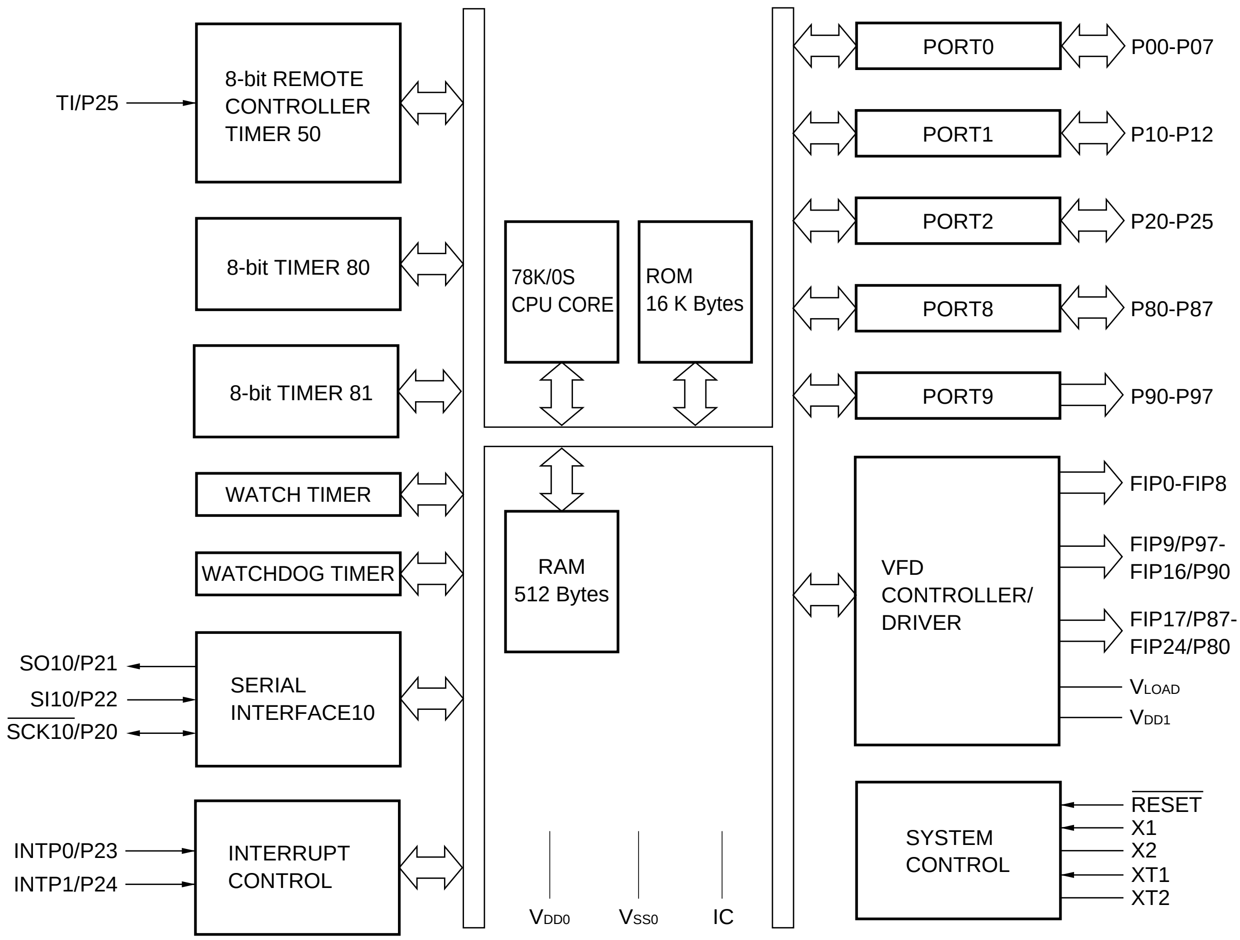
- **52-pin plastic LQFP (10 × 10)**
  μPD789870GB-xxx-8ET
  μPD789871GB-xxx-8ET



Caution Connect the IC (Internally Connected) pin directly to V_{SS0}.

FIP0 to FIP24:	Fluorescent Indicator Panel	SCK10:	Serial Clock
IC:	Internally Connected	SI10:	Serial Data Input
INTP0, INTP1:	Interrupt from Peripherals	SO10:	Serial Data Output
P00 to P07:	Port0	TI:	Timer Input
P10 to P12:	Port1	V_{DD0}, V_{DD1}:	Power Supply
P20 to P25:	Port2	V_{LOAD}:	Negative Power Supply
P80 to P87:	Port8	V_{SS0}:	Ground
P90 to P97:	Port9	X1, X2:	Crystal (Main System Clock)
RESET:	Reset	XT1, XT2:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark Internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit input/output port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P10 to P12	I/O	Port 1 3-bit input/output port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P20	I/O	Port 2 6-bit input/output port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{SCK10}$
P21				SO10
P22				SI10
P23				INTP0
P24				INTP1
P25				TI
P80 to P87	I/O	Port 8 P-ch open-drain 8-bit I/O port An on-chip pull-down resistor can be specified in 1-bit units by mask option (In case of I/O port, an on-ship pull-down resistor is connected to V_{SS0}).	Output	FIP17 to FIP24
P90 to P97	Output	Port 9 P-ch open-drain 8-bit output port An on-chip pull-down resistor is connected to V_{LOAD}.	Output	FIP9 to FIP16

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P23
INTP1				P24
SI10	Input	Serial data input to serial interface	Input	P22
SO10	Output	Serial data output from serial interface	Input	P21
$\overline{\text{SCK10}}$	I/O	Serial clock input/output for serial interface	Input	P20
TI	Input	8-bit remote control timer input	Input	P25
FIP0 to FIP8	Output	VFD controller/driver high withstand voltage large current output	Output	–
FIP9 to FIP16				P97 to P90
FIP17 to FIP24[Note]				P87 to P80
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for Subsystem clock oscillation	–	–
XT2	–		–	–
V_{LOAD}		VFD controller/driver pull-down resistor connection	–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD0}	–	Positive power supply for ports	–	–
V_{DD1}	–	Positive power supply for VFD controller/driver	–	–
V_{SS0}	–	Ground potential	–	–
IC	–	Internally connected. Connect directly to V_{SS0}.	–	–

Note An on-chip pull-down resistor can be connected to V_{LOAD} by mask option.

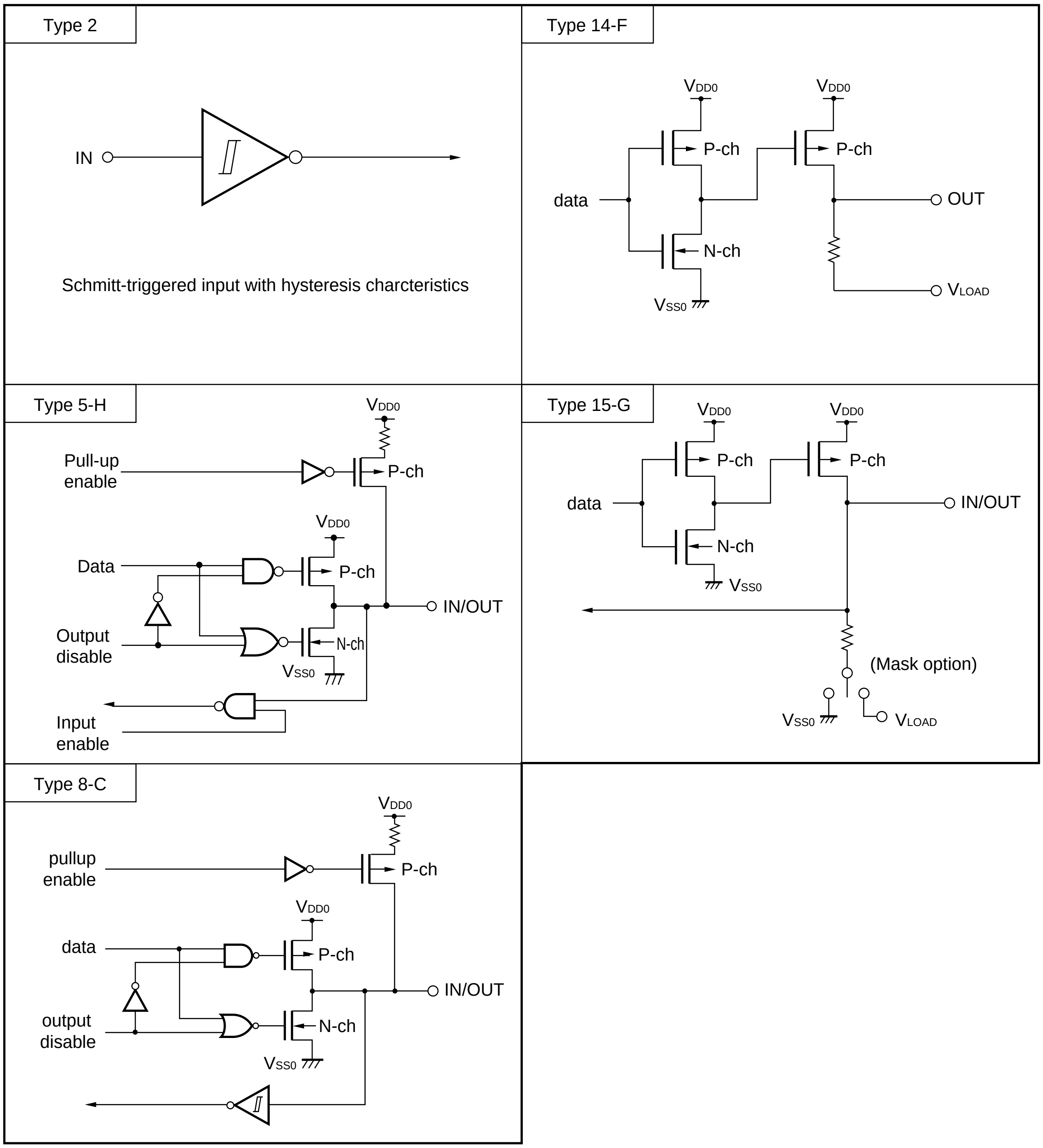
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins is shown in Table 3-1.
For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Type of I/O Circuit for Each Pin and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-H	I/O	Input: Independently connects to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P10 to P12			
P20/$\overline{SCK10}$	8-C		
P21/SO10	5-H		
P22/SI10	8-C		
P23/INTP0			
P24/INTP1			
P25/TI			
FIP0 to FIP8	14-F	Output	Leave open.
FIP9/P97 to FIP16/P90			
FIP17/P87 to FIP24/P80	15-G	I/O	
$\overline{RESET}$	2	Input	–
IC	–	–	Connect directly to V_{SS0}.

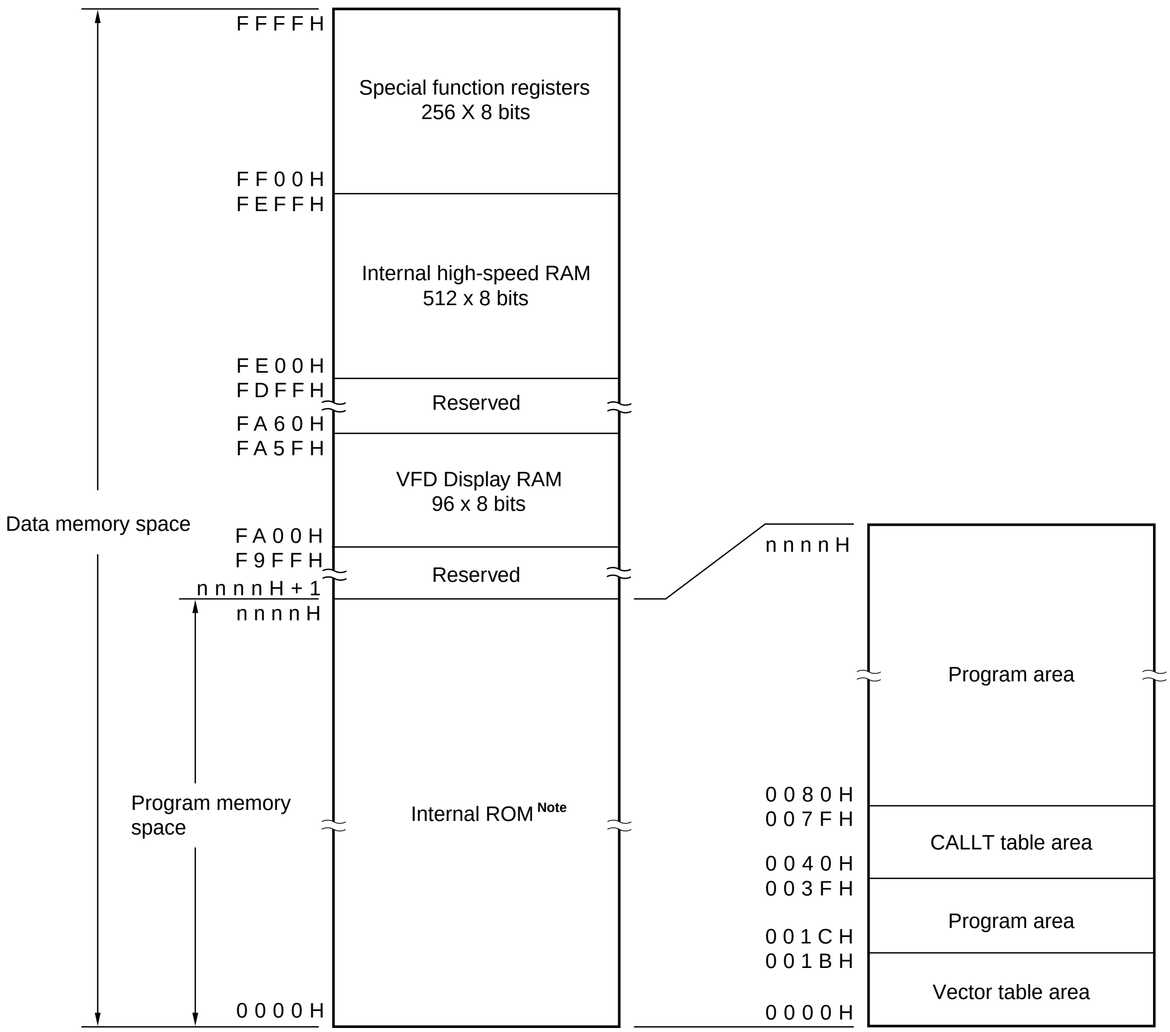
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

μPD789870 and μPD789871 can access up to 64 Kbytes of memory space.
Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The internal ROM capacity varies depending on the product (See the following table).

Part Number	Last Address of Internal ROM nnnnH
μPD789870	0FFFH
μPD789871	1FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following three types of I/O ports are available:

• CMOS Input/output:	17
• P-ch open-drain input/output:	8
• P-ch open-drain output:	8
Total:	33

Table 5-1. Port Functions

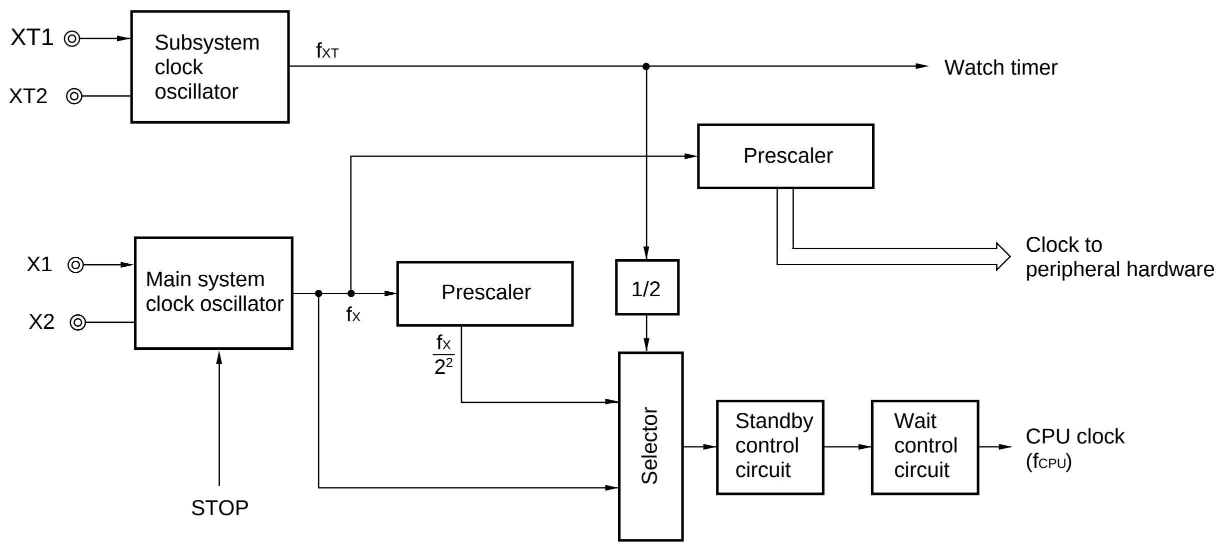
Port Name	Pin Name	Function
Port 0	P00 to P07	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 1	P10 to P12	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P25	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 8	P80 to P87	P-ch open-drain input/output port.
Port 9	P90 to P97	P-ch open-drain output port.

5.2 Clock Generator

An on-chip system clock generator is provided.
The minimum instruction execution time can be changed.

- 0.4 μs/1.6 μs (@ 5.0-MHz operation with Main system clock)
- 122 μs (@ 32.768-kHz operation with Subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Five on-chip timers are provided.

- 8-bit remote control timer 50: 1 channel
- 8-bit timer 80, 81: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Timer Operation

		8-bit remote control timer	8-bit timer	Watch timer	Watchdog timer
Operation mode	Interval timer	–	2 channels	1 channel	1 channel
Function	Pulse width measurement	1 output	–	–	–
	Interrupt request	3	2	1	1

Figure 5-2. Block Diagram of 8-Bit Remote Control Timer 50

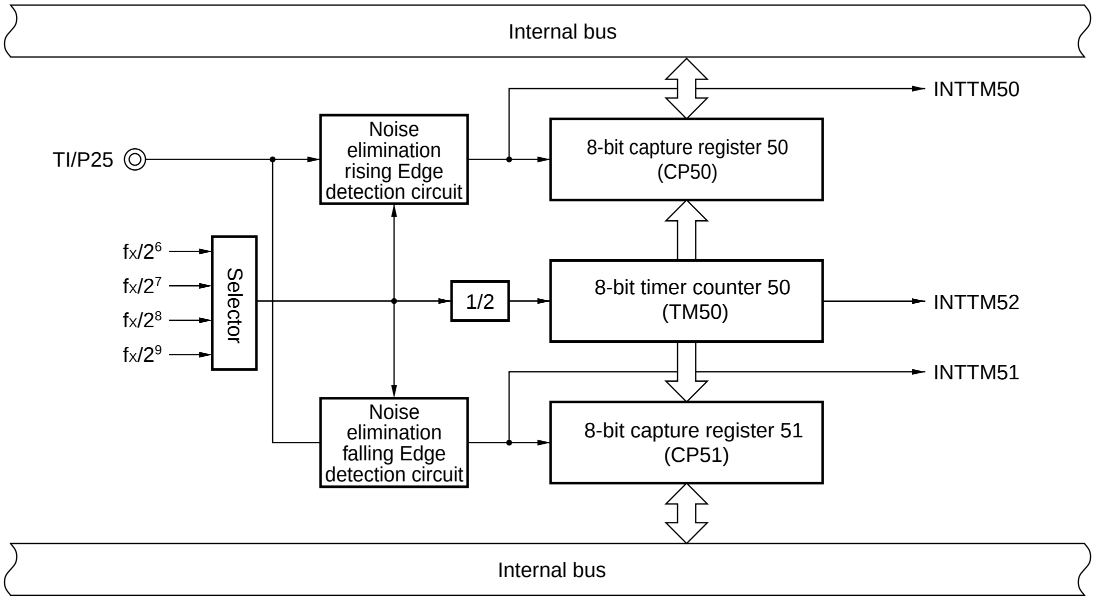


Figure 5-3. Block Diagram of 8-Bit Timer 80

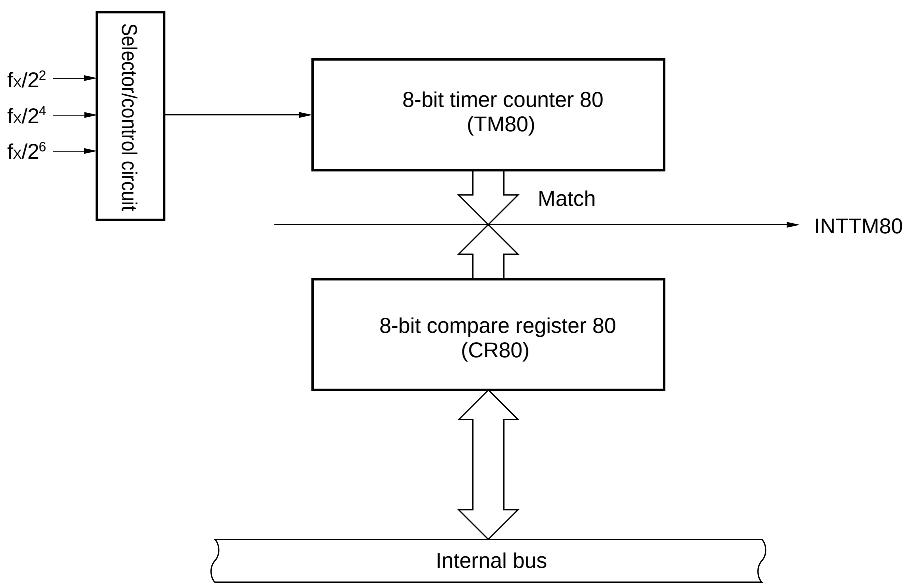


Figure 5-4. Block Diagram of 8-Bit Timer 81

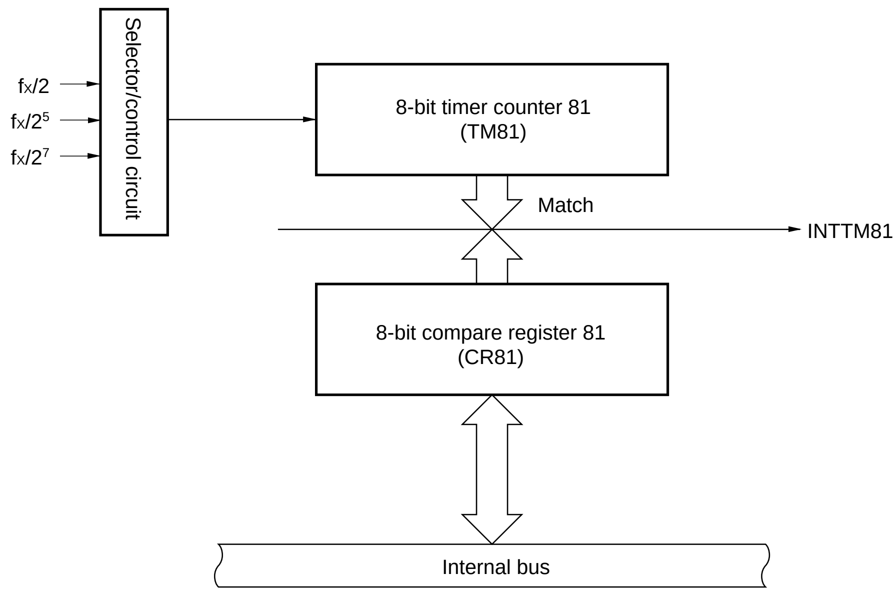
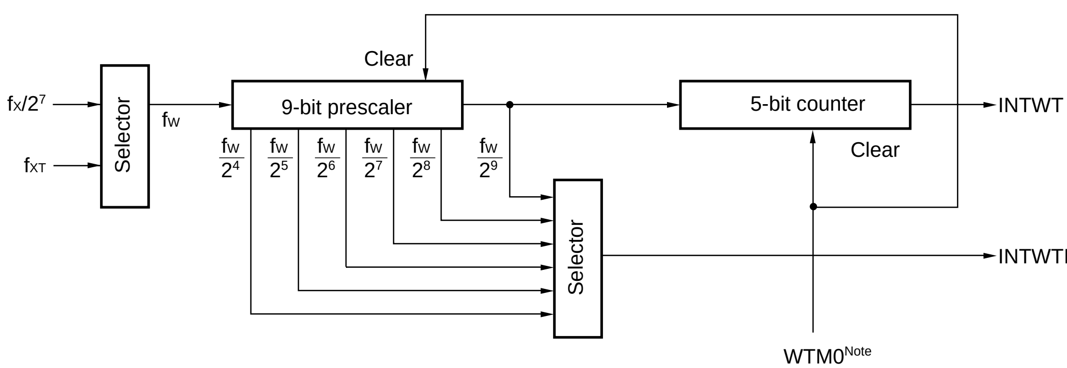
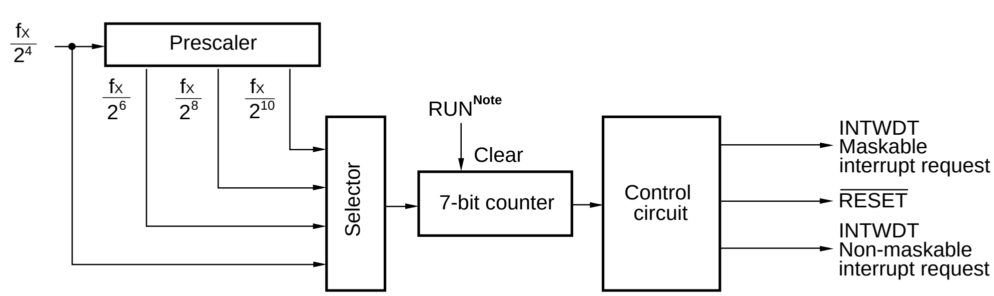


Figure 5-5. Block Diagram of Watch Timer



Note Bit 0 of the Watch timer mode control register (WTM)

Figure 5-6. Block Diagram of Watchdog Timer



Note Bit 7 of the Watchdog timer mode control register (WDTM)

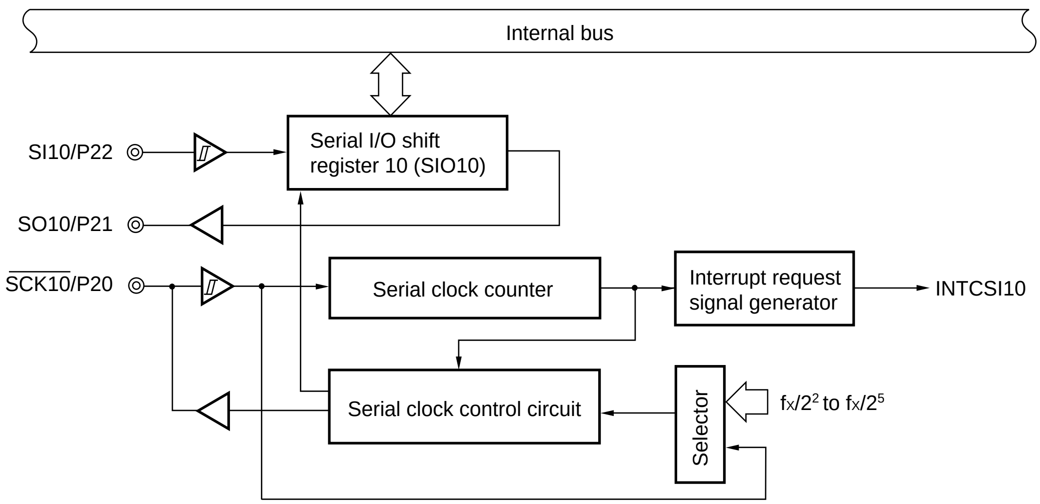
5.4 Serial Interface

One on-chip serial interface is provided.

SIO10 has the following two modes.

- Operation stop mode: Power consumption can be reduced.
- Three-wire serial I/O mode: A function to select the clock phase or data phase is incorporated.

Figure 5-7. Block Diagram of Serial Interface 10

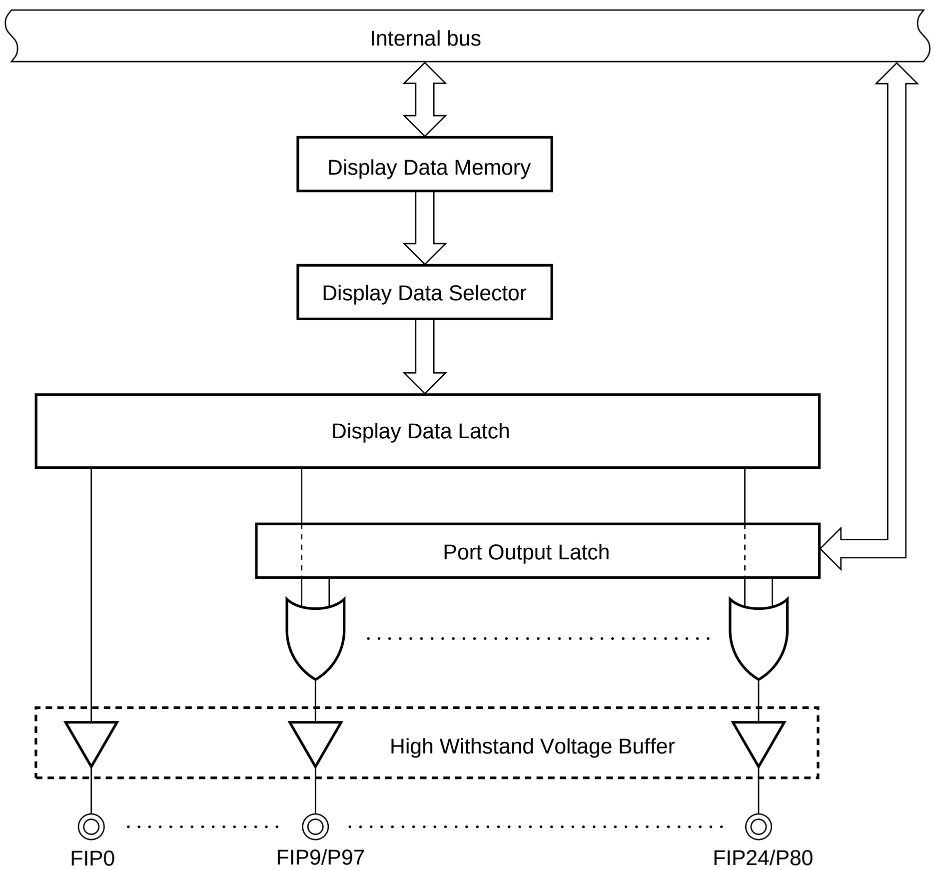


5.5 VFD Controller/Driver

A VFD controller/driver with the following function is incorporated.

(a) Total number of display outputs: 25. Output of 16 patterns is enabled.
(b) 96-bytes display RAM is provided to enable display signal output by reading display data automatically (direct memory access).
(c) A port pin which is not used for VFD display can be used as an output port or an I/O port (except for FIP0 to FIP8, which are VFD output only pins).
(d) The luminance can be adjusted in 8 stages with software.
(e) Hardware taking into consideration the key scan application is incorporated.
(f) Whether the key scan timing is inserted or not is selectable.
(g) A high withstand voltage output buffer (VFD driver) that can drive the VFD directly is incorporated.

Figure 5-8. Block Diagram of VFD Controller/Driver



6. INTERRUPT FUNCTION

A total of 13 interrupt sources are provided, divided into the following two types.

- Non-maskable interrupts: 1 source
- Maskable interrupts: 12 sources

Table 6-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with the interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTTM50	Remote control timer 50 input rising edge detection		000AH	(D)
	4	INTTM51	Remote control timer 50 input falling edge detection		000CH	
	5	INTTM52	Remote control timer 50 overflow	Internal	000EH	(B)
	6	INTKS	Key scan timing from VFD controller/driver		0010H	
	7	INTCSI10	Serial interface 10 transfer termination		0012H	
	8	INTTM80	Generation of matching signal of 8-bit timer 80		0014H	
	9	INTTM81	Generation of matching signal of 8-bit timer 81		0016H	
	10	INTWT	Watch timer interrupt		0018H	
	11	INTWTI	Interval timer interrupt		001AH	

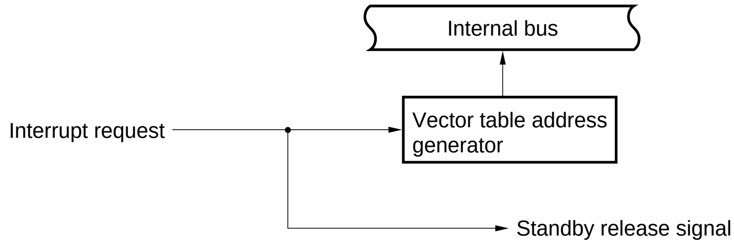
Notes 1. Priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 11 is the lowest order.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1.

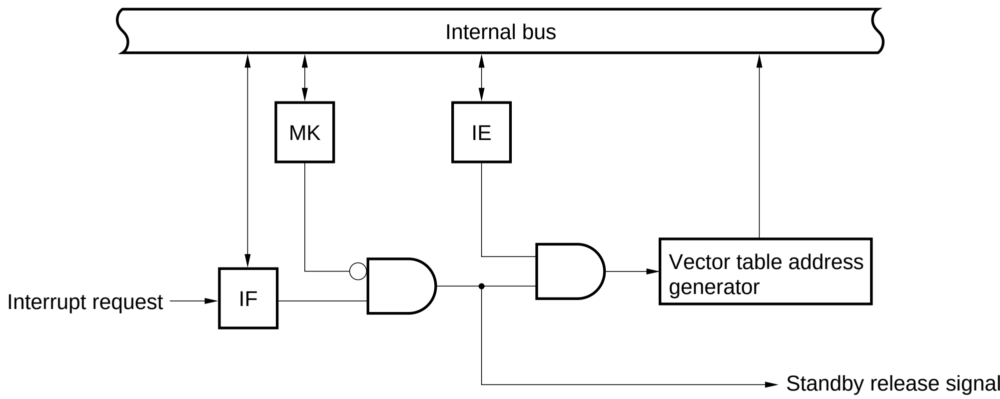
Remark As the interrupt source of the watchdog timer (INTWDT), either a non-maskable interrupt or a maskable interrupt (internal) can be selected.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

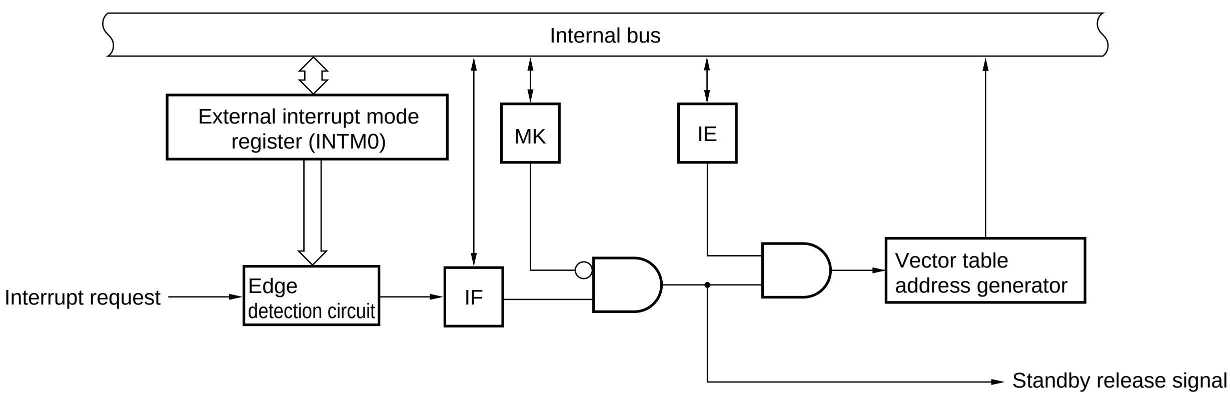
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



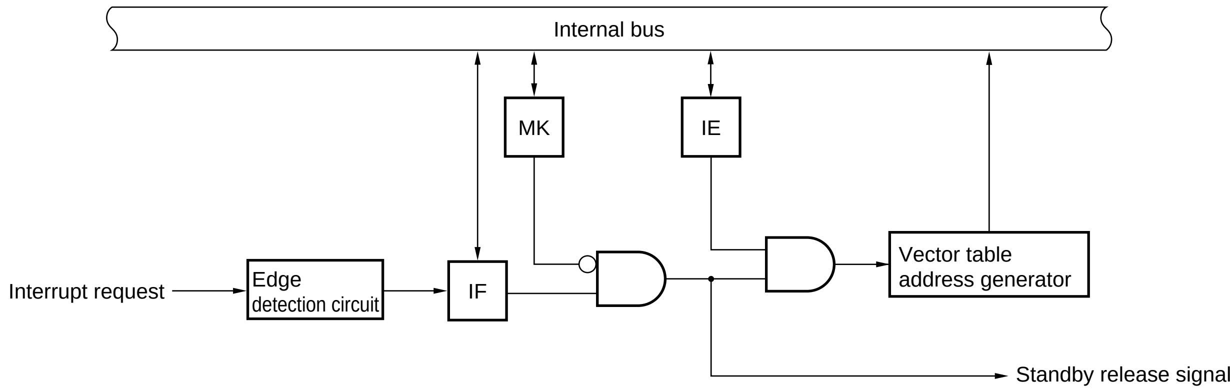
(C) External maskable interrupt (INTP0, INTP1)



IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTTM50, INTTM51)



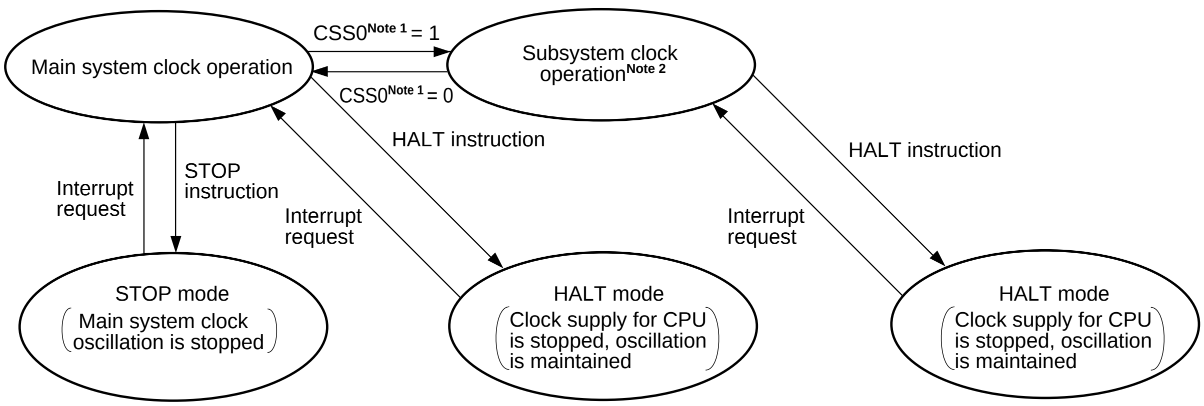
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Figure 7-1. Standby Function



Notes 1. Bit 4 of the sub-clock control register (CSS)

2. The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

8. RESET FUNCTION

The following two reset methods are available.

(1) External reset by the $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer detection runaway time.

9. MASK OPTION

- FIP17/P87 to FIP24/P80 mask option
  An on-chip pull-down resistor can be connected to V_{LOAD} by mask option.

10. INSTRUCTION SET OVERVIEW

This section lists the μPD789870 and μPD789871 instruction set.

10.1 Conventions

10.1.1 Operand identifiers and description methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 10-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7), AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH immediate data or label FE20H to FF1FH immediate data or label (even address only)
addr16 addr5	0000H to FFFFH immediate data or label (Only even addresses for 16-bit data transfer instructions) 0040H to 007FH immediate data or label (even address only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

10.1.2 Descriptions of the operation field

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt servicing flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
$\wedge$: Logical product (AND)
$\vee$: Logical sum (OR)
$\veebar$: Exclusive OR
—— : Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

10.1.3 Description of the flag operation field

(Blank): Not affected
0: Cleared to 0
1: Set to 1
$\times$: Set/cleared according to the result
R: Previously saved value is restored

10.2 Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
MOV	r. #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ←→ X			
	A, r Note 2	2	6	A ←→ r			
	A, saddr	2	6	A ←→ (saddr)			
	A, sfr	2	6	A ←→ (sfr)			
	A, [DE]	1	8	A ←→ (DE)			
	A, [HL]	1	8	A ←→ (HL)			
	A, [HL + byte]	2	8	A ←→ (HL+byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes **1.** Except r = A
2. Except r = A, X
3. Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp[Note]	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A+ (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A+ (addr16) +CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A+ (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×

Note Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r– 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags Z	AC	CY
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← $(PC + 3)_H$, (SP – 2) ← $(PC + 3)_L$, PC ← addr16, SP ←SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← $(PC + 1)_H$, (SP – 2) ← $(PC + 1)_L$, PC_H ← (00000000, addr5 + 1) PC_L ← (00000000, addr5) SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP -– 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC_H ← A, PC_L ← X			
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr.bit, $saddr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A.bit, $saddr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW.bit $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set Stop Mode			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

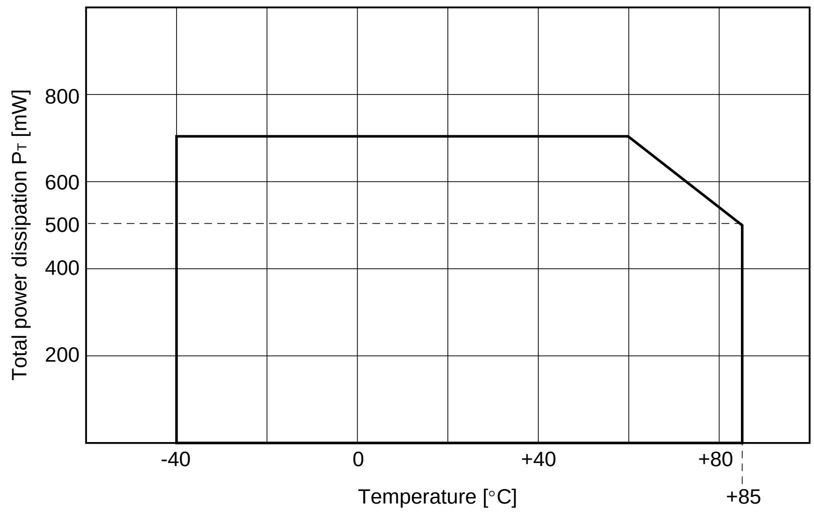
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	V_{LOAD}		V_{DD} –45 to V_{DD} + 0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P12, P20 to P25, X1, X2, XT1, XT2, $\overline{\text{RESET}}$, IC	–0.3 to V_{DD} + 0.3	V
	V_{I2}	FIP0 to FIP24	V_{DD} –45 to V_{DD} + 0.3	V
Output voltage	V_{O1}		–0.3 to V_{DD} + 0.3	V
	V_{O2}	FIP0 to FIP24	V_{DD} –45 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin for P00 to P07, P10 to P12, P20 to P25	–10	mA
		Total for P00 to P07, P10 to P12, P20 to P25	–30	mA
		Per pin for FIP0 to FIP24	–30	mA
		Total for FIP0 to FIP24	–300	mA
Output current, low	I_{OL}	Per pin for P00 to P07, P10 to P12, P20 to P25	30	mA
		Total for P00 to P07, P10 to P12, P20 to P25	160	mA
Total loss	P_T **Note**	T_A = –40 to +60 °C	700	mW
			500	mW
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Note Total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

Total power dissipation of the μPD789870 and μPD789871 can be divided to the following three. The sum of the three power dissipation should be less than the total power dissipation P_T rated in the above figure (80% or less of ratings is recommended.)

<1> CPU power dissipation: calculate V_{DD} (MAX.). x I_{DD} (MAX.).
<2> Output pin power dissipation: Power dissipation when maximum current flows into VFD output pins.
<3> Pull-down resistor power dissipation: Power dissipation by the Pull-down resistors incorporated in VFD output pins.

The following is how to calculate total power dissipation for the example in Figure 11-1.

Example Assume the following conditions:
V_{DD} = 5.5 V, 5.0-MHz oscillation
Supply current (I_{DD}) = 15.0 mA
VFD output: 11 grids x 10 segments (Blanking width = 1/16)
Maximum current at the grid pin is 15 mA.
Maximum current at the segment pin is 5 mA.
At the key scan timing, VFD output pin is OFF.
VFD output voltage: grid $V_{OD} = V_{DD} – 2$ V (voltage drop of 2 V)
Segment $V_{OD} = V_{DD} – 0.5$ V (voltage drop of 0.5 V)
Fluorescent display control voltage (V_{LOAD}) = – 35 V
Pull-down resistor = 30 kΩ

By placing the above conditions in calculation <1> to <3>, the total dissipation can be worked out.

<1> CPU power dissipation: 5.5 V x 15.0 mA = 82.5 mW

<2> Output pin power dissipation:

Grid $(V_{DD} - V_{OD}) \times \frac{\text{Total current value of each grid}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

$= 2\ V \times \frac{15\ mA \times 11\ Grids}{11\ Grids + 1} \times (1 - 1/16) = 25.8\ mW$

Segment $(V_{DD} - V_{OD}) \times \frac{\text{Total segment current value of illuminated dots}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

$= 0.5\ V \times \frac{5\ mA \times 31\ dots}{11\ Grids + 1} \times (1 - 1/16) = 6.1\ mW$

<3> Pull-down resistor power dissipation:

Grid $\frac{(V_{DD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{The number of grids}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

$= \frac{(5.5\ V - 2\ V - (-35\ V))^2}{30\ k\Omega} \times \frac{11\ Grids}{11\ Grids + 1} \times (1 - 1/16) = 42.5\ mW$

Sgment $\frac{(V_{DD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \frac{\text{The number of illuminated dots}}{\text{The number of grids + 1}} \times (1 - \text{Blanking width})$

$= \frac{(5.5\ V - 2\ V - (-35\ V))^2}{30\ k\Omega} \times \frac{31\ dots}{11\ Grids + 1} \times (1 - 1/16) = 129.2\ mW$

Total power dissipation = <1> + <2> + <3> = 82.5 + 25.8 + 6.1 + 42.5 + 129.2 = 286.1 mW

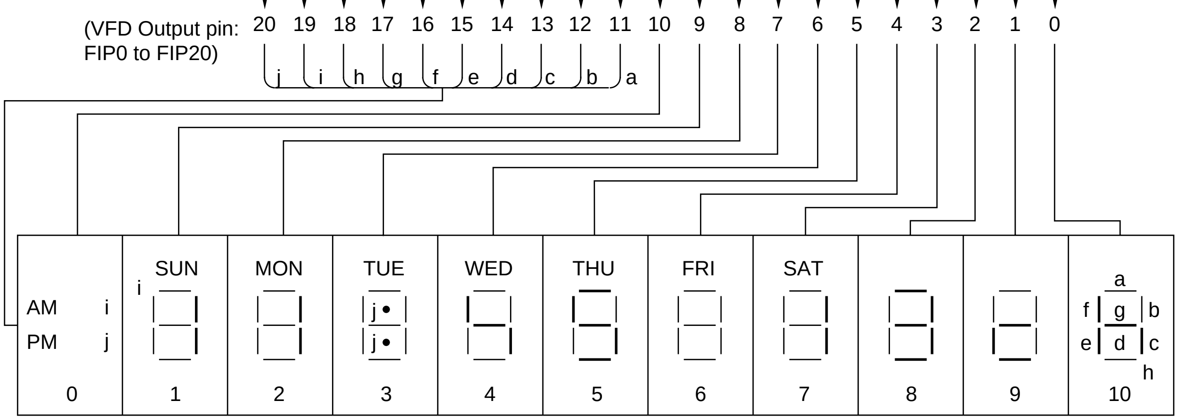
In this example, the total power dissipation does not exceed the rating of the total power dissipation, it is necessary to lower no problem in power dissipation.

However, when the total power dissipation exceeds the rating of the total power dissipation, it is necessary to lower the power dissipation. To reduce power dissipation, reduce the number of pull-down resistor.

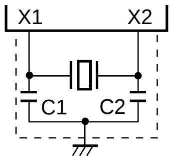
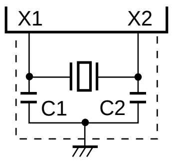
Figure 11-1. Display Example of 10 Segments-11 Digits

Display Data Memory

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
FA02H, FA01H, FA00H	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	T0
FA09H, FA08H, FA07H	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	T1
FA10H, FA0FH, FA0EH	0	0	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	T2
FA17H, FA16H, FA15H	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	T3
FA1EH, FA1DH, FA1CH	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	T4
FA25H, FA24H, FA23H	0	0	0	1	1	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	T5
FA2CH, FA2BH, FA2AH	0	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	T6
FA33H, FA32H, FA31H	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	T7
FA3AH, FA39H, FA38H	0	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	T8
FA41H, FA40H, FA3FH	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	T9
FA48H, FA47H, FA46H	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	T10



Main System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

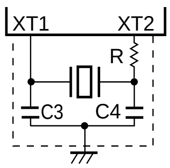
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s

Notes 1. Indicates only oscillator characteristics. Refer **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	P00 to P07, P10 to P12, P20 to P25	Per pin			–1	mA
			Total for all pins			–15	mA
Output current, low	I_{OL}	P00 to P07, P10 to P12, P20 to P25	Per pin			10	mA
			Total for all pins			80	mA
Output voltage, high	V_{OH}	P00 to P07, P10 to P12, P20 to P25	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			V_{DD} = 2.7 to 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	P00 to P07, P10 to P12, P20 to P25	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 2.7 to 5.5 V, I_{OL} = 400 μA			0.5	V
Input voltage, high	V_{IH1}	P00 to P07, P10 to P12, P21		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, P20, P22 to P25		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P12, P21		0		0.3 V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$,P20, P22 to P25		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P12, P20 to P25, $\overline{\text{RESET}}$	V_I = V_{DD}			3	μA
	I_{LIH2}	X1, X2, XT1, XT2				20	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P12, P20 to P25, $\overline{\text{RESET}}$	V_I = 0 V			–3	μA
	I_{LIL2}	X1, X2, XT1, XT2				–20	μA
Output leakage current, high	I_{LOH}	P00 to P07, P10 to P12, P20 to P25, FIP0 to FIP8, FIP9/P97 to FIP16/P90, FIP17/P87 to FIP24/P80	V_O = V_{DD}			3	μA
Output leakage current, low	I_{LOL1}	P00 to P07, P10 to P12, P20 to P25	V_O = 0 V			–3	μA
	I_{LOL2}	FIP0 to FIP8, FIP9/P97 to FIP16/P90, FIP17/P87 to FIP24/P80				–10	μA
VFD output current	I_{OD}	FIP0 to FIP24, V_{DD} = 4.5 to 5.5 V	V_{OD} = V_{LOAD}–2.0 V			–15	mA
Software pull-up resistor	R_1	V_{IN} = 0 V, P00 to P07, P10 to P12, P20 to P25		50	100	200	kΩ
Mask option pull-down resistor (V_{SS0} connection)	R_3	FIP17/P87 to FIP24/P80		15	35	90	kΩ
Mask option pull-down resistor (V_{LOAD} connection)	R_4	FIP17/P87 to FIP24/P80		30	60	135	kΩ
On-chip pull-down resistor (V_{LOAD} connection)	R_2	FIP0 to FIP8, FIP9/P97 to FIP16/P90		30	60	135	kΩ

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10% Note 2		2.0	4.0	mA
			V_{DD} = 3.0 V ± 10% Note 3		0.6	1.2	mA
	I_{DD2} Note 1	5.0-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10% Note 3		1.1	2.2	mA
			V_{DD} = 3.0 V ± 10% Note 3		0.4	0.8	mA
	I_{DD3} Note 1	32.768-kHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10%		70	160	μA
			V_{DD} = 3.0 V ± 10%		30	90	μA
	I_{DD4} Note 1	32.768-kHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10%		25	55	μA
			V_{DD} = 3.0 V ± 10%		5	25	μA
	I_{DD5} Note 1	32.768-kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	10	μA
			V_{DD} = 3.0 V ± 10%		0.05	5	μA

Notes 1. The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) is not included.

2. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. During low-speed mode operation (when PCC is set to 02H)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	0.4		8	μs
		Operation based on the subsystem clock	114	122	125	μs
TI input high-/low-level width	t_{TIH}, t_{TIL}		2/Fcount +0.2			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0, INTP1	10			μs
$\overline{RESET}$ input low-level width	t_{RSL}		10			μs

Remark Fcount is a count clock selected by 8-bit remote control timer 50.

(2) Serial interface 10 (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK10}$...Internal clock)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK10}$ high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2–50			ns
SI10 setup time (to $\overline{SCK10}$ ↑)	t_{SIK1}		150			ns
SI10 hold time (from $\overline{SCK10}$ ↑)	t_{KSI1}		400			ns
SO10 output delay time from $\overline{SCK10}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		200	ns

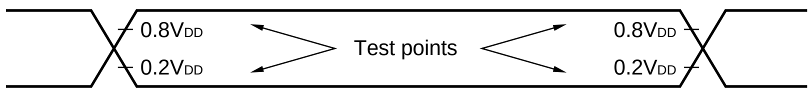
Note R and C are the load resistance and load capacitance of the SO10 output line.

(b) 3-wire serial I/O mode ($\overline{SCK10}$...External clock)

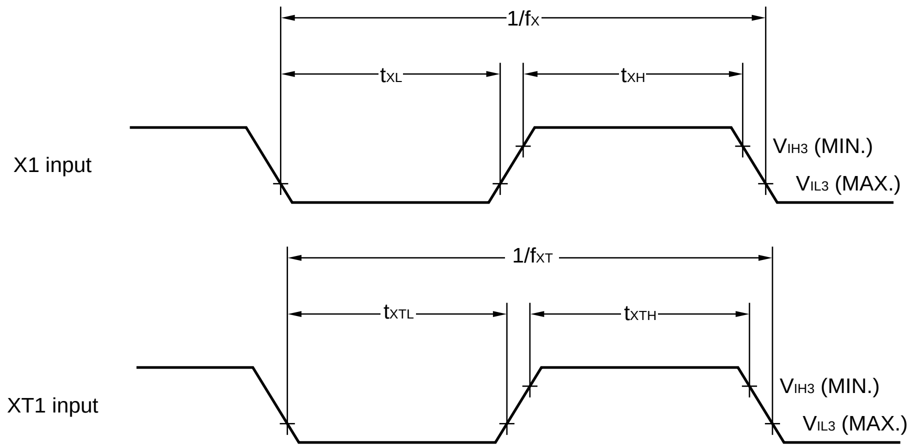
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK10}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI10 setup time (to $\overline{SCK10}$ ↑)	t_{SIK2}		100			ns
SI10 hold time (from $\overline{SCK10}$ ↑)	t_{KSI2}		400			ns
SO10 output delay time from $\overline{SCK10}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns

Note R and C are the load resistance and load capacitance of the SO10 output line.

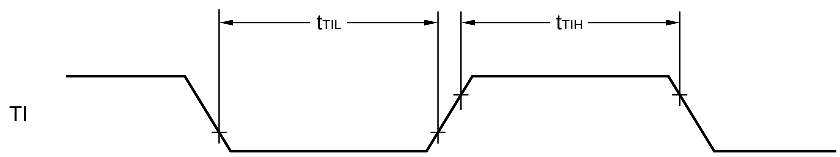
AC Timing Measurement Points (excluding the X1 and XT1 inputs)



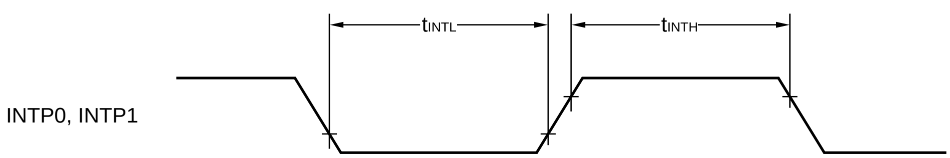
Clock Timing



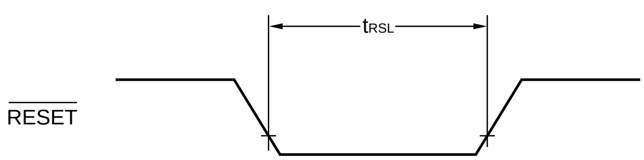
TI Timing



Interrupt Input Timing

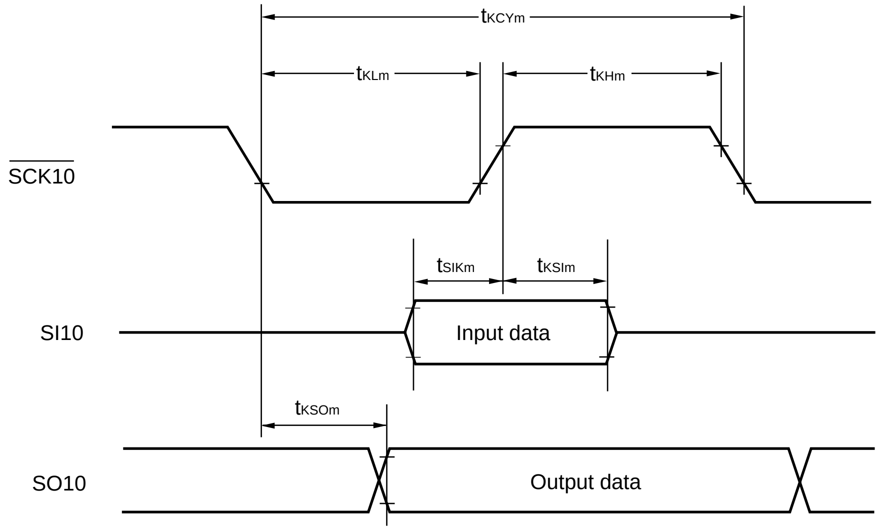


$\overline{\text{RESET}}$ Input Timing



Serial Transfer Timing

3-wire serial I/O mode:



Remark m = 1, 2

Data Memory Stop Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

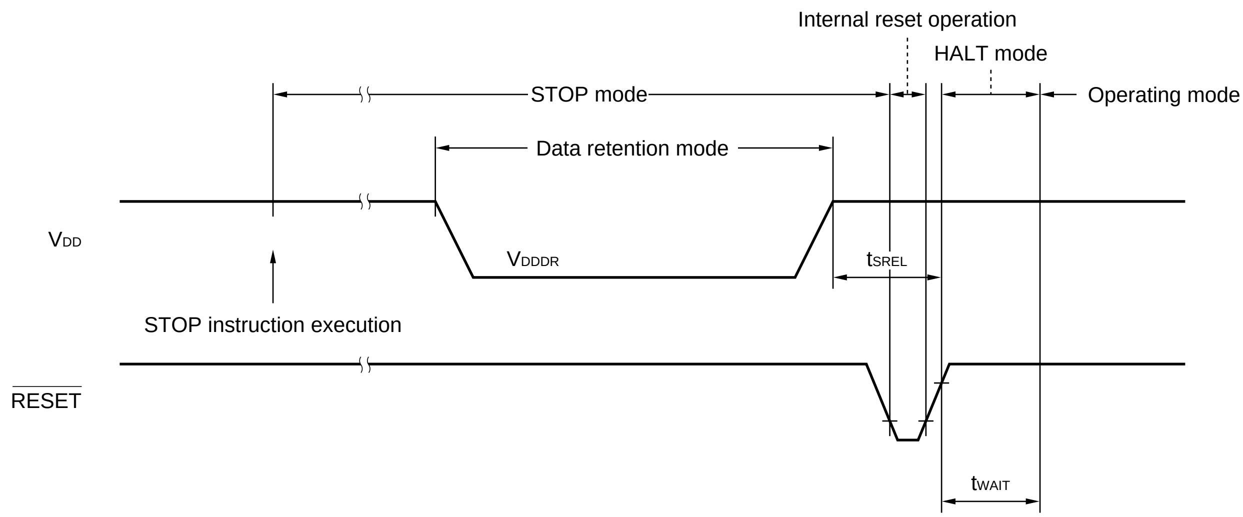
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

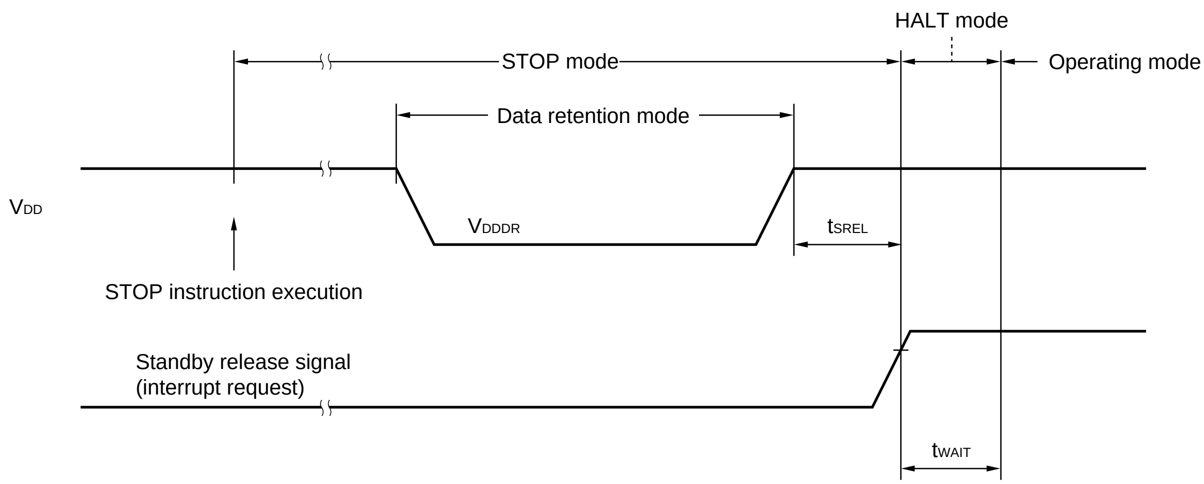
2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected.

Remark f_X: Main system clock oscillation frequency

Data Retention Timing (STOP Mode Release by RESET)

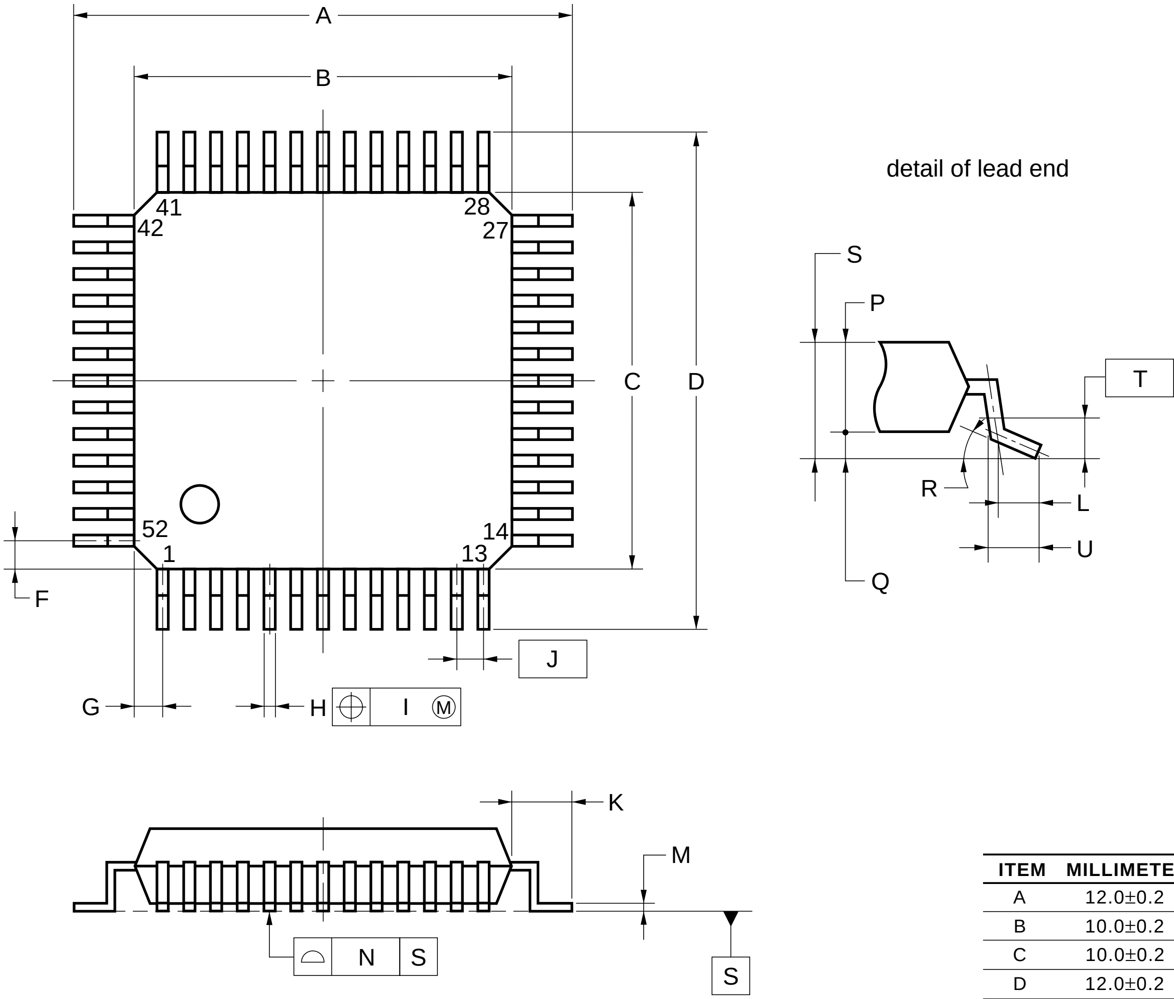


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



12. PACKAGE DRAWING

52-PIN PLASTIC LQFP (10x10)



ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.1
G	1.1
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.05}$
N	0.10
P	1.4
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.5±0.1
T	0.25
U	0.6±0.15

S52GB-65-8ET-1

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD789870 and μPD789871.

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789872[Notes 1, 2, 3]	Device file for μPD789871 Subseries
CC78K0S-L [Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated for on-chip flash memory microcontrollers
FA-52GB[Note 4]	Flash memory programming adapter for 52-pin plastic QFP (GB-8ET type)

Debugging Tools(1/2)

IE-78K0S-NS In-circuit emulator	In-circuit emulator used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter	Adapter used to supply power from a 100- to 240-V AC outlet
IE-70000-98-IF-C Interface adapter	Adapter required when using the PC-9800 series (excluding notebook PCs) as the host machine for the IE-78K0S-NS (C bus supported)
IE-70000-CD-IF-A PC card/interface	PC card and interface cable required when using a notebook PC as the host machine for the IE-78K0S-NS (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter	Adapter required when using an IBM PC/AT™ or compatible as the host machine for the IE-78K0S-NS (ISA bus supported)
IE-70000-PCI-IF Interface adapter	Adapter required when using a PC equipped with a PCI bus as the host machine for the IE-78K0S-NS
IE-789872-NS-EM1 Emulation board	Emulation board used to emulate the peripheral hardware specific to the device. This is used in combination with the in-circuit emulator.
NP-52GB[Note 4] Emulation probe	Board to connect an in-circuit emulator to the target system.
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789872[Notes 1, 2]	Device file for μPD789871 Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on the PC-9800 series (Japanese Windows™)

2. Based on IBM PC/AT and compatibles (Japanese Windows/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)

4. Product made by and available from Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789872.

APPENDIX B. RELATED DOCUMENTS

The related document indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789870, 789871 Preliminary Product Information	This manual
μPD78F9872 Preliminary Product Information	U14880E
μPD789871 Subseries User's Manual	To be prepared
78K/0S Series Instruction User's Manual	U11047E

Document Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Parts User Open Interface Specifications	To be Prepared
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows based	Operation	U14910E
IE-78K0S-NS In-circuit Emulator		U13549E
IE-789872-NS-EM1 Emulation Board		To be Prepared

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
OS for 78K/0S Series MX78K0S	Fundamental	U12938E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Device	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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