# Intel® IXF30007

## Enhanced Digital Wrapper for Ultra Long-Haul Transmission Systems

Intel® Internet Exchange Architecture

The Intel® IXF30007 is a fully compliant G.709 digital wrapper device that covers most Optical Transport Network (OTN) applications on a single chip. Built on the technology developed for the Intel® IXF30001 (FEC100), the first 10Gbit/s FEC device in the market, the IXF30007 supports enhanced Forward Error Correction (FEC) using concatenated RS-codes that can be set to up to 9dB using various parameters.

The IXF30007 is designed for optical transmission applications where the coding gain reached with standard forward error correcting (FEC) algorithms (ITU-T G.975, ITU-T G.709) is not sufficient. The core FEC technology concatenates two Reed-Solomon codes that are configurable in both error correction capability and block length, delivering a coding gain configuration between zero and 30 percent overhead.

The IXF30007 consists of two completely separated signal paths referred to as north and south paths. While the north path is primarily designed to operate as a line receiver, the south path may be used as a line transmitter. The IXF30007 forms the basis of a single chip transponder application and, using integrated bridges between both paths, may be configured as a regenerator and provide APS support.

The Intel IXF30007 provides all basic functions required for an OTN system, and appropriate configuration of the outer code ensures compliance with the digital signal wrapping technique defined by ITU-T. With integrated overhead processing circuitry and different types of payload mapping, the IXF30007 is a key component in wrapper-based transparent operations, administration, maintenance and provisioning of optical networks.

### Flexible Design

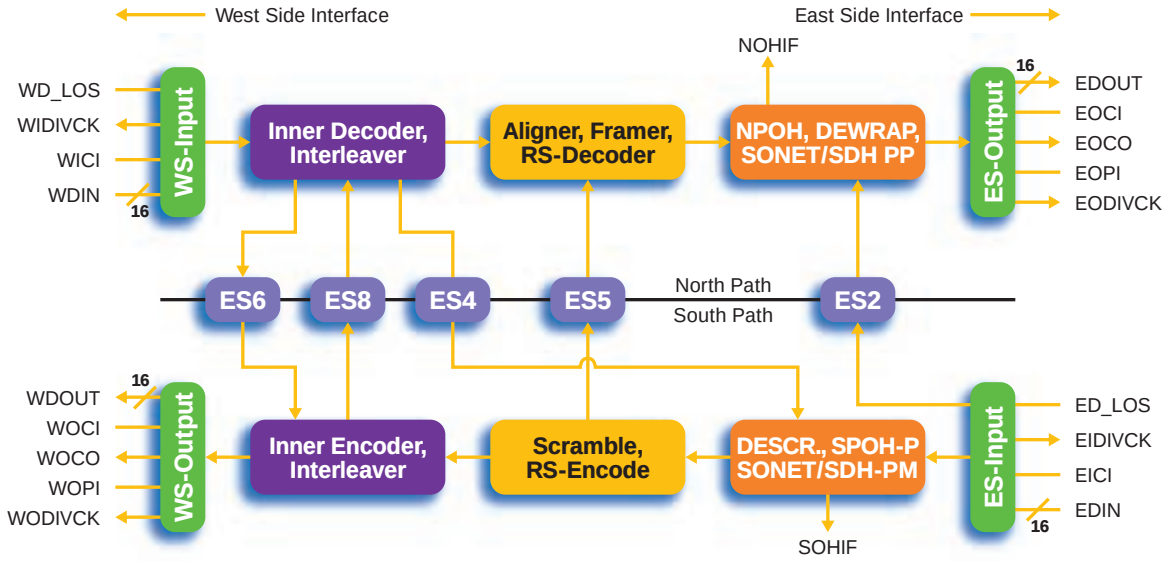
Supporting both asynchronous and synchronous mapping schemes, the IXF30007 has additional features for SONET/SDH data streams such as a Performance Monitor (PM) and post processor. The device I/Os are also compliant with OIF-standards.


Synchronous and asynchronous mapping of STM-64 streams is supported for SDH payload data, as proposed by ITU-T G.709. In addition to ITU-T G.709 compliant framing, the IXF30007 may also be combined with any other outer code configuration.

Outer and inner RS-Codes are concatenated in the IXF30007 through the use of an interleaver, enabling correction of high input-error-rates as well as burst errors typically found in multiple-wavelength DWDM systems.

The integrated, nonintrusive PM in the south path can be used to check incoming payload signal quality by monitoring the B1 and B2 values contained in the regenerator section and line overhead. Monitoring also comprises J0 string extraction and mapping of up to four configurable OH bytes to the processor interface. On the north path, an integrated SOH post processor allows up to two configurable bytes. Should severe transmission error occur, such as loss of signal or wrapper frame synchronization, received SONET/SDH data may be replaced by AIS frames.

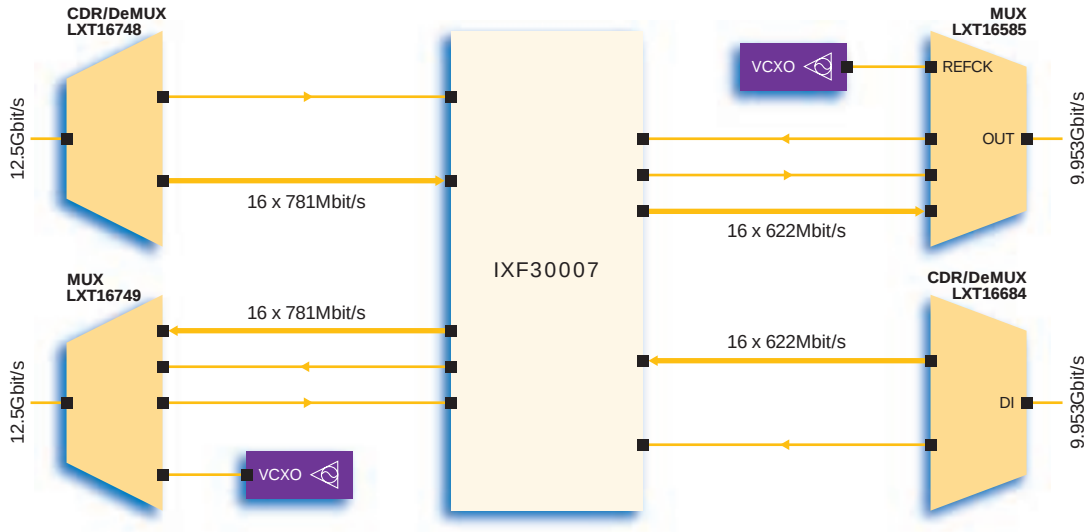
IXF30007 is controlled by a processor interface allowing event-driven communication to reduce processor load. An included IEEE 1149.1 (JTAG) interface may be used to access the internal register bank.




## Features

## Benefits

| Features | Benefits |
|---|---|
| ■ Flexible digital wrapper for OTN with ITU-T G.709 compliance, including enhanced Forward Error Correction (FEC). | ■ Usable in many locations and applications within an OTN. Future-proof due to compliancy with OTN standards, as well as downward compatibility. |
| ■ Wide coverage of OTN overhead functions implemented in hardware. | ■ Reduces costs, space, power and software development time. |
| ■ 9dB of coding gain. | ■ Optimum performance for ultra long-haul applications, allowing use of cost-optimized optical solutions in metro networks. |
| ■ OC-192/STM-64 client type processing related to OTN functions and applications. | ■ Compliance with existing standards, resulting in reduced development time. |
| ■ Flexible overhead rate between 0 percent and 30 percent using configurable error correction capability and block length for codes<br>• Inner code: *l*=200…255, *t*=0…24<br>• Outer code: *l*=200…255, *t*=0…12 | ■ High flexibility, allowing proprietary standards as well as configurations that are compatible with ITU-T G.709, generic ITU-T G.975 and IXF30001/IXF30003. Ability to correct large burst errors in multiple-wavelength DWDM systems. |
| ■ OC-192/STM-64 SONET/SDH performance monitor (B1, B2, J0, general purpose) and post processor (AIS insertion). | ■ No additional performance monitor device required; basic SONET/SDH functionality downstream. |
| ■ Downward compatible to Intel® IXF30003 (FEC100) and Intel® IXF30005 (WRAP100). | ■ Eases migration pass, allows bridging between different standards. |
| ■ Bidirectional device for single chip transponder operation (synchronous or asynchronous). | ■ Compact system design, reduced cost, lower power consumption, multiple clocking options available. |
| ■ OIF-compliant LVDS Inputs/Outputs. | ■ Allows use of SERDES components provided by Intel and 3rd party vendors. |
| ■ Low power consumption (6W maximum). | ■ Eases mechanical systems design and power management. |




## Key Applications

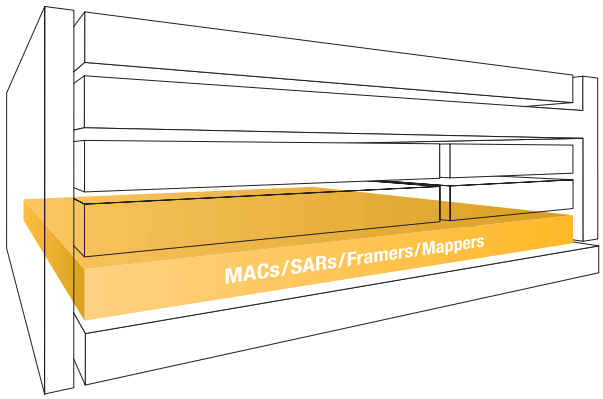
- Ultra long-haul optical communication systems
- Submarine cable network elements
- Low-cost metro networks
- ITU G.709 compliant transport networks
- Increased bandwidth in existing systems
- Bridging functions between OTN-compliant networks and legacy network elements

## Support Collateral

- IXF30007 Data Sheet
- IXD80103 Evaluation System with GUI
- OTN/G.709 Optical Transport Network Node Interface Elements/Interconnects Application Brief
- SONET/SDH Aggregation to OTN Application Brief
- FAQs

## Intel® Internet Exchange Architecture

Intel® Internet Exchange Architecture is an end-to-end family of high-performance, flexible and scalable hardware and software development building blocks designed to meet the growing performance requirements of today's networks. Based on programmable silicon and software building blocks, Intel® IXA solutions enable faster development, more cost-effective deployment and future upgradability of network and communications systems. Additional information can be found at www.intel.com/IXA



## Intel Access

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| Developer's Site | http://developer.intel.com |
| Intel® Internet Exchange Architecture Home Page | http://www.intel.com/IXA |
| Networking Components Home Page | http://developer.intel.com/design/network |
| Other Intel Support: | http://developer.intel.com/design/litcentr |
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