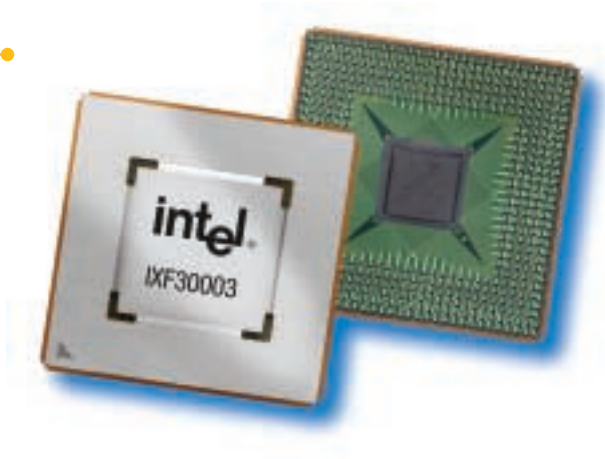
Intel® IXF30003 10Gbit/s Forward Error Correction

Coding and Decoding for 10Gbit/s Fiber-Optic Transmission

Intel® Internet Exchange Architecture

Product Description

A simple Forward Error Correction (FEC)-protected optical transmission channel consists of three different types of nodes: FEC sender module, FEC regenerator, and FEC receiver. Payload data is wrapped into the optical layer by the sender module and sent over an optical transmission link. The FEC regenerator corrects received data before it is transmitted to the next node, and the FEC receiver terminates the wrapped transmission and outputs client data.



The Intel® IXF30003 is a FEC transponder device that provides coding and decoding for a 10Gbit/s fiber optical transmission protected by forward error correction. Based on the out-of-band FEC scheme recommended by ITU-T G.975, the IXF30003 offers a substantial gain in the transmission quality of optical networks running at 10Gbit/s, especially in DWDM systems. Due to the out-of-band nature, the IXF30003 does not impose any restrictions on payload data type and is optimized for low power.

Similar in design to the Intel® IXF30001, the IXF30003 additionally provides an integrated performance monitor for SONET/SDH payload data. This can be used to check payload signal quality by monitoring B1 or B2 values contained in the SONET/SDH overhead, as well as comprising JO string extraction. For added flexibility and reduced board space, the IXF30003 may be used as the FEC sender, FEC receiver, FEC transceiver, or an error-correcting regenerator.

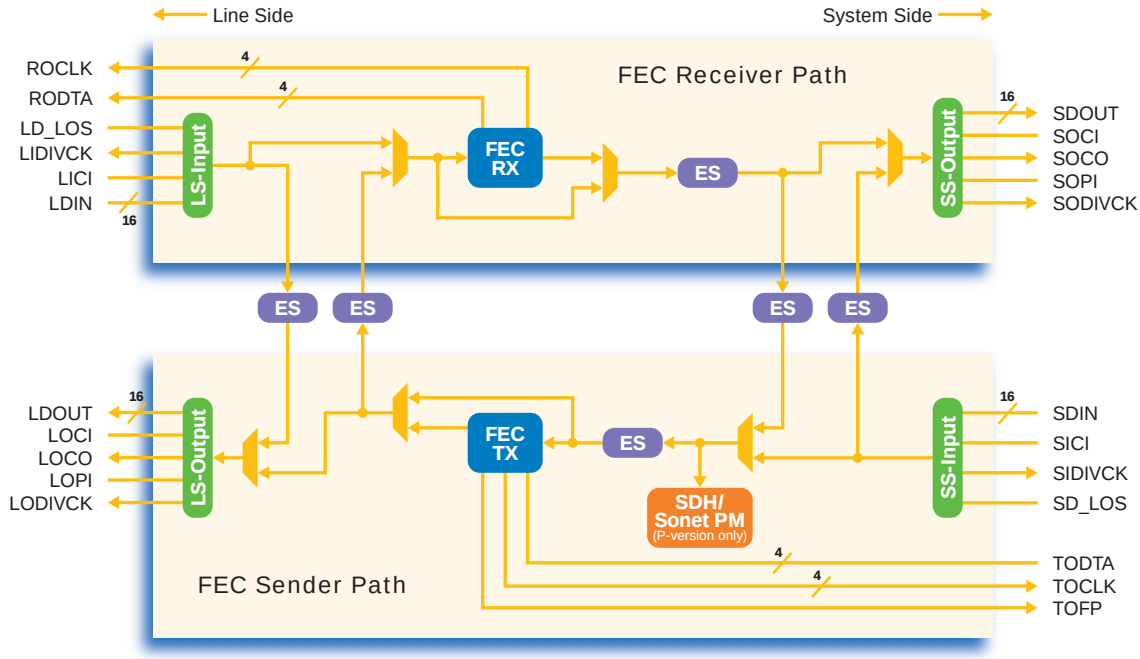
The Intel IXF30003 opens the door to wrapper-based transparent operation, administration, maintenance and provisioning in optical networks. The integrated error statistics circuitry and serial optical overhead channels (OCOH) allow remote management of the optical network. Manufactured in a low-power 0.18µ CMOS technology, the IXF30003 can be controlled using an 8-bit processor interface, which allow high event-driven communication and reduced processor load.

Key Applications

- SDH STM-64
- SONET OC-192
- Submarine Systems
- Optical Transport Networks

Support Collateral

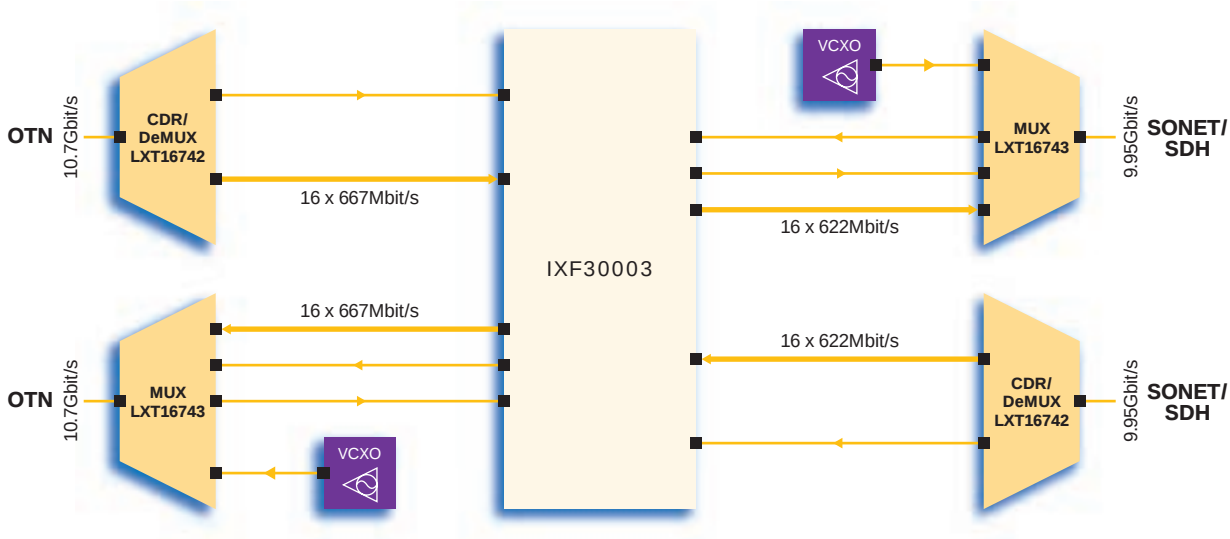
- Evaluation Boards
- GUI Software
- IXF30003 Data Sheet
- FAQs
- Application Notes



Device Architecture

The Intel IXF30003 is a full FEC transceiver with four high-speed interfaces and the following modules:

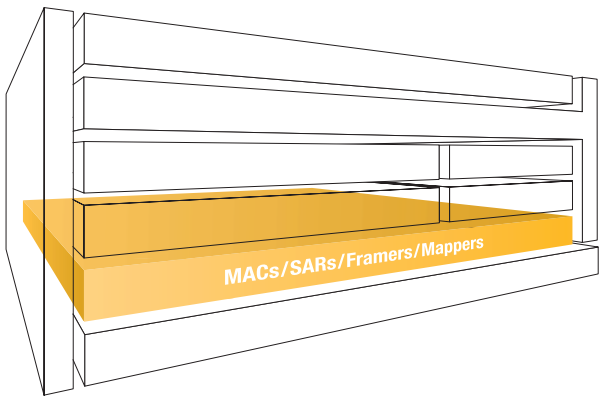
- **Receiver.** The FEC receiver module first recovers the FEC frame structure, performs de-scrambling, error correction, and removal of error correction information from the RS code.
- **Transmitter.** Received client data or data entering the SDIN is transferred to the wrapped data rate; the FEC frame is created from client data, the overhead channels, and error protection symbols; and data is scrambled and sent out.
- **SONET/SDH Performance Monitor.** SONET/SDH payload data may be monitored parallel to the FEC processing using B1 and B2 transmission error detection and extraction of JO trace message.
- **Loopback.** A loopback from SDIN to SDOUT may be activated, requiring the SICI and SOCI interface clocks be the same frequency, with some drift. For test purposes, the LDOUT may also be connected directly to the LDIN.
- **Processor Interface.** An integrated 8-bit processor interface allows device control and surveillance, supporting both synchronous and asynchronous operation.
- **Overhead Channels.** Four independent overhead channels, separate from the client data transmission, each transferring up to 5.2Mbit/s raw data.



Features	Benefits
■ Full, independent receive and transmit path	■ Allows single chip bidirectional line cards, for reduced real estate and lower power
■ Four OIF compliant LVDS 622/666Mbit interfaces	■ Industry-standard interfacing on line and system side, simple interfacing to chipsets and framers
■ 576 BGA package, 0.18µ CMOS 1.8V technology, 3.5W maximum power consumption	■ Superior thermal performance, low-power technology. No heat sink required for systems with airflow, reduced real estate on Z-axis
■ 16-channel RS (255,239) error protection scheme including scrambling according to G.975	■ Industry-proven, out-of-band algorithm
■ SONET/SDH performance monitoring	■ Allows on-chip QA of SONET/SDH traffic and reduces chip count in backbone applications
■ Payload independent	■ No restrictions on payload data types
■ Coding gain of approximately 6dB	■ Covers longer distances between optical amplifiers; allows more optical processing elements in the optical path; increased reliability of the transmission link
■ Error statistics on bit- and byte-error level	■ Versatile use of error statistics, monitoring transmission quality
■ May be operated as sender, receiver, transceiver, or regenerator	■ Added flexibility and reduced board space savings
■ SONET/SDH B1, B2, and JO performance monitoring on sender side	■ Checks payload signal quality
■ Device controllable via 8-bit processor interface	■ Reduced processor load for event-driven communication

Intel® Internet Exchange Architecture

Intel® Internet Exchange Architecture is an end-to-end family of high-performance, flexible and scalable hardware and software development building blocks designed to meet the growing performance requirements of today's networks. Based on programmable silicon and software building blocks, Intel® IXA solutions enable faster development, more cost-effective deployment and future upgradability of network and communications systems. Additional information can be found at www.intel.com/IXA



Intel Access

Developer's Site	http://developer.intel.com
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Networking Components Home Page	http://developer.intel.com/design/network
Other Intel Support:	http://developer.intel.com/design/litcentr
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