XC651A Series

PFM Controlled,Step - Up DC/DC Converter +Multi Voltage Detector

- ◆CMOS Low Power Consumption
- ◆PFM Controlled, Step-Up DC/DC Converter
- ◆5 Level Window Comparator
- ◆Voltage Detector × 2 (Independent Power Supply)
- ◆TSSOP-16 Package

■Applications

- ●Battery Powered Equipment
- ●Various Portable Equipment

■General Description

The XC651A series are step-up DC/DC converter and multi voltage detector IC s. CMOS processes and laser trimming technology provide high accuracy and low power consumption.
The XC651A comprises of a PFM controlled step-up DC/DC converter, a voltage detector with 4 x 5 level window comparators built-in, plus 2 other voltage detectors.
The step-up DC/DC converter's EN pin (chip enable) provides power consumption savings when the step-up operations are not operating (stand-by mode).
The series is available in a small TSSOP-16 package.

■Features

Independent power supply for each built-in block :
Each of the following built-in blocks is operated by a separate power supply :
PFM controlled, step-up DC/DC converter (PFM DC/DC)
5 level window comparator (MWVD)
Negative Logic : XC651A3 Series
Positive Logic : XC651A4 Series
Voltage detector 1 with built-in delay circuit (VD1)
Voltage detector 2 (VD2)

Highly accurate set-up voltage :
PFM controlled, step-up DC/DC converter : set-up voltage accuracy ±2.5%
5 level window comparator : set-up voltage accuracy ±2%
Voltage detectors 1, 2 : set-up voltage accuracy ±2%

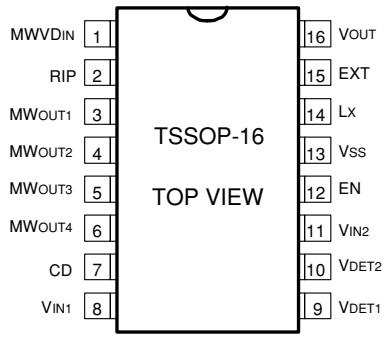
Set-up voltage range :
PFM controlled, step-up DC/DC converter : 2.0V ~ 3.0V (selectable in 0.1V steps)
5 level window comparator : 1.1V ~ 2.5V * (selectable in 0.1V steps)
Voltage detectors 1, 2 : 0.9V ~ 3.0V (selectable in 0.1V steps)

Operational voltage range :
0.9V ~ 6.0V

Small Package :
TSSOP-16

* Note : The set-up voltage of the 5 level window comparator cannot be freely set-up due to the limitations of the circuit. Please also note that the set-up voltage range of MWVD1 is 1.0V ~ 1.8V.

■Pin Configuration



■Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION
1	MWVDIN	MWVD detect, MWVD current
2	RIP	MWVD ripple exclusion capacitor connection
3	MWOUT1	MWVD output 1
4	MWOUT2	MWVD output 2
5	MWOUT3	MWVD output 3
6	MWOUT4	MWVD output 4
7	CD	VD1 delay time set-up capacitor connection
8	VIN1	VD1 detect, VD1 current
9	VDET1	VD1 output
10	VDET2	VD2 output
11	VIN2	VD2 detect, VD2 current
12	EN	DC/DC enable
13	VSS	Ground pin (common)
14	Lx	DC/DC built-in transistor switch output
15	EXT	DC/DC external transistor drive output
16	VOUT	DC/DC output voltage monitor, DC/DC current

■Product Classification

●Ordering Information

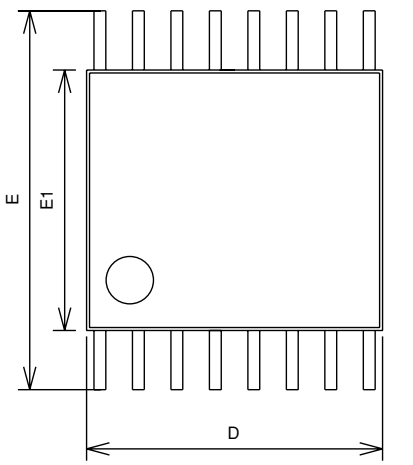
XC651A □□□□□□

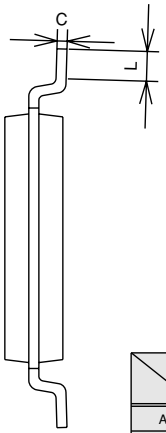
① ②③

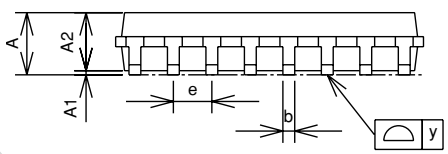
SYMBOL	DESCRIPTION	SYMBOL	DESCRIPTION
①	Voltage Characteristics : Based on internal standards	②	Package Type V：TSSOP−16
		③	Device Orientation R：Em bossed Tape (Right) L：Em bossed Tape (Left)

■Packaging Information

●TSSOP-16



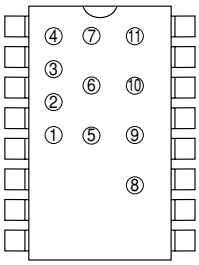




	SIZE mm		
	MIN	TYP	MAX
A	—	—	1.10
A1	0.03	0.07	0.10
A2	0.95	—	1.05
b	0.15	0.22	0.30
C	0.12	0.17	0.22
D	4.9	5.10	5.30
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.40	0.50	0.60
y	—	—	0.10

■Marking

●TSSOP-16



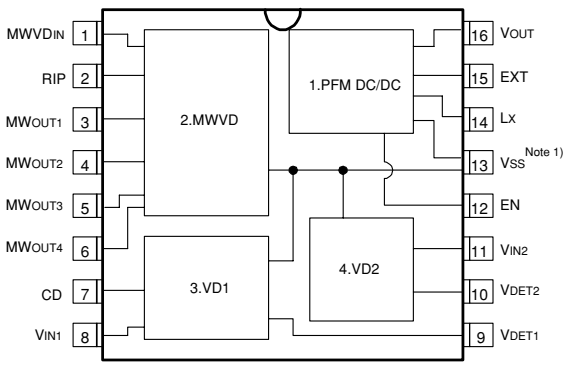
TSSOP-16
(TOP VIEW)

①～④: Represents the diffusion lot.
⑤～⑪: Represents the product series

Example) XC651A1004VR
④ ～ ⑪

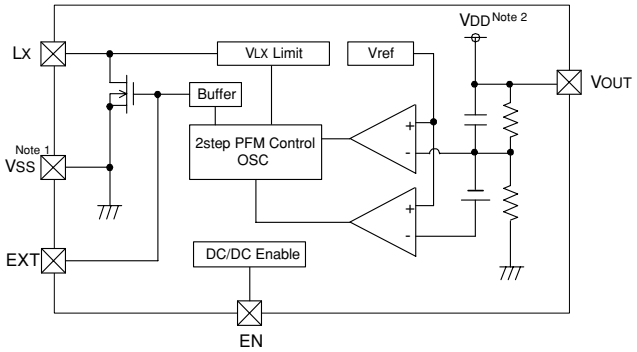
■Block Diagrams

1) Overall Composition



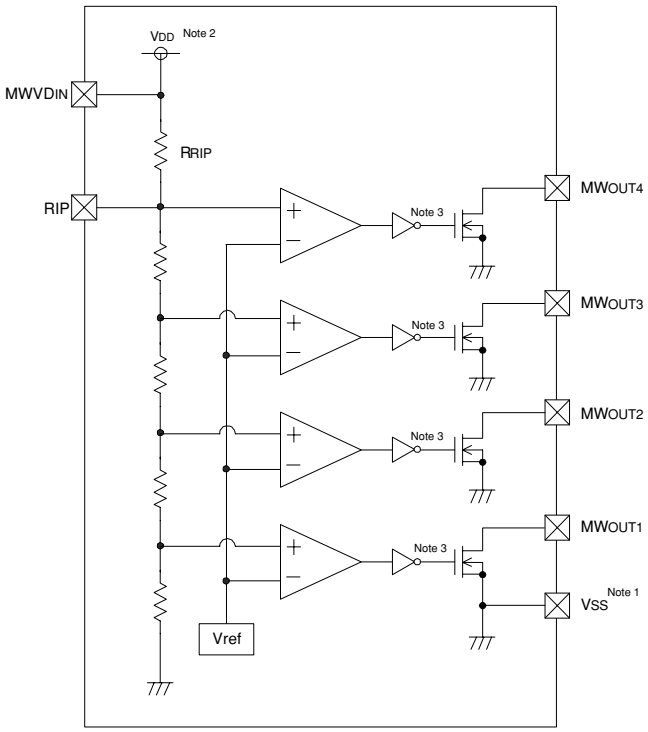
Note 1 : The VSS pin is common to each block.
Note 2 : The VDD pin is independent of each block.

2) PFM DC/DC



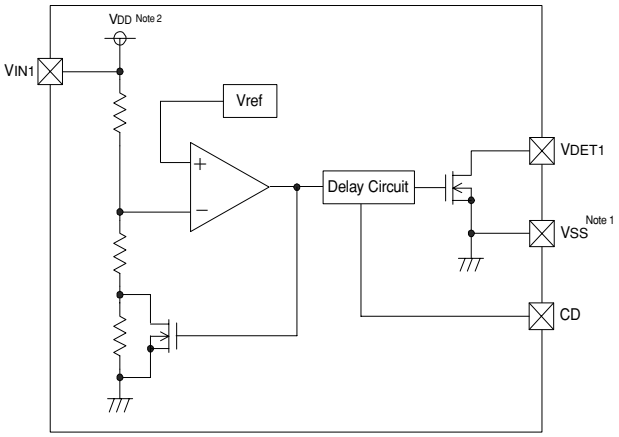
Note 1 : The VSS pin is common to each block.
Note 2 : VDD is independent for each block.

3) MWVD



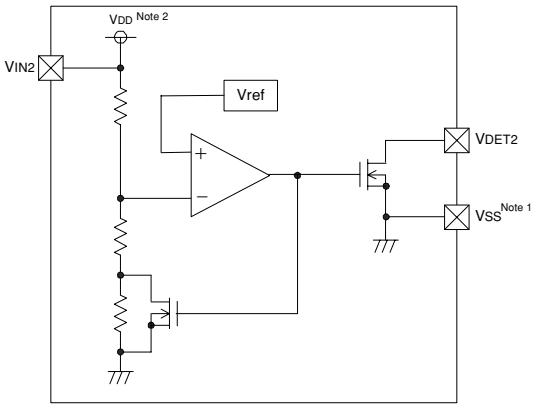
Note 1 : The VSS pin is common to each block.
Note 2 : VDD is independent for each block.
Note 3 : Applies to the XC6514 Series (Positive Logic) only.

4) VD 1



Note 1 : The VSS pin is common to each block.
Note 2 : VDD is independent for each block.

5) VD 2



Note 1 : The VSS pin is common to each block.
Note 2 : VDD is independent for each block.

■Absolute Maximum Ratings

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	UNITS
Output Voltage	V_{OUT}	9	V
Lx Pin Voltage	V_{LX}	9	V
Lx Pin Current	I_{LX}	400	mA
EXT Pin Voltage	V_{EXT}	-0.3 ~ V_{OUT} + 0.3	V
EXT Pin Current	I_{EXT}	±50	mA
EN Input Voltage	V_{EN}	-0.3 ~ V_{OUT} + 0.3	V
MWVDIN Input Voltage	$MWVD_{IN}$	9	V
RIP Input Voltage	V_{RIP}	-0.3 ~ $MWVD_{IN}$ + 0.3	V
MWOUT Output Voltage	V_{MWOUT}	9	V
MWOUT Output Current	I_{MWOUT}	50	mA
V_{IN} Input Voltage	V_{IN}	9	V
V_{DET} Output Voltage	V_{DET}	9	V
V_{DET} Output Current	I_{DET}	50	mA
CD Input Voltage	V_{CD}	-0.3 ~ V_{IN1} + 0.3	V
Continuous Total Power Dissipation	Pd	350	mW
Operating Ambient Temperature	Topr	-30 ~ +80	°C
Storage Temperature	Tstg	-40 ~ +125	°C

■Electrical Characteristics (XC651A4AA3VR)

(note that the above is a sample part number and that actual part numbers will differ)

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Set-Up Voltage

Ta=25°C

BLOCK	PARAMETER	SYMBOL	SET-UP VOLTAGE VALUE	UNITS
1. PFM DC/DC	Output Voltage	V_{OUT}	2.500	V
2. MWVD	$MWOUT1$ detect voltage	V_{DFMW1}	1.275	V
	$MWOUT2$ detect voltage	V_{DFMW2}	1.245	V
	$MWOUT3$ detect voltage	V_{DFMW3}	1.210	V
	$MWOUT4$ detect voltage	V_{DFMW4}	1.060	V
3. VD1	Detect Voltage 1	V_{DF1}	1.500	V
4.VD2	Detect Voltage 2	V_{DF2}	0.950	V

1. PFM DC/DC

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Output Voltage	V_{OUT}	Ext. components connected	2.438	2.500	2.563	V	1
Operating Voltage	V_{IN}		-	-	6.0	V	-
Operating Start-Up Voltage	V_{ST}	Ext. components connected, I_{OUT}=1mA	-	0.8	0.9	V	1
Operating Hold Voltage	V_{HLD}	Ext. components connected, I_{OUT}=1mA	0.7	-	-	V	1
Supply Current 1	I_{DD1}	Output Voltage x 0.95 applied to V_{OUT}	-	35.0	56.9	μA	2
Supply Current 2	I_{DD2}	Output Voltage + 0.5V applied to V_{OUT}	-	2.5	5.0	μA	2
Lx Switch ON Resistance	R_{SWON}	Output Voltage x 0.95 applied to V_{OUT},V_{LX}=0.4V	-	9.1	13.7	Ω	2
Lx Leak Current	I_{LXL}	No ext. components, V_{OUT}=V_{LX}=10V	-	-	1.0	μA	3
Lx Control Voltage	V_{LXLMT}	Output Voltage x 0.95 applied to V_{OUT}, Output Voltage applied to Lx, When the oscillator frequency is more than double	0.7	-	1.1	V	2
EXT H ON Resistance	R_{EXTH}	Output Voltage x 0.95 applied to V_{OUT}, V_{EXT}=V_{OUT} - 0.4V	-	140	210	Ω	2
EXT L ON Resistance	R_{EXTL}	Output Voltage x 0.95 applied to V_{OUT}, V_{EXT}=0.4V	-	140	210	Ω	2
Duty Ratio 1	DTY1	Output Voltage x 0.95 applied to V_{OUT}, EXT waveform measurement	70	75	80	%	2
Duty Ratio 2	DTY2	Ext. components connected, I_{OUT}=1mA, LX ON time measurement	-	62	-	%	1
Max Oscillator Frequency	$MAXF_{OSC}$	Output Voltage x 0.95 applied to V_{OUT}, EXT waveform measurement	85	100	115	kHz	2
Stand-by Current	I_{STB}	Output Voltage x 0.95 applied to V_{OUT}, V_{EN}=0V	-	0.2	1.0	μA	2
EN H Voltage	V_{ENH}	Output Voltage x 0.95 applied to V_{OUT}, EXT oscillation judgement	0.7	-	-	V	4
EN L Voltage	V_{ENL}	Output Voltage x 0.95 applied to V_{OUT}, EXT stopped judgement	-	-	0.2	V	4
EN H Current	I_{ENH}	Output Voltage x 0.95 applied to V_{OUT}, V_{EN}=V_{OUT}	-	-	0.25	μA	4
EN L Current	I_{ENL}	Output Voltage x 0.95 applied to V_{OUT}, V_{EN}=0V	-	-	- 0.25	μA	4
Efficiency (note 1)	EFFI	Ext. components connected	-	70	-	%	1

Conditions : Unless indicated, connect EN to V_{OUT}, V_{IN}=Output Voltage x 0.6, I_{OUT}=10mA

Note : 1. EFFI={ [(output voltage) x (output current)] / [(input voltage) x (input current)] } x 100

2. MWVD (Positive Logic)

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
MW OUT1 Detect Voltage	V_{DFMW1}		1.250	1.275	1.301	V	5
MW OUT2 Detect Voltage	V_{DFMW2}		1.220	1.245	1.270	V	5
MW OUT3 Detect Voltage	V_{DFMW3}		1.186	1.210	1.234	V	5
MW OUT4 Detect Voltage	V_{DFMW4}		1.039	1.060	1.081	V	5
MW OUT1 Hysteresis Width	V_{HYSMW1}	(Release Voltage=V_{DFMW1} + V_{HYSMW1})	4	10	-	mV	5
MW OUT2 Hysteresis Width	V_{HYSMW2}	(Release Voltage=V_{DFMW2} + V_{HYSMW2})	4	10	-	mV	5
MW OUT3 Hysteresis Width	V_{HYSMW3}	(Release Voltage=V_{DFMW3} + V_{HYSMW3})	4	10	-	mV	5
MW OUT4 Hysteresis Width	V_{HYSMW4}	(Release Voltage=V_{DFMW4} x (1 + V_{HYSMW4} / 100))	2	-	8	%	5
Supply Current	I_{SSMW}	MWVD$_{IN}$=2.0V	-	5.0	20.0	μA	6
Operating Voltage	MWVD$_{IN}$		0.9	-	6.0	V	-
MW OUT1 Output Current	I_{OUTMW1}	Nch V_{DS}=0.5V, MWVD$_{IN}$=0.9V	0.18	1.8	-	mA	7
MW OUT2 Output Current	I_{OUTMW2}	Nch V_{DS}=0.5V, MWVD$_{IN}$=0.9V	0.18	1.8	-	mA	7
MW OUT3 Output Current	I_{OUTMW3}	Nch V_{DS}=0.5V, MWVD$_{IN}$=0.9V	0.18	1.8	-	mA	7
MW OUT4 Output Current	I_{OUTMW4}	Nch V_{DS}=0.5V, MWVD$_{IN}$=0.9V	0.18	1.8	-	mA	7
MW OUT1 Delay Time	T_{DLYMW1}	Release Voltage ⟶ Output Inversion, RIP open	-	-	0.4	msec	8
MW OUT2 Delay Time	T_{DLYMW2}	Release Voltage ⟶ Output Inversion, RIP open	-	-	0.4	msec	8
MW OUT3 Delay Time	T_{DLYMW3}	Release Voltage ⟶ Output Inversion, RIP open	-	-	0.4	msec	8
MW OUT4 Delay Time	T_{DLYMW4}	Release Voltage ⟶ Output Inversion, RIP open	-	-	0.4	msec	8
Ripple Rejection Resistance	R_{RIP}	RIP=1V, MWVD$_{IN}$=0V	250	500	1000	kΩ	9

Special Parameter : $V_{DFMW1} \geq V_{DFMW2} \geq V_{DFMW3}$

3. VD 1

V_{DF1}=1.5V Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage VD1	V_{DF1}		1.470	1.500	1.530	V	5
Hysteresis Width VD1	V_{HYS1}	(Release Voltage=V_{DF1} x (1 + V_{HYS1} / 100))	2	-	8	%	5
Supply Current	I_{SS1}	V_{IN1}=2.0V	-	1.5	3.0	μA	6
Operating Voltage	V_{IN1}		0.7	-	6.0	V	-
Output Current V_{DET1}	I_{OUT1}	N-ch VDS=0.5V, V_{IN1}=0.9V	0.22	2.2	-	mA	7
V_{DET1} L ⟶ H Delay Time	T_{LH1}	CD=3.3μF, V_{IN1}=V_{DF1} x 0.9 ⟶ V_{DF1} x 1.1	500	1000	2000	msec	8
V_{DET1} H ⟶ L Delay Time	T_{HL1}	CD=3.3μF, V_{IN1}=V_{DF1} x 1.1 ⟶ V_{DF1} x 0.9	20	50	100	msec	8

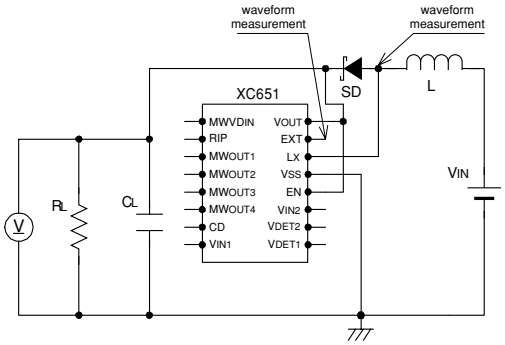
4. VD 2

V_{DF2}=0.95V Ta=25°C

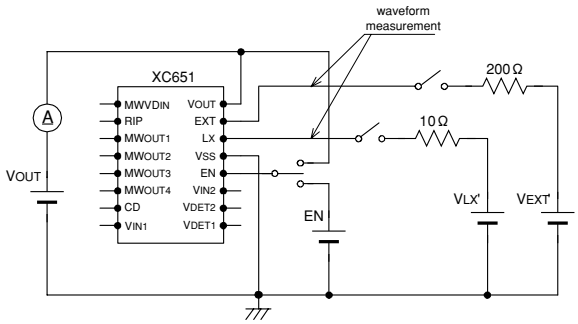
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage VD2	V_{DF2}		0.931	0.950	0.969	V	5
Hysteresis Width VD2	V_{HYS2}	(Release Voltage=V_{DF2} x (1 + V_{HYS2}/ 100))	2	-	8	%	5
Supply Current	I_{SS2}	V_{IN2}=2.0V	-	1.5	3.0	μA	6
Operating Voltage	V_{IN2}		0.7	-	6.0	V	-
Output Current V_{DET2}	I_{OUT2}	N-ch V_{DS}=0.5V, V_{IN2}=0.9V	0.18	1.8	-	mA	7
Delay Time V_{DET2}	T_{DLY2}	Release Voltage ⟶ Output Inversion	-	-	0.2	msec	8

■Test Circuits

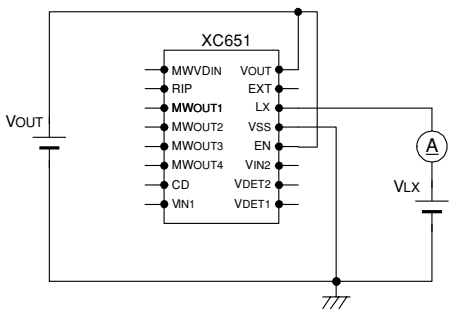
Measurement Circuit 1



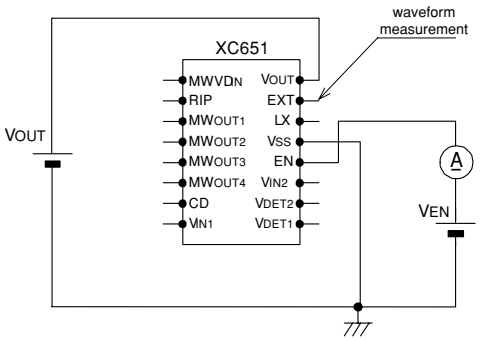
Measurement Circuit 2



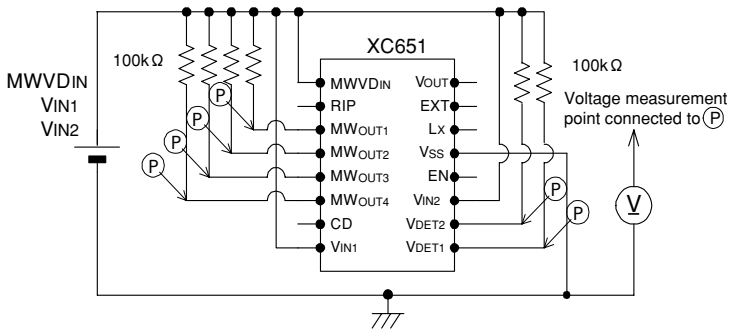
Measurement Circuit 3



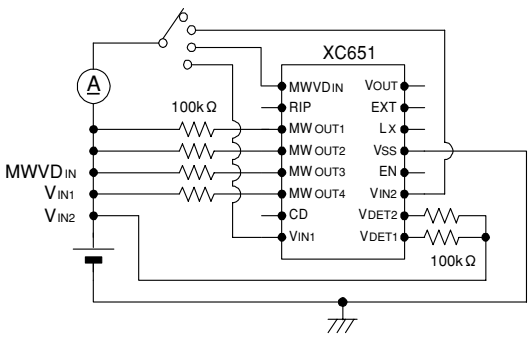
Measurement Circuit 4



Measurement Circuit 5



Measurement Circuit 6



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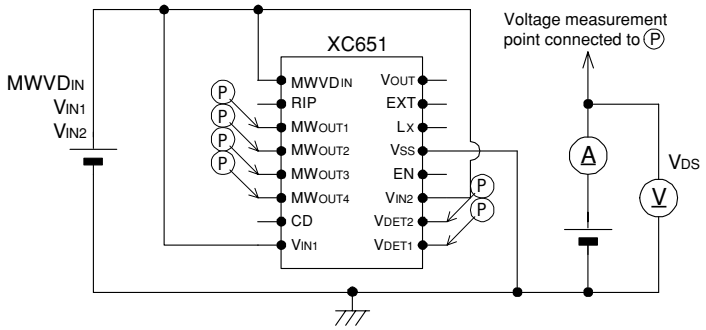
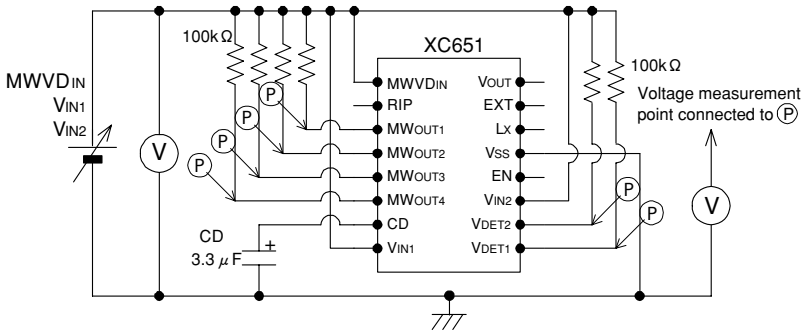
Measurement Circuit 7



Measurement Circuit 8



Measurement Circuit 9