# TJ1004

PRELIMINARY SPECIFICATION

## General Description

TChip's TJ1004 is a single chip RF front-end for Global Positioning System (GPS) receivers. The TJ1004 uses innovative design techniques and a leading-edge BiCMOS process to offer a complete GPS front-end solution with minimum external parts count, lowest power consumption, small size and high reliability.

The TJ1004 is a superhet receiver. The 1575.42MHz L1 GPS signal is down-converted and filtered by an LC filter, then sampled with a 2-bit A/D converter for subsequent digital processing. The A/D converter also performs conversion to the 2nd, final IF. A crystal oscillator and a PLL generate all required clock signals. Two different reference frequencies are supported. A frequency of 16.368MHz results in a 2nd IF of 4.092MHz, which is compatible with many existing baseband processors. A frequency of 13.000MHz can be used to simplify integration of GPS into cellular (GSM) handsets.

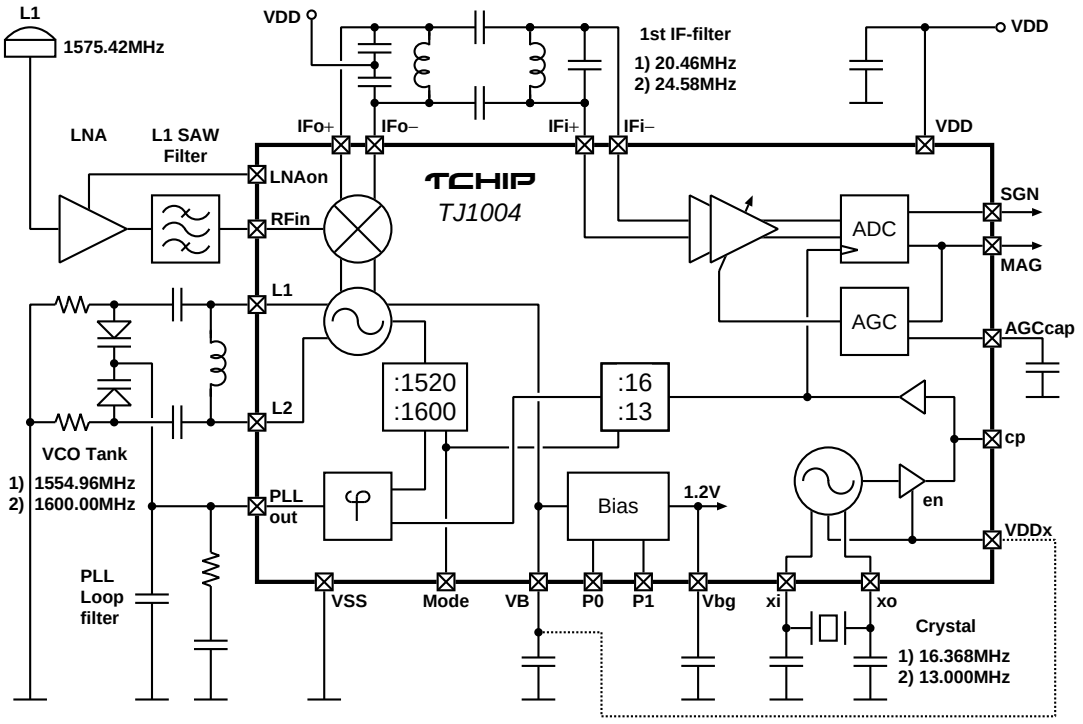
The TJ1004 may be operated from an unregulated 2.2 to 3.6V power supply over the $-40$ to $+85^{\circ}$C temperature range, consuming only 5.2mA in the fully active state. Three low-latency power-down modes are provided to aid in implementing various additional power-saving schemes under control of the CPU. These features make the TJ1004 an ideal core building block for integration into portable, battery-operated equipment and applications where high reliability and low power consumption are of paramount importance.

## Features

- Double-conversion receiver for GPS C/A code
- Unregulated supply voltage – 2.2 to 3.6V
- Ultra low power, fast power-down modes
  - Fully active – 5.2mA typ.
  - Standby – 3.5mA
  - Doze – 300$\mu$A
  - Sleep – 10nA
- On-chip reference crystal oscillator
- Supports 16.368MHz and 13.000MHz clocks
- 2-bit sign and magnitude digital output
- Low off-chip parts count
- Compatible with existing baseband solutions
- 28-Lead miniature package

## Applications

- Location-aware cellular phones
- Wristwatches, time references
- PDAs, handheld navigation systems
- Covert GPS receivers
- Asset tracking
- Distributed continuous surveying receivers
- Power-sensitive, battery operated GPS receivers



## Absolute Maximum Ratings

Max. Supply Voltage ..... 7V
Max. RF Input .....+10dBm
Max. current into any pin ..... ±20mA
Continuous Power Dissipation.....600mW

Operating Temperature.....–40 to +85°C
Junction Temperature ..... 125°C
Storage Temperature ..... –65 to +150°C
Lead Temperature (Soldering, 10s) ..... 260°C

*Absolute maximum ratings are short term stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.*

**ESD sensitive device:** use proper precautions when handling this device.

## Electrical Characteristics

$V_{DD}$ = 2.2 to 3.6V, $T_{amb}$ = −40 to +85°C, no load, crystal oscillator active, unless otherwise noted. All voltages are referred to $V_{SS}$. Typical values are at $V_{DD}$ = 2.5V, $T_{amb}$ = +25°C. All values given here are estimations as the data sheet contains advance information.

| Parameter | Conditions | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **RF Mixer** | | | | | | |
| Conversion gain | | 8.9 | 9.5 | 10.4 | dB | 1 |
| SSB noise figure | differential output | | 12 | 14 | dB | |
| 1dB compression point | input referred | | −17 | | dBm | |
| input VSWR | at 1.57GHz | | 1.1:1 | 1.4:1 | | |
| Diff. output impedance | | 950 | 1200 | 1450 | Ω | 2 |
| **IF Strip** | | | | | | |
| Voltage gain | | 70 | 80 | | dB | |
| Gain control range | | 50 | 60 | | dB | |
| Diff. input impedance | | 3800 | 4800 | 5800 | Ω | 2 |
| Input DC level | | | $V_{bg}$ | | V | |
| AGC sensitivity | pin 26 | 5.4 | 6.8 | 8.0 | mV/dB | 3, 4 |
| AGC volt. at max. gain | pin 26 | 0.72 | 0.85 | 1.0 | V | 3 |
| AGC output current | pin 26, at 25°C | 12 | 16 | 20 | µA | 3, 4 |
| AGC hold leakage curr. | pin 26, at 85°C | | | 10 | nA | |
| ADC sensitivity | full scale (MAG=1) | 65 | 90 | 115 | mV | 5 |
| ADC SGN duty cycle | | | 50 | | % | |
| ADC MAG duty cycle | | | 33 | | % | |
| **Local Oscillator, PLL** | | | | | | |
| VCO gain | recommended tank | | 160 | | MHz/V | |
| Phase noise | 100kHz offset | | −100 | | dBc/Hz | 6 |
| PLL spurs | | | (−50) | TBD | dBc | |
| PFC gain | pin 9 | | 1.6 | | µA/rad | |
| PFC output current | peak, pin 9 | 7.4 | 10 | 13.8 | µA | |
| PFC voltage swing | pin 9 | 3.4 | 3.7 | 4.0 | V | |
| PFC leakage current | pin 9, at +85°C | | | 10 | nA | |
| Lock time | | | TBD | | µs | 7 |

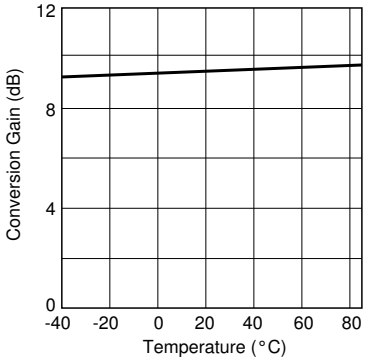
## Electrical Characteristics - *Continued*

| Parameter | Conditions | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **Crystal Oscillator** | | | | | | |
| Crystal drive level | | | 10 | | $\mu$W | 8 |
| Oscillation amplitude | differential, across crystal | 1.0 | 1.25 | 1.6 | $V_{pp}$ | 8 |
| Supply voltage | pin 5 | 1.8 | 2 | 3.6 | V | |
| Start-up current | into VDDx (pin 5) | 320 | 540 | 880 | $\mu$A | |
| Operating current | into VDDx (pin 5) | | 100 | | $\mu$A | 8 |
| Clock duty cycle | pin 4, output | 40 | 50 | 60 | % | |
| **Voltage Regulator** | | | | | | |
| Bandgap ref. voltage | no load | 1.16 | 1.22 | 1.28 | V | |
| Bandgap ref. output curr. | | 200 | | | $\mu$A | 9 |
| Reg. output voltage | | 1.85 | 1.95 | 2.05 | V | |
| Line regulation | 2.2 to 3.6V | | 4 | | mV | |
| Reg. output current | | 500 | | | $\mu$A | 9 |
| **Digital Interfaces** | | | | | | |
| Input high level | | $0.8V_{DD}$ | | | V | |
| Input low level | | | | $0.2V_{DD}$ | V | |
| Output high level | $I_{OH}$=−1mA | $0.9V_{DD}$ | | | V | 10 |
| Output low level | $I_{OL}$=1mA | | | $0.1V_{DD}$ | V | 10 |
| Output rise time | $C_{load}$=15pF | | | 10 | ns | 11 |
| Output fall time | $C_{load}$=15pF | | | 10 | ns | 11 |
| LNAon dropout voltage | $I_{load}$=3mA | | 100 | 200 | mV | 12 |
| **Power Supply** | | | | | | |
| Supply voltage | | 2.2 | 2.5 | 3.6 | V | |
| Supply current | fully active | | 5.2 | 8.0 | mA | |
| | stand-by | | 3.5 | 5.8 | mA | |
| | doze, crystal oscillator on | | 300 | 500 | $\mu$A | 8 |
| | doze, crystal oscillator off | | 75 | 130 | $\mu$A | |
| | sleep | | 10 | 100 | nA | |

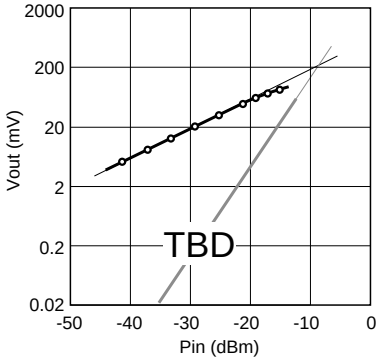
**Note 1:** Voltage conversion gain, differential, terminated on rated impedance.
**Note 2:** I/O impedances track to 5% or better.
**Note 3:** Internal AGC regulator may be overriden by applying a control voltage to pin 26 (50$\mu$A minimum source capability recommended).
**Note 4:** This value is proportional to absolute temperature (PTAT).
**Note 5:** Voltage at ADC input (IF-amp output), which switches MAG output to 1.
**Note 6:** Open PLL loop. Value depends on Q of external tank circuit.
**Note 7:** Recommended loop filter, worst case, loop filter capacitors discharged, from doze.
**Note 8:** Crystal oscillator is amplitude regulated. Actual crystal drive level and oscillator operating current depend on crystal type and Q.
**Note 9:** Minimum current available to an external load under worst-case conditions.
**Note 10:** All digital output pads, including LNAon.
**Note 11:** Measured between the 10% and 90% points.
**Note 12:** LNAon used as power supply for external LNA. $V_{DD}$ = 2.2V, worst case conditions.

## Typical Operating Characteristics

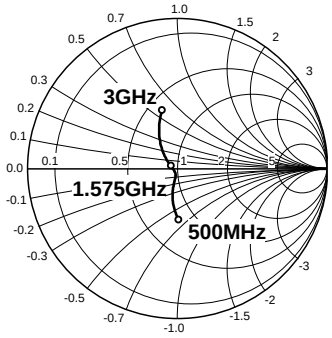
**RF Mixer Gain vs. Temp.**



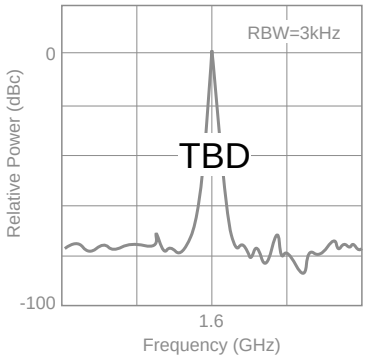

**RF Mixer Linearity**



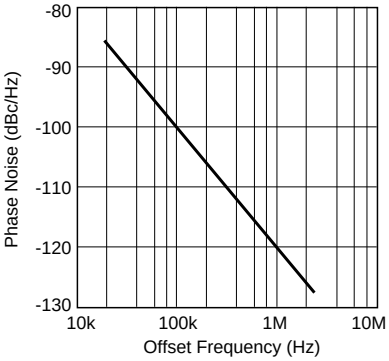

**$S_{11}$ vs. Frequency**



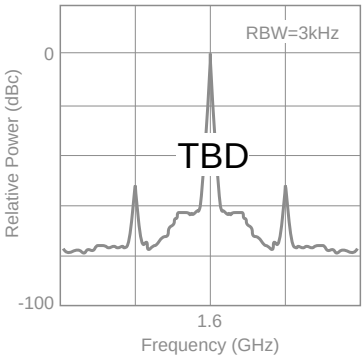

**Local Oscillator Spectrum**



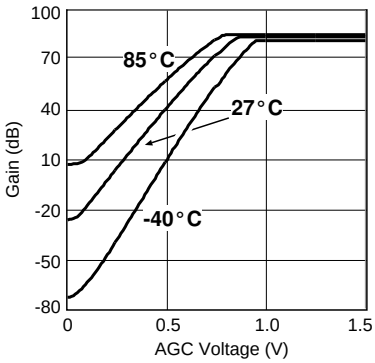

**LO Phase Noise vs. Offset**



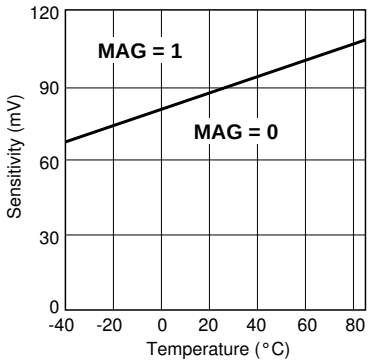

**PLL Spectrum**



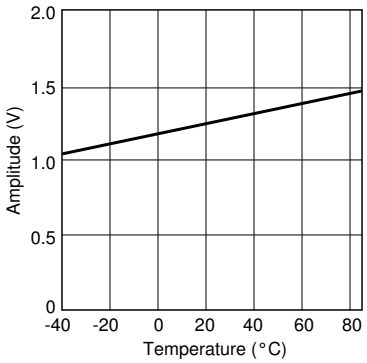

**IF-Amp Gain vs. AGC Voltage**



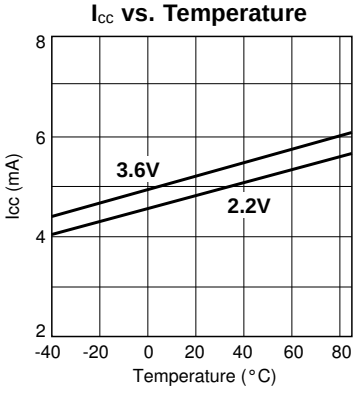

**ADC Sensitivity**



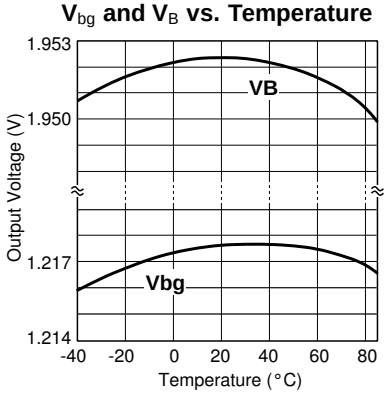

**XTAL Oscillator Amplitude**



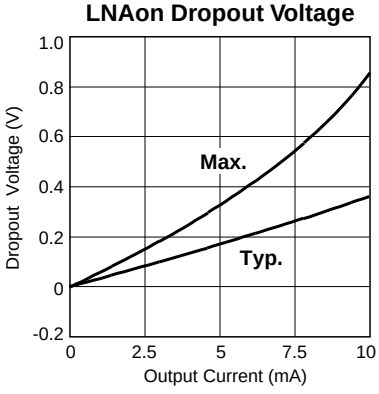

**$I_{cc}$ vs. Temperature**




**$V_{bg}$ and $V_B$ vs. Temperature**

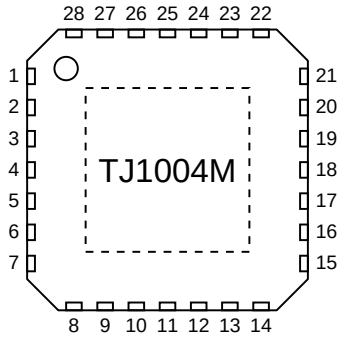



**LNAon Dropout Voltage**

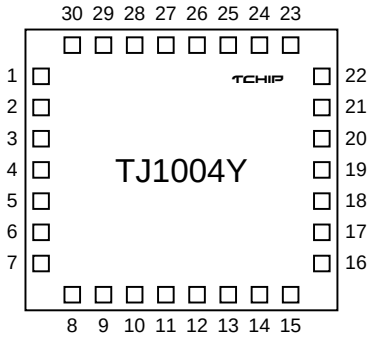


## Pin Configuration




**Micro Leadframe Package**




**Bare Die**

## Pin Description

| Name | MLF (M) | Die (Y) | Description |
|---|---|---|---|
| SGN | 1 | 1 | ADC sign bit data output. Synchronized to falling edge of CP. |
| MAG | 2 | 2 | ADC magnitude bit data output. Synchronized to falling edge of CP. |
| Mode | 3 | 3 | Selects 16.368MHz (low) or 13.000MHz (high) operating mode. |
| cp | 4 | 4 | Clock signal input/output. |
| VDDx | 5 | 5 | Supply voltage to the crystal oscillator. Normally connected to VB. |
| xi | 6 | 6 | Crystal oscillator input pin. |
| xo | 7 | 7 | Crystal oscillator output pin. |
| VSS | 8 | 8 | Negative power supply pin. |
| (test) | – | 9 | Test pin, output of the phase comparator voltage doubler (4V). Do not connect. |
| PLLout | 9 | 10 | Output of the PLL phase comparator. Connected to the loop filter. |
| VSS | 10 | 11 | Negative power supply pin. |
| L1 | 11 | 12 | Local oscillator tank connection (see applications information). |
| L2 | 12 | 13 | Local oscillator tank connection (see applications information). |
| VSS | 13 | 14 | Negative power supply pin. |
| VB | 14 | 15 | Output of the on-chip 2V voltage regulator. Decouple to VSS close to the chip. |
| LNAon | 15 | 16 | LNA enable output, active high. May supply power to a low power LNA. |
| Vbg | 16 | 17 | 1.2V bandgap reference output. |
| VDD | 17 | 18 | Positive power supply pin. Decouple to VSS close to the chip. |
| VSS | 18 | 19 | Negative power supply pin. |
| RFin | 19 | 20 | Input for the 1575.42MHz GPS L1 signal. Impedance: 50Ω nominal. |
| VSS | 20 | 21 | Negative power supply pin. |
| IFo– | 21 | 22 | IF output of the mixer. Connected to the external LC channel filter. |
| IFo+ | 22 | 23 | IF output of the mixer. Connected to the external LC channel filter. |
| VDD | 23 | 24 | Positive power supply pin. Decouple to VSS close to the chip. |
| VSS | PAD | 25 | Negative power supply pin. Must be connected/soldered to PCB. |
| IFi+ | 24 | 26 | IF amplifier input. Connected to the external LC filter. |
| IFi– | 25 | 27 | IF amplifier input. Connected to the external LC filter. |
| AGCcap | 26 | 28 | Connection to the AGC capacitor, sets the AGC time constant. |
| P1 | 27 | 29 | Power control pin #1. Selects power down modes. |
| P0 | 28 | 30 | Power control pin #2. Selects power down modes. |

## Circuit Description

The TJ1004 is a superheterodyne receiver front-end for the GPS L1 band characterized by a high degree of versatility. A typical receiver consists of an active antenna, the TJ1004, a RF and an IF filter, and a LC resonator for the local oscillator.

The signal path in the TJ1004 begins with the RF mixer, which converts the RF signal to the 1st IF. The mixer is single balanced, provides 9.5dB typ. gain and a 50Ω input impedance matching most existing filters for GPS use. The mixer output directly connects to the first IF filter, which is implemented as a 4th order balanced LC design and provides a limited amount of voltage gain.

The filtered signal is then amplified by an IF amplifier with AGC. The AGC control circuit incorporates a hold function, which keeps the voltage at the AGC capacitor - and thus the amplifier gain - constant during circuit power-off periods. Subsequently, an ADC converts the 1st IF signal to a 2-bit digital word while at the same time effecting down-conversion to the 2nd IF by sub-sampling the 1st IF signal. The ADC has a positive temperature coefficient and as such partly compensates for the negative TC of the IF amplifier. The 2-bit digital word (sign and magnitude) is suitable for direct interface to a baseband processor.

Local oscillator signals are generated by an internal fixed-frequency PLL. The local oscillator is a balanced VCO with external tank. Its output is divided with an ECL divider and supplied to a phase-frequency comparator. This block includes a hold function to maintain the VCO control voltage at approximately the correct value during a power-down phase, for faster restart of the VCO and minimum lock time when power is restored.

The reference frequency is provided by an amplitude regulated crystal oscillator. The generated clock signal corresponds to the sample clock of the A/D converter. An on-chip regulator supplies 2V to the VCO, and to the VB pin. By connecting the VDDx pin to VB, the crystal oscillator is enabled and the reference clock signal is available on pin CP where it may be used to drive the baseband processor, the controlling microprocessor and other functional blocks where desired. A low logic level on VDDx disables the crystal oscillator, and an externally generated reference clock may be applied to CP.

Two power control pins select one of three operating modes. The LNAon output is designed to source sufficient current to provide the power supply to an external LNA. Alternatively, LNAon may be used as an active high LNA enable signal.

## Frequency Plans

The TJ1004 supports two distinct reference frequencies, leading to different frequency plans. The first reference frequency, 16.368MHz, is directly compatible with many existing baseband circuits and is therefore an ideal choice in applications where the TJ1004 substitutes a previous generation front-end circuit. The second reference frequency, 13.000MHz, uses a low cost TCXO as found in GSM, thus simplifying integration of GPS functionality into cellular phones. Selection of a reference frequency is effected by the logic level at the MODE input. In most applications the MODE pin will be hard-wired to VDD or VSS since the choice of reference frequency is a system issue which dictates different IF frequencies, external component values and possibly affects settings in the baseband circuit or processor firmware. The two frequency plans are shown in Table 1.

| Reference Frequency | Mode | 1st IF Frequency | 2nd IF Frequency | LO Frequency | Image Frequency |
|---|---|---|---|---|---|
| 16.368MHz | 0 | 20.46MHz | 4.092MHz | 1554.96MHz | 1534.50MHz |
| 13.000MHz | 1 | 24.58MHz | 1.420MHz | 1600.00MHz | 1624.58MHz |

Table 1: Supported frequency plans.

## Ordering Information

| Part | Temperature Range | Package |
|---|---|---|
| TJ1004M | –40 to 85°C | MLF |
| TJ1004Y | –40 to 85°C | Die |

## Related Products

| Part | Description |
|---|---|
| TJ1001 | 1.2–2GHz Low Power LNA |