Intel® IXB8055 UTOPIA/POS Reference Design to IXF6012/ IXF6048

Hardware Implementation Appplication Note

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Revision History

Date	Revision	Description
3/19/01	001	First release.
4/13/01	002	Update trademark and copyright usage. No technical changes.

Contents

Tables

1.0 Introduction

This application note describes how to use the Intel® IXB8055 UTOPIA/POS Reference Design with the IXF6012/IXF6048. Although the reference design was specifically designed to support the IXF6012/IXF6048, it does not support every possible mode that the IXF6012/IXF6048 is capable of. The reference design also implements some features that are not supported in the IXF6012/IXF6048. This section explains what is supported and what is not supported.

For more information, refer to the *IXF6012 Datasheet* available on the Intel developer.com website at:

http://developer.intel.com/design/network/products/optical/framers/ixf6048.htm

2.0 Interconnection

Table 1 describes how to interface the Intel® IXB8055 UTOPIA/POS Reference Design to the IXF6012/IXF6048. Because the reference design was designed specifically to connect to the IXF6012/IXF6048, and uses the same signal names, connecting the two devices is relatively straightforward.

Table 1. Interconnect Table (Sheet 1 of 5)

Intel® IXB8055 UTOPIA/POS Reference Design Pin Name	Intel® IXB8055 UTOPIA/POS Reference Design Pin Number	IXF6012/IXF6048 Pin Name	IXF6012/IXF6048 Pin Number	Notes
—	—	RXADDR[4]	A21	Connect to logic 1 on the IXF6012/IXF6048
—	—	RXADDR[3]	B20	Connect to logic 1 on the IXF6012/IXF6048
RXADDR[2]	AA4	RXADDR[2]	C19	—
RXADDR[1]	AB4	RXADDR[1]	B19	—
RXADDR[0]	AB5	RXADDR[0]	C18	—
RXDATA[31]	M5	RXDATA[31]	F23	RXDATA_3[7]
RXDATA[30]	M6	RXDATA[30]	B27	RXDATA_3[6]
RXDATA[29]	N1	RXDATA[29]	D25	RXDATA_3[5]
RXDATA[28]	N3	RXDATA[28]	C26	RXDATA_3[4]
RXDATA[27]	N4	RXDATA[27]	E23	RXDATA_3[3]
RXDATA[26]	N5	RXDATA[26]	B26	RXDATA_3[2]
RXDATA[25]	P1	RXDATA[25]	C25	RXDATA_3[1]
RXDATA[24]	P2	RXDATA[24]	A27	RXDATA_3[0]
RXDATA[23]	P3	RXDATA[23]	D22	RXDATA_2[7]
RXDATA[22]	P4	RXDATA[22]	C23	RXDATA_2[6]
RXDATA[21]	P5	RXDATA[21]	D21	RXDATA_2[5]

Table 1. Interconnect Table (Sheet 2 of 5)

Intel® IXB8055 UTOPIA/POS Reference Design Pin Name	Intel® IXB8055 UTOPIA/POS Reference Design Pin Number	IXF6012/ IXF6048 Pin Name	IXF6012/ IXF6048 Pin Number	Notes
RXDATA[20]	R1	RXDATA[20]	E21	RXDATA_2[4]
RXDATA[19]	R2	RXDATA[19]	C22	RXDATA_2[3]
RXDATA[18]	R3	RXDATA[18]	B24	RXDATA_2[2]
RXDATA[17]	R5	RXDATA[17]	B23	RXDATA_2[1]
RXDATA[16]	T1	RXDATA[16]	F20	RXDATA_2[0]
RXDATA[15]	T2	RXDATA[15]	A20	RXDATA_1[7]
RXDATA[14]	T4	RXDATA[14]	F16	RXDATA_1[6]
RXDATA[13]	T5	RXDATA[13]	A19	RXDATA_1[5]
RXDATA[12]	U1	RXDATA[12]	A18	RXDATA_1[4]
RXDATA[11]	U2	RXDATA[11]	D17	RXDATA_1[3]
RXDATA[10]	U3	RXDATA[10]	B17	RXDATA_1[2]
RXDATA[9]	U4	RXDATA[9]	B18	RXDATA_1[1]
RXDATA[8]	V1	RXDATA[8]	D16	RXDATA_1[0]
RXDATA[7]	V2	RXDATA[7]	B14	RXDATA_0[7]
RXDATA[6]	V3	RXDATA[6]	F14	RXDATA_0[6]
RXDATA[5]	V4	RXDATA[5]	D14	RXDATA_0[5]
RXDATA[4]	W1	RXDATA[4]	A13	RXDATA_0[4]
RXDATA[3]	W2	RXDATA[3]	A14	RXDATA_0[3]
RXDATA[2]	W3	RXDATA[2]	A12	RXDATA_0[2]
RXDATA[1]	Y22	RXDATA[1]	B13	RXDATA_0[1]
RXDATA[0]	AA1	RXDATA[0]	D13	RXDATA_0[0]
RXPFA	W5	RXPFA	B9	—
—	—	RXPADL[2]	E12	Leave unconnected
RXPADL[1]	AA6	RXPADL[1]	F12	—
RXPADL[0]	AB6	RXPADL[0]	B10	—
RXCLK_0	AB13	—	—	Do not use
UCLK01	W12	RXCLK_0	E17	Connect to same clock source
RXENB_0	W6	RXENB_0	E19	—
RXSOF_0	AB7	RXSOF_0	B11	—
RXEOF_0	AA7	RXEOF_0	C12	—
RXPRTY_0	Y7	RXPRTY_0	D12	—
RXERR_0	W7	RXERR_0	E13	—
RXFA_0	V7	RXFA_0	B12	—
RXVAL_0	AB8	RXVAL_0	F13	—

Table 1. Interconnect Table (Sheet 3 of 5)

Intel® IXB8055 UTOPIA/POS Reference Design Pin Name	Intel® IXB8055 UTOPIA/ POS Reference Design Pin Number	IXF6012/ IXF6048 Pin Name	IXF6012/ IXF6048 Pin Number	Notes
RXCLK_1	AB12	—	—	Do not use
UCLK01	W12	RXCLK_1	F17	Connect to same clock source
RXENB_1	AA8	RXENB_1	D19	—
RXSOF_1	Y8	RXSOF_1	C14	Do not connect
RXEOF_1	V8	RXEOF_1	D15	—
RXPRTY_1	AB9	RXPRTY_1	C15	—
RXERR_1	AA9	RXERR_1	C16	—
RXFA_1	Y9	RXFA_1	A17	—
RXVAL_1	W9	RXVAL_1	E15	—
RXCLK_2	AA12	—	—	Do not use
UCLK23	C11	RXCLK_2	E18	Connect to same clock source
RXENB_2	V9	RXENB_2	F19	—
RXSOF_2	AB10	RXSOF_2	A22	—
RXEOF_2	AA10	RXEOF_2	B21	—
RXPRTY_2	W10	RXPRTY_2	B22	—
RXERR_2	V10	RXERR_2	C21	—
RXFA_2	AB11	RXFA_2	E20	—
RXVAL_2	W11	RXVAL_2	A23	—
RXCLK_3	Y12	—	—	Do not use
UCLK23	C11	RXCLK_3	F18	Connect to same clock source
RXENB_3	V11	RXENB_3	C20	—
RXSOF_3	Y10	RXSOF_3	B25	—
RXEOF_3	V12	RXEOF_3	A25	—
RXPRTY_3	V13	RXPRTY_3	D23	—
RXERR_3	U12	RXERR_3	C24	—
RXFA_3	W13	RXFA_3	A26	—
RXVAL_3	Y13	RXVAL_3	D24	—
—	—	TXADDR[4]	D11	Connect to logic 1 on the IXF6012/ IXF6048
—	—	TXADDR[3]	A9	Connect to logic 1 on the IXF6012/ IXF6048
TXADDR[2]	A3	TXADDR[2]	D10	—
TXADDR[1]	A4	TXADDR[1]	C9	—
TXADDR[0]	A5	TXADDR[0]	A8	—
TXDATA[31]	B1	TXDATA[31]	B4	TXDATA_3[7]

Table 1. Interconnect Table (Sheet 4 of 5)

Intel® IXB8055 UTOPIA/POS Reference Design Pin Name	Intel® IXB8055 UTOPIA/POS Reference Design Pin Number	IXF6012/IXF6048 Pin Name	IXF6012/IXF6048 Pin Number	Notes
TXDATA[30]	C1	TXDATA[30]	F8	TXDATA_3[6]
TXDATA[29]	C2	TXDATA[29]	F7	TXDATA_3[5]
TXDATA[28]	D1	TXDATA[28]	D7	TXDATA_3[4]
TXDATA[27]	E1	TXDATA[27]	A3	TXDATA_3[3]
TXDATA[26]	E3	TXDATA[26]	A4	TXDATA_3[2]
TXDATA[25]	E4	TXDATA[25]	B3	TXDATA_3[1]
TXDATA[24]	F1	TXDATA[24]	E7	TXDATA_3[0]
TXDATA[23]	F2	TXDATA[23]	E5	TXDATA_2[7]
TXDATA[22]	F3	TXDATA[22]	C1	TXDATA_2[6]
TXDATA[21]	F4	TXDATA[21]	G6	TXDATA_2[5]
TXDATA[20]	F5	TXDATA[20]	D4	TXDATA_2[4]
TXDATA[19]	G1	TXDATA[19]	E4	TXDATA_2[3]
TXDATA[18]	G2	TXDATA[18]	F5	TXDATA_2[2]
TXDATA[17]	G3	TXDATA[17]	D2	TXDATA_2[1]
TXDATA[16]	G4	TXDATA[16]	D3	TXDATA_2[0]
TXDATA[15]	G5	TXDATA[15]	E2	TXDATA_1[7]
TXDATA[14]	H1	TXDATA[14]	F4	TXDATA_1[6]
TXDATA[13]	H2	TXDATA[13]	G4	TXDATA_1[5]
TXDATA[12]	H3	TXDATA[12]	E1	TXDATA_1[4]
TXDATA[11]	H5	TXDATA[11]	J6	TXDATA_1[3]
TXDATA[10]	J1	TXDATA[10]	F3	TXDATA_1[2]
TXDATA[9]	J2	TXDATA[9]	H5	TXDATA_1[1]
TXDATA[8]	J3	TXDATA[8]	G3	TXDATA_1[0]
TXDATA[7]	J4	TXDATA[7]	K6	TXDATA_0[7]
TXDATA[6]	J5	TXDATA[6]	H2	TXDATA_0[6]
TXDATA[5]	K1	TXDATA[5]	J4	TXDATA_0[5]
TXDATA[4]	K2	TXDATA[4]	L6	TXDATA_0[4]
TXDATA[3]	K4	TXDATA[3]	G1	TXDATA_0[3]
TXDATA[2]	K5	TXDATA[2]	L5	TXDATA_0[2]
TXDATA[1]	L1	TXDATA[1]	J3	TXDATA_0[1]
TXDATA[0]	L2	TXDATA[0]	K3	TXDATA_0[0]
TXSFA	B5	TXSFA	C5	—
TXPFA	C5	TXPFA	B6	—
—	—	TXPADL[2]	C8	Tie to logic 1 on the IXF6012/IXF6048

Table 1. Interconnect Table (Sheet 5 of 5)

Intel® IXB8055 UTOPIA/POS Reference Design Pin Name	Intel® IXB8055 UTOPIA/ POS Reference Design Pin Number	IXF6012/ IXF6048 Pin Name	IXF6012/ IXF6048 Pin Number	Notes
TXPADL[1]	A6	TXPADL[1]	C7	—
TXPADL[0]	B6	TXPADL[0]	A7	—
TXCLK_0	C10	—	—	Do not use
UCLK01	W12	TXCLK_0	F10	Connect to same clock source
TXENB_0	D5	TXENB_0	D9	—
TXSOF_0	D6	TXSOF_0	M6	—
TXEOF_0	E6	TXEOF_0	H1	—
TXPRTY_0	A7	TXPRTY_0	J2	—
TXERR_0	B7	TXERR_0	K4	—
TXFA_0	C7	TXFA_0	D8	—
TXCLK_1	B10	—	—	Do not use
UCLK01	W12	TXCLK_1	E10	Connect to same clock source
TXENB_1	D7	TXENB_1	F9	—
TXSOF_1	E7	TXSOF_1	K5	—
TXEOF_1	A8	TXEOF_1	G2	—
TXPRTY_1	B8	TXPRTY_1	H4	—
TXERR_1	C8	TXERR_1	J5	—
TXFA_1	D8	TXFA_1	A5	—
TXCLK_2	C9	—	—	Do not use
UCLK23	C11	TXCLK_2	F11	Connect to same clock source
TXENB_2	D9	TXENB_2	B8	—
TXSOF_2	E9	TXSOF_2	H6	—
TXEOF_2	E10	TXEOF_2	G5	—
TXPRTY_2	D10	TXPRTY_2	D1	—
TXERR_2	F11	TXERR_2	E3	—
TXFA_2	B12	TXFA_2	A6	—
TXCLK_3	B9	—	—	Do not use
UCLK23	C11	TXCLK_3	E11	Connect to same clock source
TXENB_3	C12	TXENB_3	E9	—
TXSOF_3	D12	TXSOF_3	C2	—
TXEOF_3	E12	TXEOF_3	F6	—
TXPRTY_3	F12	TXPRTY_3	E6	—
TXERR_3	C13	TXERR_3	C4	—
TXFA_3	D13	TXFA_3	E8	—

3.0 Register Values

This section describes what register values should be programmed in the IXF6012/IXF6048 to work with the reference design in the different modes.

Note: Only the register fields that apply to the UTOPIA interface are discussed here. There are many other fields not described here which must be programmed with the proper values.

3.1 UTOPIA Bus Modes

Table 2 is derived from the *IXF6012 Datasheet* (the Line Side Interface column has been omitted). For more information, refer to the *IXF6012 Datasheet* available on the Intel developer.com website at:

http://developer.intel.com/design/network/products/optical/framers/ixf6048.htm

Table 2. IXF6012/IXF6048 UTOPIA Interface Operating Modes (Sheet 1 of 4)

Operating Mode	ATM/POS UTOPIA Interface	UMODE[1:0]/MPHY_MODE Strapping	IXF6012/IXF6048 Register Values
Single STS-48c/ STM-16c	1x32	1x32 mode, DSI	GOCNF[QMode] = 0 GOCNF[CMode] = 1 R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 10 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 10
	1x64	Not supported.	
Single STS-48/ STM-16	1x32	x32 mode, MPHY	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 10 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 10
	1x64	Not supported.	
	4x8	4x8 mode, DSI	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 1 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 1 T_UICNF[XmtUWidth] = 00
	4x16	Not supported.	—

Table 2. IXF6012/IXF6048 UTOPIA Interface Operating Modes (Sheet 2 of 4)

Operating Mode	ATM/POS UTOPIA Interface	UMODE[1:0]/MPHY_MODE Strapping	IXF6012/IXF6048 Register Values
Single STS-12/ STM-4	1x16	x16 mode, MPHY	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 01 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 01
	1x8	x8 mode, MPHY	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 00
	4x8	4x8 mode, DSI	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 1 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 1 T_UICNF[XmtUWidth] = 00
Single STS-3	1x8	x8 mode, MPHY; one FIFO is unused; if any cells are sent to the unused FIFO they are lost.	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 00
	1x16	x16 mode, MPHY	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 01 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 01
	3x8	4x8 mode, DSI; one port and FIFO is left unconnected and unused; if any cells are sent to the unused FIFO they are lost.	GOCNF[QMode] = 0 GOCNF[CMode] = 0 R_UICNF[RcvUQuad] = 1 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 1 T_UICNF[XmtUWidth] = 00

Table 2. IXF6012/IXF6048 UTOPIA Interface Operating Modes (Sheet 3 of 4)

Operating Mode	ATM/POS UTOPIA Interface	UMODE[1:0]/MPHY_MODE Strapping	IXF6012/IXF6048 Register Values
Quad STS-12c/ STM-4c	1x32	x32 mode, MPHY	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 10 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 10
	1x64	Not supported.	
	4x8	4x8 mmode, DSI	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 1 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 1 T_UICNF[XmtUWidth] = 00
	4x16	Not supported.	—
Quad STS-3c/ STM-1c	1x16	x16 mode, MPHY	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 01 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 01
	4x8	4x8 mode DSI	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 1 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 1 T_UICNF[XmtUWidth] = 00

Table 2. IXF6012/IXF6048 UTOPIA Interface Operating Modes (Sheet 4 of 4)

Operating Mode	ATM/POS UTOPIA Interface	UMODE[1:0]/MPHY_MODE Strapping	IXF6012/IXF6048 Register Values
Quad STS-1	1x8	x8 mode, MPHY	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 00
	1x16	x16 mode, MPHY	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 0 R_UICNF[RcvUWidth] = 01 T_UICNF[XmtUQuad] = 0 T_UICNF[XmtUWidth] = 01
	4x8	4x8 mode, DSI	GOCNF[QMode] = 1 GOCNF[CMode] = x R_UICNF[RcvUQuad] = 1 R_UICNF[RcvUWidth] = 00 T_UICNF[XmtUQuad] = 1 T_UICNF[XmtUWidth] = 00

3.2 Other Register Values

Table 3 shows the register bits that affect behavior on the UTOPIA bus and shows what is supported by the reference design and what is not.

Table 3. IXF6012/IXF6048 Register Programmable Modes (Sheet 1 of 4)

Register	Field	Comments
GOCNF	QMode	Both single and quad transceiver modes are supported. See Table 2.
	CMode	Both concatenated and non-concatenated modes are supported. See Table 2.
	UAddrBase[2:0]	This document recommends that RXADDR[4:3] and TXADDR[4:3] be tied to 2'b11. RXADDR[2:0]/TXADDR[2:0] are connected to the reference design. This field should be programmed to 3'110 for proper operation.
R_COCNF	RcvChMode[1:0]	10 (ATM cell mode) or 11 (POS packet mode) is supported. R_COCNF[RcvChMode] and T_COCNF[XmtChMode] must be programmed to the same value.

Table 3. IXF6012/IXF6048 Register Programmable Modes (Sheet 2 of 4)

Register	Field	Comments
T_COCNF	XmtChMode[1:0]	10 (ATM cell mode) or 11 (POS packet mode) is supported. R_COCNF[RcvChMode] and T_COCNF[XmtChMode] must be programmed to the same value.
R_UICNF (global)	RcvATMHEC	Application dependent; the reference design does not care about the contents of the HEC byte.
	RcvSmallMem	Application dependent; the reference design does not know anything about the FIFO sizes in the IXF6012/IXF6048.
	RcvTestOEn	Should probably program to 1; unused signals should not be left floating; however, need to verify that unused signals are driven to idle (unasserted) values.
	RcvValCnf	Program to 1; RXVAL will be deasserted after the end of the packet or when the receive FIFO has run dry and will not be reasserted again until the port has been deselected and selected again. This is compliant with the POS-PHY specification.
	RcvFifEmptEOF	Program to 0; RXFA is asserted if the FIFO contains one or more EOFs or the number of words is equal to or greater than the highwater mark.
	RcvDirStatCnf	Program to 1 (RXFA_0, _1, _2, and _3 always driven).
	RcvMPhyDevCnf	Program to 0 (RXDATA, RXSOF, RXPRTY, and RXFA always driven). It is assumed that the IXF6012/IXF6048 is the only device connected to the reference design. Otherwise, program to 1.
	RcvUQuad	Both single and quad modes are supported. See Table 2.
	RcvUWidth[1:0]	Only 00 (8 bit interface), 01 (16 bit interface), and 10 (32 bit interface) are supported. 11 (64 bit interface) is not supported. See Table 2.
	RcvSelMode	Program to 0. We do not support “memory-mapped” mode.
R_UIIML (global)	RcvIML[7:0]	Due to the reference design’s block (64 byte) orientation, we should not use a value smaller than (000)00001.

Table 3. IXF6012/IXF6048 Register Programmable Modes (Sheet 3 of 4)

Register	Field	Comments
R_UICHCNF (per port)	RcvBurstCnf	The reference design never deasserts RXENB in the middle of a cell. However, 0 is recommended, since this matches more closely the UTOPIA spec.
	RcvFACnf	Must be programmed to 0 (RXFA_0, _1, _2, and _3 are active high).
	RcvPrtyCnf	Both even and odd parity is supported by the reference design. The PAR_MODE straps must be tied accordingly.
	RcvDRCnf	Both one and two clock cycle decode-response delay is supported by the reference design. The DR_MODE straps must be tied accordingly.
	RcvCellStruct	Application dependent: both 0 or 1 can be programmed. The reference design supports 52, 53, 54, and 56 byte cells. The only cell size not supported is 64 byte, which is only used in UTOPIA 64 bit mode, which the reference design does not support. The CELL_SIZE strap must be tied accordingly.
	RcvCADeassert[5:0]	This should be programmed to cause RXFA to be updated after the final word, per the UTOPIA Level 1/2 specifications.
R_PWM	RcvPWM[11:0]	The reference design and the IX Bus operates using 64 byte blocks, so the watermark should be set no lower than 64 bytes.
T_UICNF	XmtSmallMem	Application dependent; the reference design does not know anything about the IXF6012/IXF6048's internal FIFO sizes.
	XmtFifEmptEOF	0 means that transmission begins if there is an EOF or the threshold specified in T_UIIML is exceeded. 1 means that only T_UIIML is used. Either one should work for the reference design; this is probably application dependent.
	XmtDirStatCnf	Program to 1 (TXFA_0, _1, _2, _3 always driven).
	XmtMPhyDevCnf	Program to match R_UICNF[RcvMPhyDevCnf]).
	XmtUQuad	Both single and quad modes are supported by the reference design. This field must match R_UICNF[RcvUQuad]). See Table 2.
	XmtUWidth[1:0]	Only 00 (8 bit interface), 01 (16 bit interface), and 10 (32 bit interface) are supported. 11 (64 bit interface) is not supported. This field must match R_UICNF[RcvUWidth]. See Table 2.
	XmtSelMode	Program to 0. We do not support "memory-mapped" mode.
T_UIIML	XmtIML[7:0]	Application dependent.

Table 3. IXF6012/IXF6048 Register Programmable Modes (Sheet 4 of 4)

Register	Field	Comments
T_UICHCNF	XmtBurstCnf	The reference design will never deassert TXENB in the middle of a cell transfer; however, should program to 0 to match behavior in UTOPIA specs.
	XmtFACnf	Program to 0 (TXFA_0, _1, _2, and _3 active high).
	XmtPrtyCnf	Both even and odd parity is supported by the reference design. Must match what is programmed in R_UICHCNF[RcvPrtyCnf]. The PAR_MODE straps must be tied accordingly.
	XmtDRCnf	Both one and two clock cycle decode-response delay is supported by the reference design. Must match what is programmed in R_UICHCNF[RcvDRCnf]. The DR_MODE straps must be tied accordingly.
	XmtCellStruct	Both 0 or 1 can be programmed. The reference design supports 52, 53, 54, and 56 byte cells. The only cell size not supported is 64 byte, which is only used in UTOPIA 64 bit mode, which the reference design does not support. Must match R_UICHCNF[XmtCellStruct] (but why would it be different?). The CELL_SIZE straps must be tied accordingly.
	XmtCADeassert[5:0]	This should be set so that TXPFA/ TXSFA/TXFA is deasserted four cycles before the end of the cell, per the UTOPIA Level 1/2 specifications.
T_UIFDP	XmtFDCnf[7:0]	Use full FIFO depth unless there are special requirements which require a smaller FIFO depth.
T_NFPWM	XmtNFPWM[11:0]	Application dependent.
T_NEPWM	XmtNEPWM[11:0]	Application dependent.

4.0 Unsupported Features

The following modes are supported by the reference design, but are not supported by the IXF6012/IXF6048.

4.1 DSI 2x16 Mode

The IXF6012/IXF6048 only supports a 4x16 mode. It is not possible for a single device to support this. However, it is possible to use two devices, each running in DSI 2x16 mode, and connecting them to a single the IXF6012/IXF6048 device running in 4x16 mode.

4.2 DSI 1x16_2x8 Mode

This mode was added to the to support non-IXF6012/IXF6048 configurations. The IXF6012/IXF6048 itself does not support such a mode.

4.3 Parity Modes

The IXF6012/IXF6048 does not support “no parity” or “dual parity” modes.