

TC74VHC165F, TC74VHC165FN, TC74VHC165FS, TC74VHC165FT

8 - BIT SHIFT REGISTER (P - IN, S - OUT)

The TC74VHC165 is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

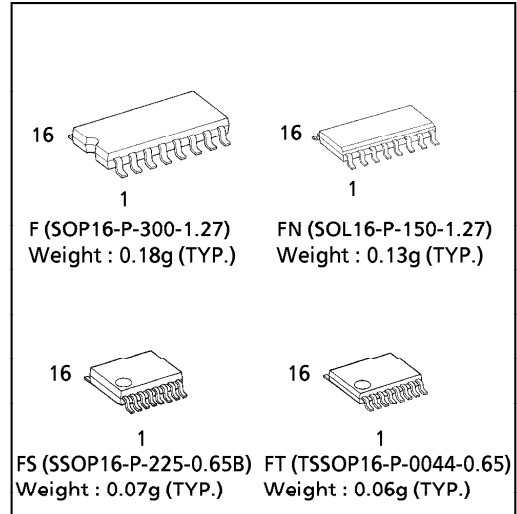
It consists of parallel-in or serial-in, serial-out 8 - bit shift register with a gated clock input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse. When the SHIFT/LOAD input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

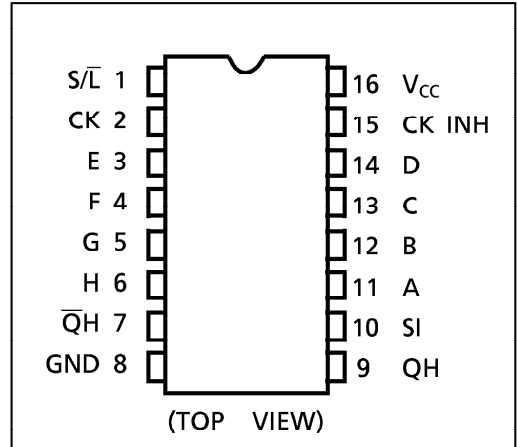
An Input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

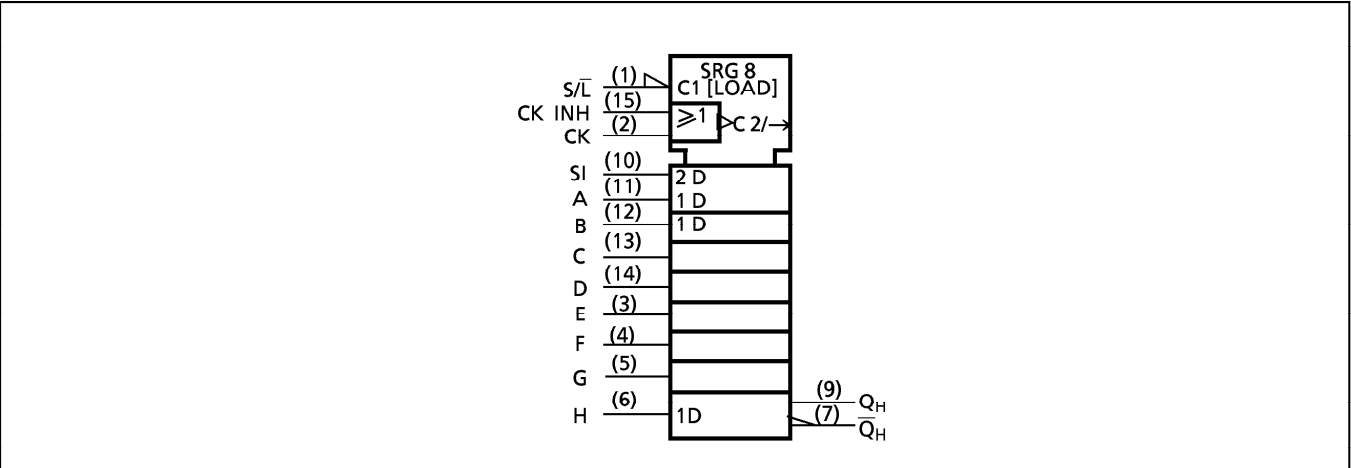
- High Speed $f_{MAX} = 150\text{MHz}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74ALS165



PIN ASSIGNMENT



IEC LOGIC SYMBOL



961001EBA2

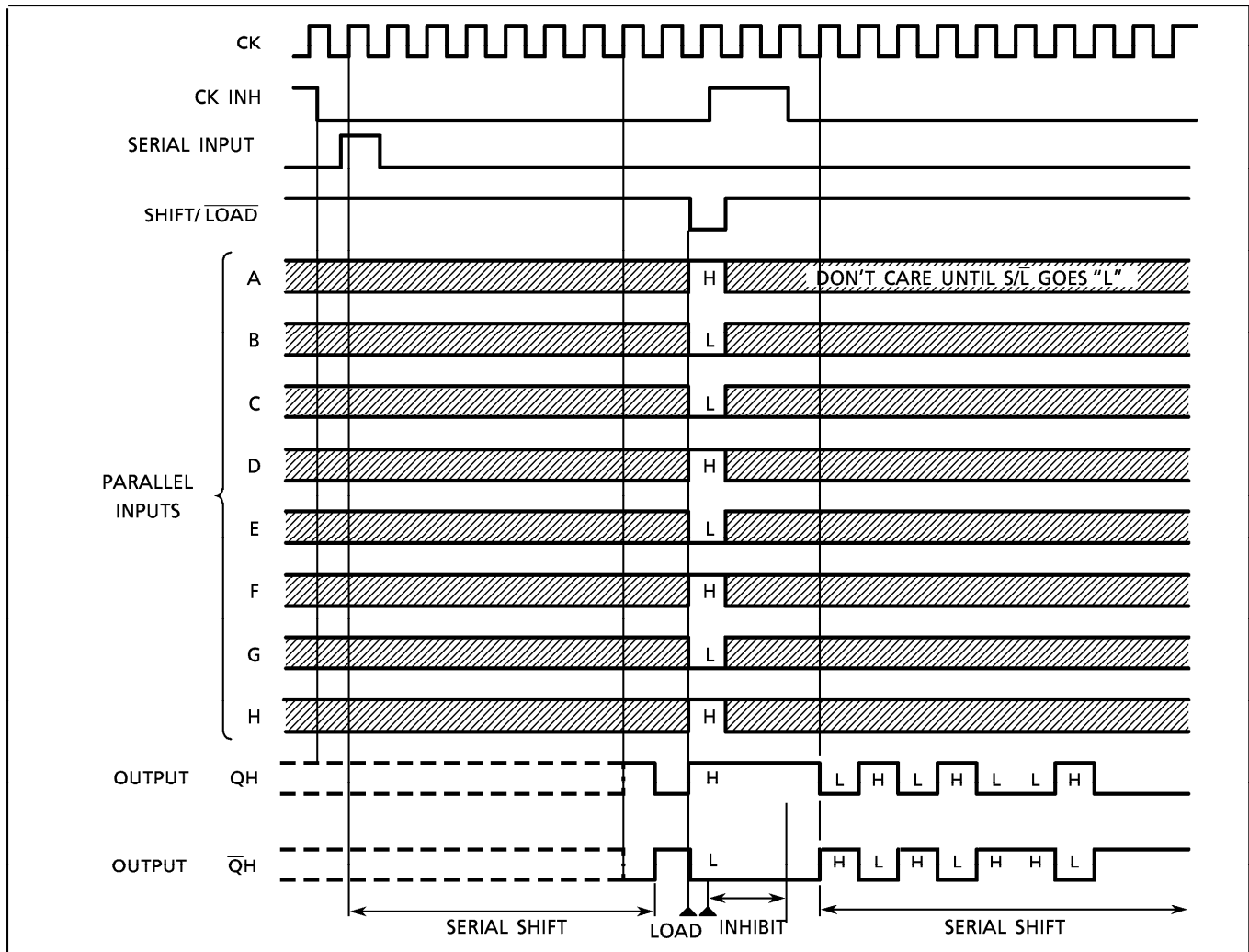
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TRUTH TABLE

| INPUTS | | | | | INTERNAL OUTPUTS | | OUTPUT | |
|------------|------------|------------|-----------|--------------------|------------------|-----|--------|------------------|
| SHIFT/LOAD | CLOCK INH | CLOCK | SERIAL IN | PARALLEL A H | QA | QB | QH | \overline{QH} |
| L | X | X | X | a h | a | b | h | \overline{h} |
| H | L | \uparrow | H | X | H | QAn | QGn | \overline{QGn} |
| H | L | \uparrow | L | X | L | QAn | QGn | \overline{QGn} |
| H | \uparrow | L | H | X | H | QAn | QGn | \overline{QGn} |
| H | \uparrow | L | L | X | L | QAn | QGn | \overline{QGn} |
| H | X | H | X | X | NO CHANGE | | | |
| H | H | X | X | X | NO CHANGE | | | |

X : Don't Care
 a h : The level of steady state input voltage at inputs A through H respectively
 QAn~QGn : The level of QA~QG, respectively, before the most recent positive transition of the CK.

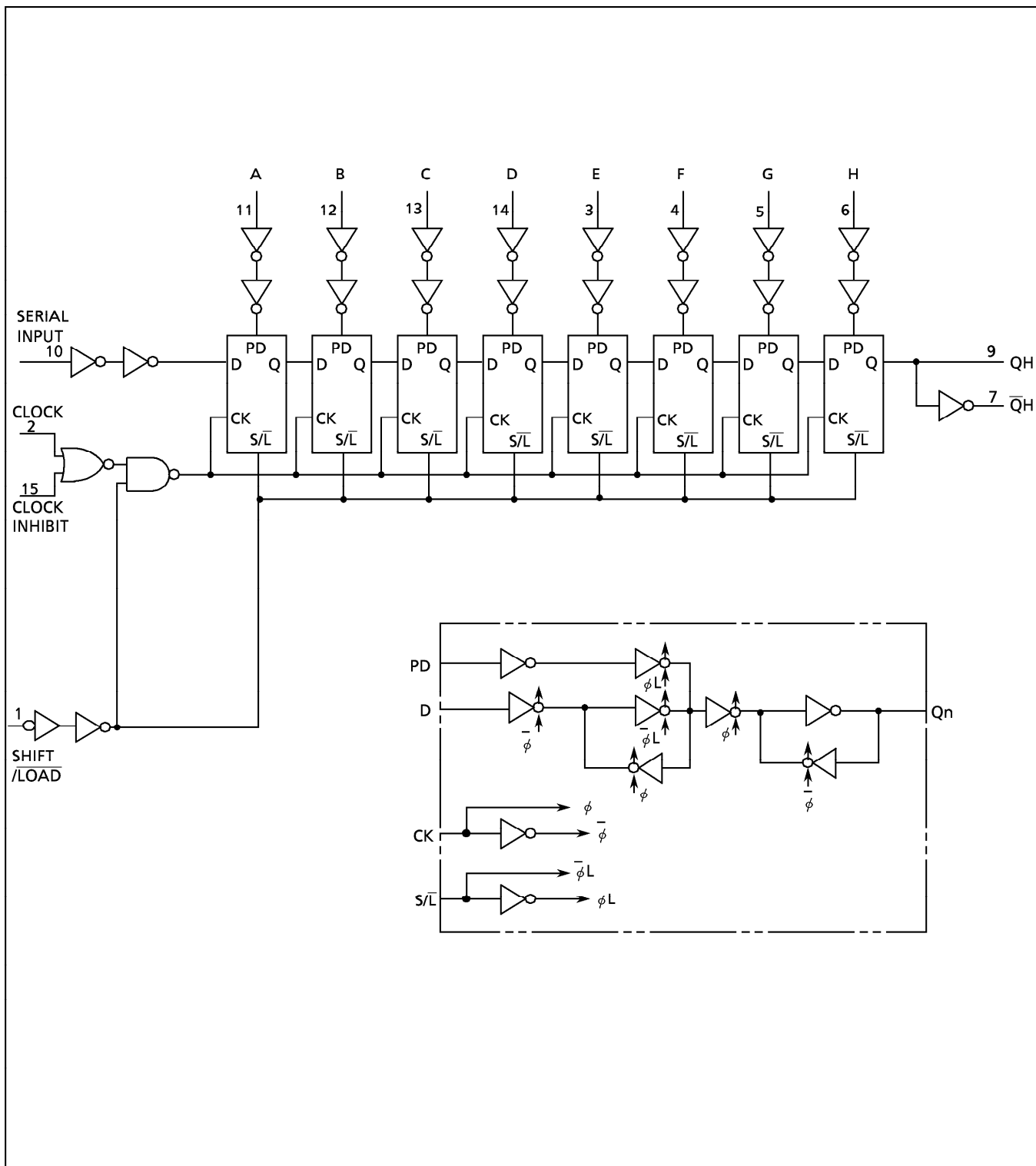
TIMING CHART



961001EBA2'

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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|-----------------------------|-----------|----------------------|------|
| Supply Voltage Range | V_{CC} | -0.5~7.0 | V |
| DC Input Voltage | V_{IN} | -0.5~7.0 | V |
| DC Output Voltage | V_{OUT} | -0.5~ $V_{CC} + 0.5$ | V |
| Input Diode Current | I_{IK} | -20 | mA |
| Output Diode Current | I_{OK} | ±20 | mA |
| DC Output Current | I_{OUT} | ±25 | mA |
| DC V_{CC} /Ground Current | I_{CC} | ±50 | mA |
| Power Dissipation | P_D | 180 | mW |
| Storage Temperature | T_{stg} | -65~150 | °C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNIT |
|--------------------------|-----------|---|------|
| Supply Voltage | V_{CC} | 2.0~5.5 | V |
| Input Voltage | V_{IN} | 0~5.5 | V |
| Output Voltage | V_{OUT} | 0~ V_{CC} | V |
| Operating Temperature | T_{opr} | -40~85 | °C |
| Input Rise and Fall Time | dt/dv | 0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$) | ns/V |

DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | V_{CC} (V) | $T_a = 25^\circ\text{C}$ | | | $T_a = -40 \sim 85^\circ\text{C}$ | | UNIT | |
|-----------------------------|-----------------------|--------------------------------------|---------------------------------|--------------------------|------|---------------------|-----------------------------------|---------------------|------|---------------|
| | | | | MIN. | TYP. | MAX. | MIN. | MAX. | | |
| High - Level Input Voltage | V_{IH} | | 2.0 | 1.50 | — | — | 1.50 | — | V | |
| | | | 3.0~5.5 | $V_{CC} \times 0.7$ | — | — | $V_{CC} \times 0.7$ | — | | |
| Low - Level Input Voltage | V_{IL} | | 2.0 | — | — | 0.50 | — | 0.50 | V | |
| | | | 3.0~5.5 | — | — | $V_{CC} \times 0.3$ | — | $V_{CC} \times 0.3$ | | |
| High - Level Output Voltage | V_{OH} | $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -50 \mu\text{A}$ | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | | |
| | | | | $I_{OH} = -4\text{mA}$ | 3.0 | 2.58 | — | — | 2.48 | |
| Low - Level Output Voltage | V_{OL} | $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 50 \mu\text{A}$ | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | | |
| | | | | $I_{OL} = 4\text{mA}$ | 3.0 | — | — | 0.36 | — | |
| 4.5 | $I_{OL} = 8\text{mA}$ | — | — | 0.36 | — | 0.44 | | | | |
| | Input Leakage Current | I_{IN} | $V_{IN} = 5.5V \text{ or } GND$ | 0~5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent Supply Current | I_{CC} | $V_{IN} = V_{CC} \text{ or } GND$ | 5.5 | — | — | 4.0 | — | 40.0 | | |

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

| PARAMETER | SYMBOL | TEST CONDITION | Ta = 25°C | | Ta = -40~85°C | | UNIT |
|--|--|----------------|---------------------|-------|---------------|-------|------|
| | | | V _{CC} (V) | LIMIT | LIMIT | LIMIT | |
| Minimum Pulse Width (CK, CK INH) | t _{W(L)} t _{W(H)} | | 3.3 ± 0.3 | 6.0 | 7.0 | ns | |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum Pulse Width (S/ \bar{L}) | t _{W(L)} | | 3.3 ± 0.3 | 7.5 | 9.0 | | |
| | | | 5.0 ± 0.5 | 5.0 | 6.0 | | |
| Minimum Set-up Time (PI-S/ \bar{L}) | t _s | | 3.3 ± 0.3 | 7.5 | 8.5 | | |
| | | | 5.0 ± 0.5 | 5.0 | 5.0 | | |
| Minimum Set-up Time (SI-CK, CK INH) | t _s | | 3.3 ± 0.3 | 5.0 | 6.0 | | |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum Set-up Time (S/ \bar{L} -CK, CK INH) | t _s | | 3.3 ± 0.3 | 5.0 | 6.0 | | |
| | | | 5.0 ± 0.5 | 4.0 | 4.0 | | |
| Minimum Hold Time (PI-S/ \bar{L}) | t _h | | 3.3 ± 0.3 | 0.5 | 0.5 | | |
| | | | 5.0 ± 0.5 | 1.0 | 1.0 | | |
| Minimum Hold Time (SI-CK, CK INH) | t _h | | 3.3 ± 0.3 | 0.0 | 0.0 | | |
| | | | 5.0 ± 0.5 | 0.5 | 0.5 | | |
| Minimum Hold Time (S/ \bar{L} -CK, CK INH) | t _h | | 3.3 ± 0.3 | 0.0 | 0.0 | | |
| | | | 5.0 ± 0.5 | 0.5 | 0.5 | | |
| Minimum Removal Time (CK INH-CK) (CK-CK INH) | t _{rem} | | 3.3 ± 0.3 | 5.0 | 5.0 | | |
| | | | 5.0 ± 0.5 | 3.5 | 3.5 | | |

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

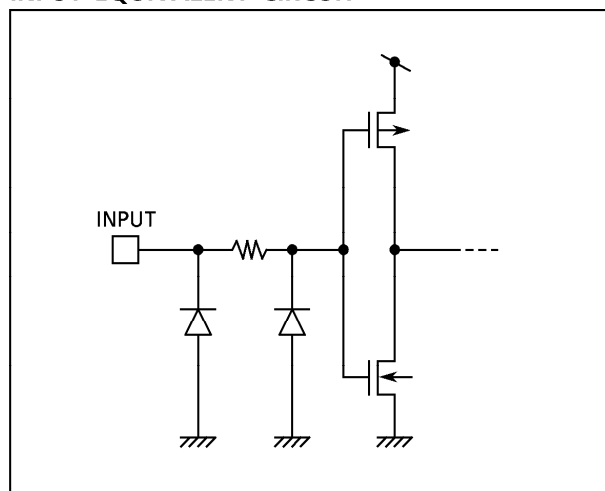
| PARAMETER | SYMBOL | TEST CONDITION | | Ta = 25°C | | | Ta = -40~85°C | | UNIT | |
|---|------------------|---------------------|---------|-----------|------|------|---------------|------|------|-----|
| | | V _{CC} (V) | CL (pF) | MIN. | TYP. | MAX. | MIN. | MAX. | | |
| Propagation Delay Time (CK, CK INH-QH, QH) | t _{pLH} | 3.3 ± 0.3 | 15 | — | 9.9 | 15.4 | 1.0 | 18.0 | ns | |
| | | | 50 | — | 12.4 | 18.9 | 1.0 | 21.5 | | |
| | t _{pHL} | 5.0 ± 0.5 | 15 | — | 6.6 | 9.9 | 1.0 | 11.5 | | |
| | | | 50 | — | 8.1 | 11.9 | 1.0 | 13.5 | | |
| Propagation Delay Time (S/L-QH, QH) | t _{pLH} | 3.3 ± 0.3 | 15 | — | 9.9 | 15.8 | 1.0 | 18.5 | | ns |
| | | | 50 | — | 12.4 | 19.3 | 1.0 | 22.0 | | |
| | t _{pHL} | 5.0 ± 0.5 | 15 | — | 6.7 | 9.9 | 1.0 | 11.5 | | |
| | | | 50 | — | 8.2 | 11.9 | 1.0 | 13.5 | | |
| Propagation Delay Time (H-QH, QH) | t _{pLH} | 3.3 ± 0.3 | 15 | — | 9.2 | 14.1 | 1.0 | 16.5 | ns | |
| | | | 50 | — | 11.7 | 17.6 | 1.0 | 20.0 | | |
| | t _{pHL} | 5.0 ± 0.5 | 15 | — | 5.9 | 9.0 | 1.0 | 10.5 | | |
| | | | 50 | — | 7.4 | 11.0 | 1.0 | 12.5 | | |
| Maximum Clock Frequency | f _{MAX} | 3.3 ± 0.3 | 15 | 65 | 85 | — | 55 | — | | MHz |
| | | | 50 | 60 | 105 | — | 50 | — | | |
| | | 5.0 ± 0.5 | 15 | 110 | 150 | — | 90 | — | | |
| | | | 50 | 95 | 130 | — | 85 | — | | |
| Input Capacitance | C _{IN} | | | — | 4 | 10 | — | 10 | pF | |
| Power Dissipation Capacitance | C _{PD} | (Note 1) | | — | 50 | — | — | — | | |

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

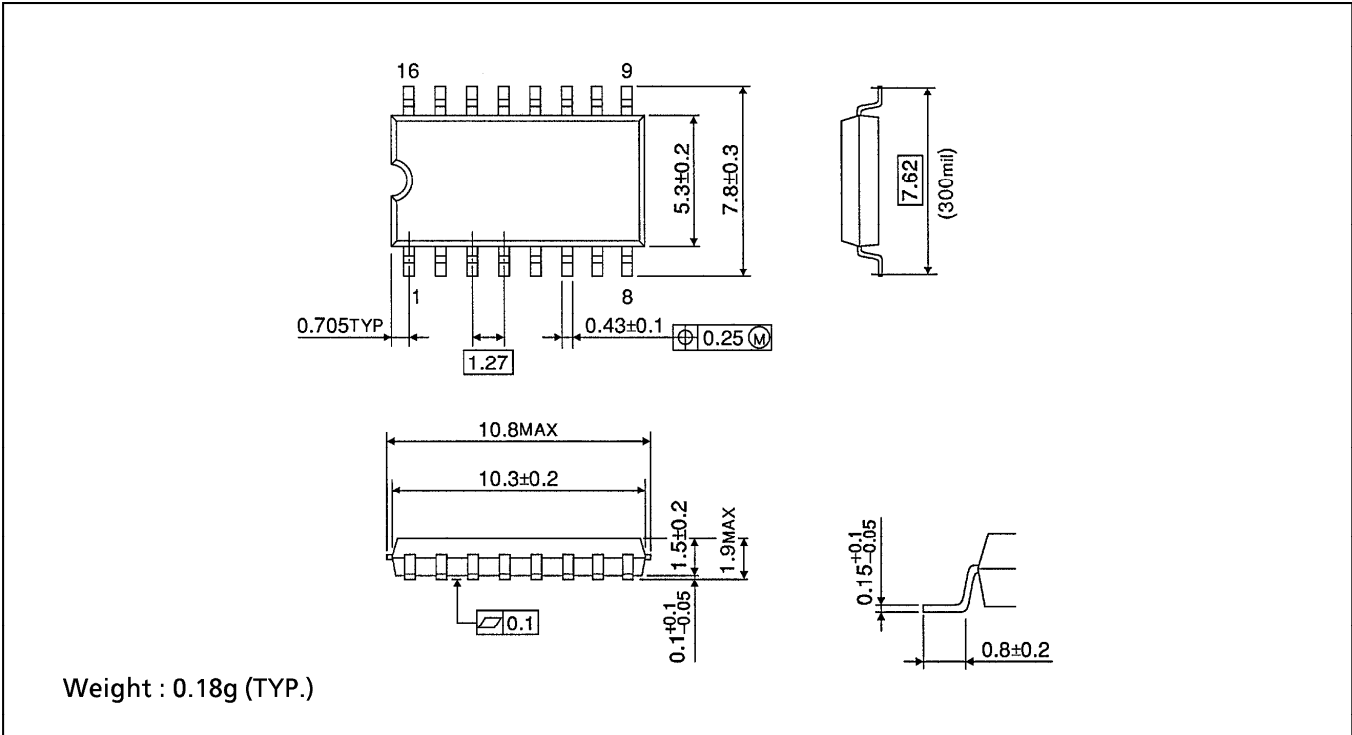
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

INPUT EQUIVALENT CIRCUIT



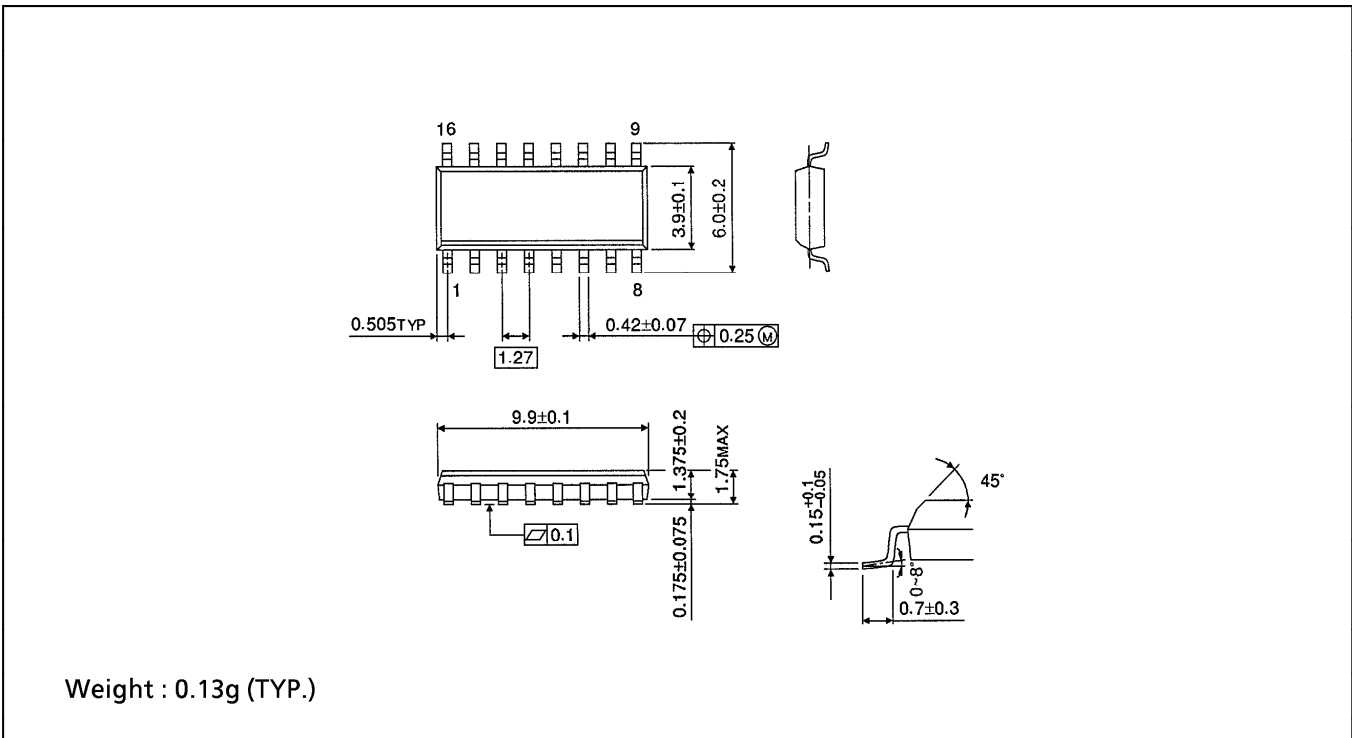
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm



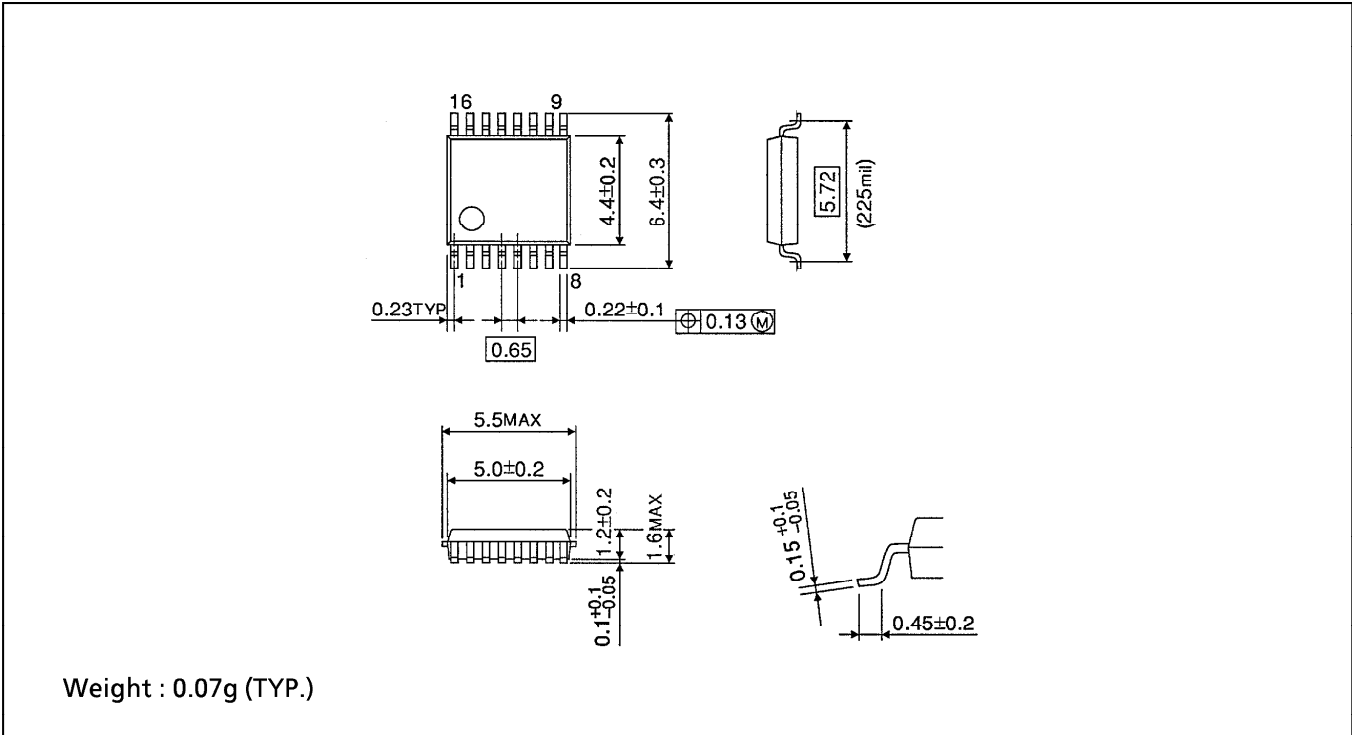
SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOP16-P-150-1.27)

Unit in mm



SSOP 16PIN OUTLINE DRAWING (SSOP16-P-225-0.65B)

Unit in mm



TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)

Unit in mm

