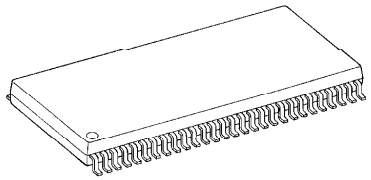
ADVANCE INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16500FT

LOW-VOLTAGE 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16500FT is a high performance CMOS 18-bit UNIVERSAL BUS TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6V.
Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CKAB}}$ and $\overline{\text{CKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch / flip-flop on the high-to-low transition of $\overline{\text{CKAB}}$.



TSSOP56-P-0061-0.50

Weight : 0.25g (Typ.)

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CKBA. When the $\overline{\text{OE}}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3 – state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.

PRELIMINARY

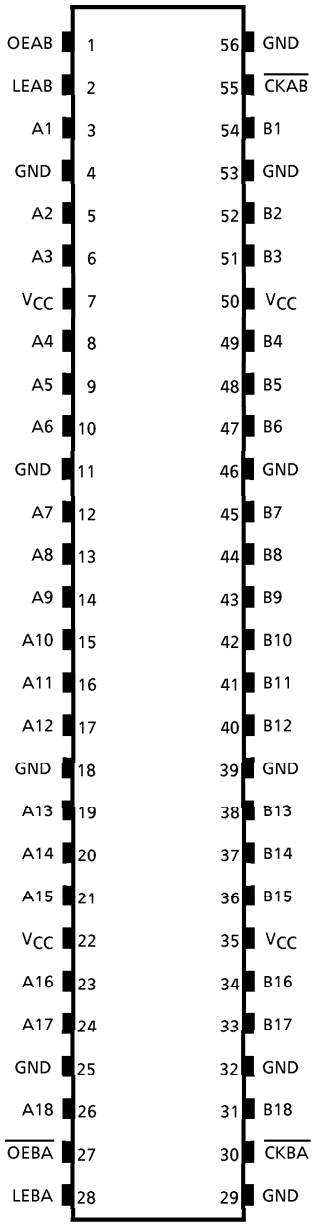
FEATURES

- Low Voltage Operation : V_{CC} = 1.8~3.6V
- High Speed Operation : t_{pd} = TBD (max.) at V_{CC} = 3.0~3.6V
  : t_{pd} = TBD (max.) at V_{CC} = 2.3~2.7V
  : t_{pd} = TBD (max.) at V_{CC} = 1.8V
- 3.6V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ± 24mA (min.) at V_{CC} = 3.0V
  : I_{OH} / I_{OL} = ± 18mA (min.) at V_{CC} = 2.3V
  : I_{OH} / I_{OL} = ± 6mA (min.) at V_{CC} = 1.8V
- Latch-up Performance : ± 300mA
- ESD Performance : Human Body Model > ± 2000V
  : Machine Model > ± 200V
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs.

Note 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

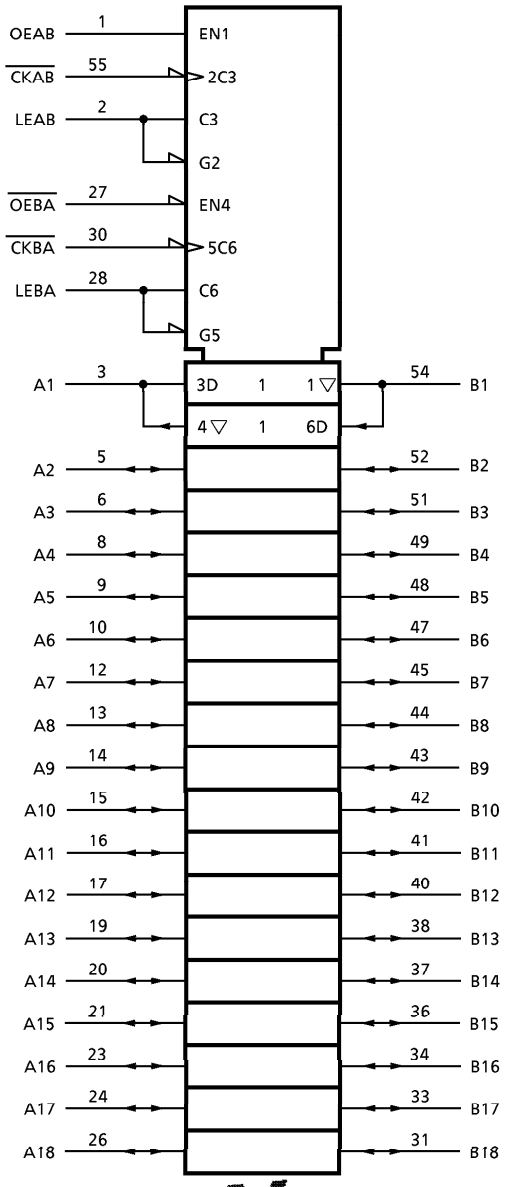
961001EBA2

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



PRELIMINARY

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TRUTH TABLE *

INPUTS				OUTPUTS
OEAB	LEAB	$\overline{CKAB}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B0**
H	L	L	X	B0***

* A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CKBA}$.
** Output level before the indicated steady-state input conditions were established.
*** Output level before the indicated steady-state input conditions were established, provided that $\overline{CKAB}$ was low before LEAB went low.

SYSTEM DIAGRAM

PRELIMINARY