IS61LV51216

512K x 16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM WITH 3.3V SUPPLY

ADVANCED INFORMATION
FEBRUARY 2002

FEATURES

- High-speed access time:
  — 8, 10, and 12 ns
- CMOS low power operation
- Low stand-by power:
  — Less than 5 mA (typ.) CMOS stand-by
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available

DESCRIPTION

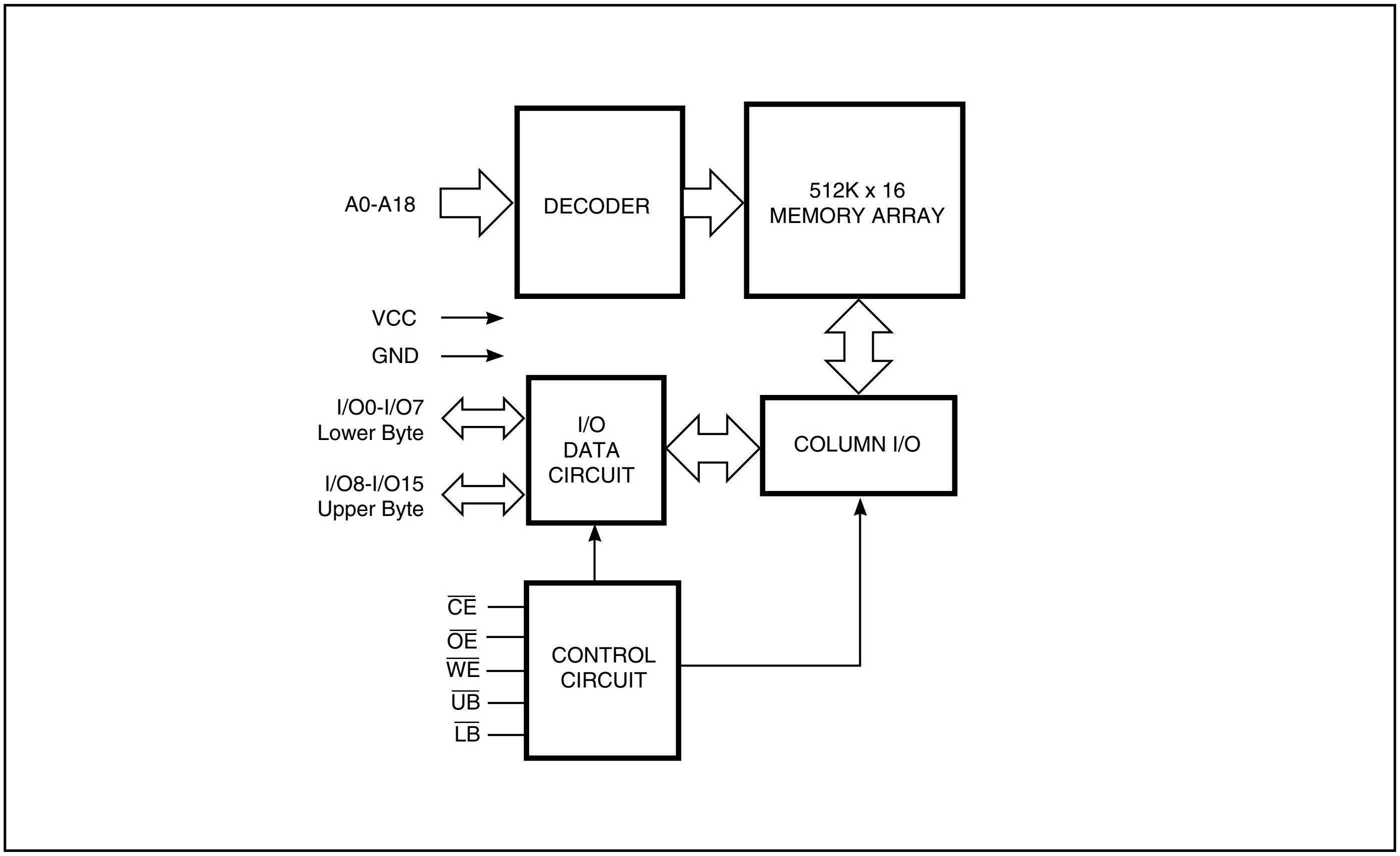
The *ISSI* IS61LV51216 is a high-speed, 8M-bit static RAM organized as 525,288 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The active LOW Write Enable ($\overline{\text{WE}}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{\text{UB}}$) and Lower Byte ($\overline{\text{LB}}$) access.

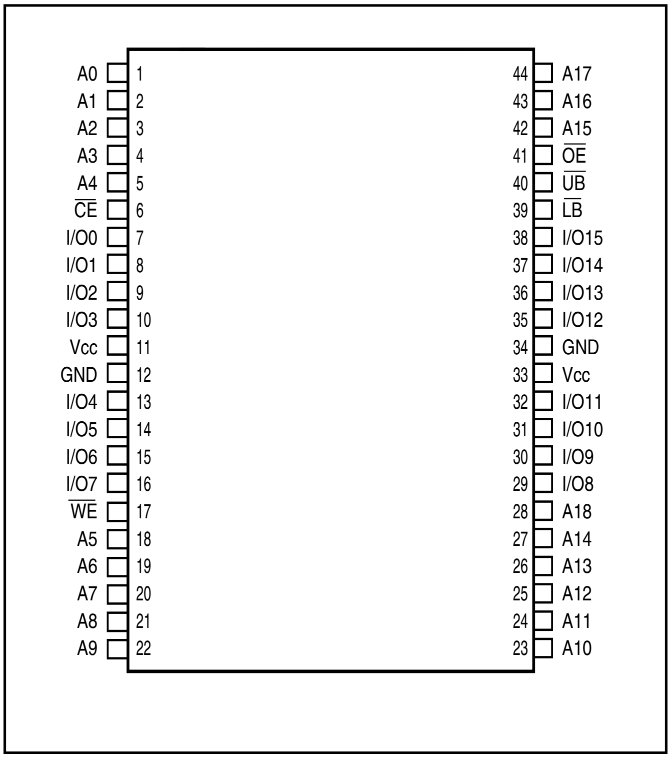
The IS61LV51216 is packaged in the JEDEC standard 44-pin TSOP Type II and 48-pin Mini BGA (10mm x 12mm).

FUNCTIONAL BLOCK DIAGRAM



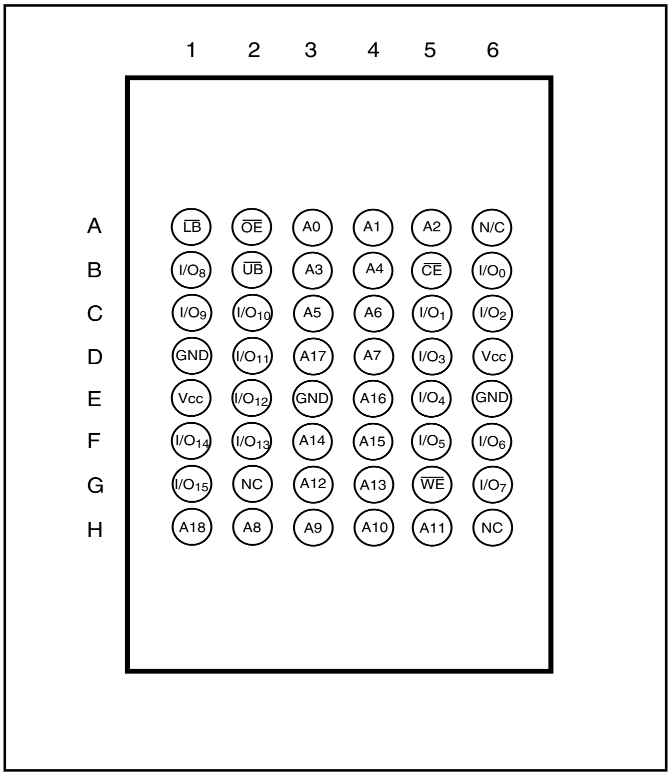
PIN CONFIGURATIONS

44-Pin TSOP (Type II)



Name	Pin	Pin	Name
A0	1	44	A17
A1	2	43	A16
A2	3	42	A15
A3	4	41	$\overline{OE}$
A4	5	40	$\overline{UB}$
$\overline{CE}$	6	39	$\overline{LB}$
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
Vcc	11	34	GND
GND	12	33	Vcc
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
$\overline{WE}$	17	28	A18
A5	18	27	A14
A6	19	26	A13
A7	20	25	A12
A8	21	24	A11
A9	22	23	A10

48-Pin mini BGA (10mmx12mm)



	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	N/C
B	I/O$_8$	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O$_0$
C	I/O$_9$	I/O$_{10}$	A5	A6	I/O$_1$	I/O$_2$
D	GND	I/O$_{11}$	A17	A7	I/O$_3$	Vcc
E	Vcc	I/O$_{12}$	GND	A16	I/O$_4$	GND
F	I/O$_{14}$	I/O$_{13}$	A14	A15	I/O$_5$	I/O$_6$
G	I/O$_{15}$	NC	A12	A13	$\overline{WE}$	I/O$_7$
H	A18	A8	A9	A10	A11	NC

PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

TRUTH TABLE

						I/O PIN		
Mode	**$\overline{\text{WE}}$**	**$\overline{\text{CE}}$**	**$\overline{\text{OE}}$**	**$\overline{\text{LB}}$**	**$\overline{\text{UB}}$**	**I/O0-I/O7**	**I/O8-I/O15**	**Vcc Current**
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	–45 to +90	°C
V_{CC}	Vcc Related to GND	–0.3 to +4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V +10%, -5%
Industrial	–40°C to +85°C	3.3V +10%, -5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–1 –5	1 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC} Outputs Disabled	Com. Ind.	–1 –5	1 5	µA

Notes:
1. V_{IL} (min.) = –2.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-8		-10		-12		
Symbol	**Parameter**	**Test Conditions**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	230 240	— —	220 230	— —	210 220	mA
I_{SB}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = f_{MAX}.	Com. Ind.	— —	85 95	— —	75 95	— —	75 85	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com. Ind.	— —	50 55	— —	50 55	— —	50 55	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	— —	40 45	— —	40 45	— —	40 45	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE}	$\overline{\text{CE}}$ Access Time	—	8	—	10	—	12	ns
t_{DOE}	$\overline{\text{OE}}$ Access Time	—	3.5	—	4	—	5	ns
t_{HZOE}(2)	$\overline{\text{OE}}$ to High-Z Output	—	3	—	4	0	5	ns
t_{LZOE}(2)	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZCE}(2	$\overline{\text{CE}}$ to High-Z Output	0	3	0	4	0	6	ns
t_{LZCE}(2)	$\overline{\text{CE}}$ to Low-Z Output	3	—	3	—	3	—	ns
t_{BA}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Access Time	—	3.5	—	4	—	5	ns
t_{HZB}(2)	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to High-Z Output	0	3	0	3	0	4	ns
t_{LZB}(2)	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{PU}	Power Up Time	0	—	0	—	0	—	ns
t_{PD}	Power Down Time	—	8	—	10	—	12	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

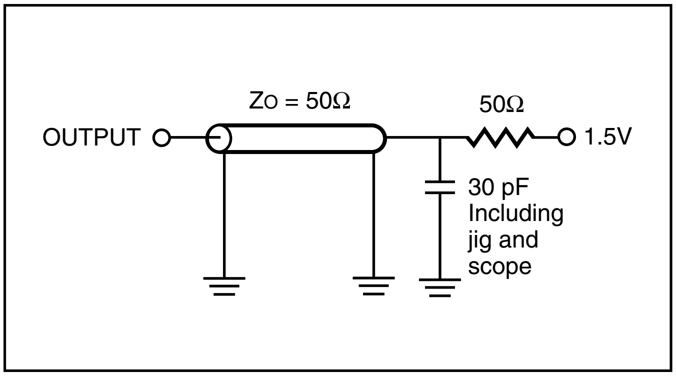


Figure 1

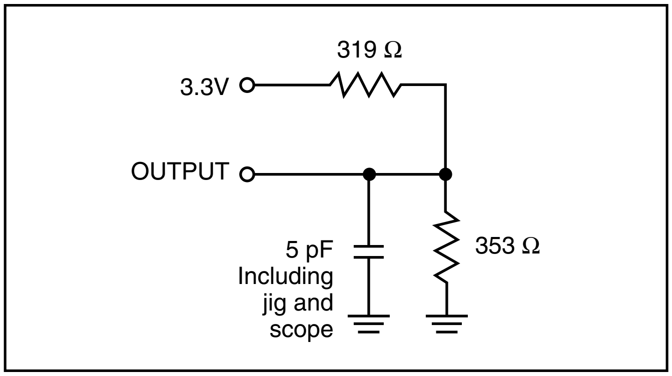
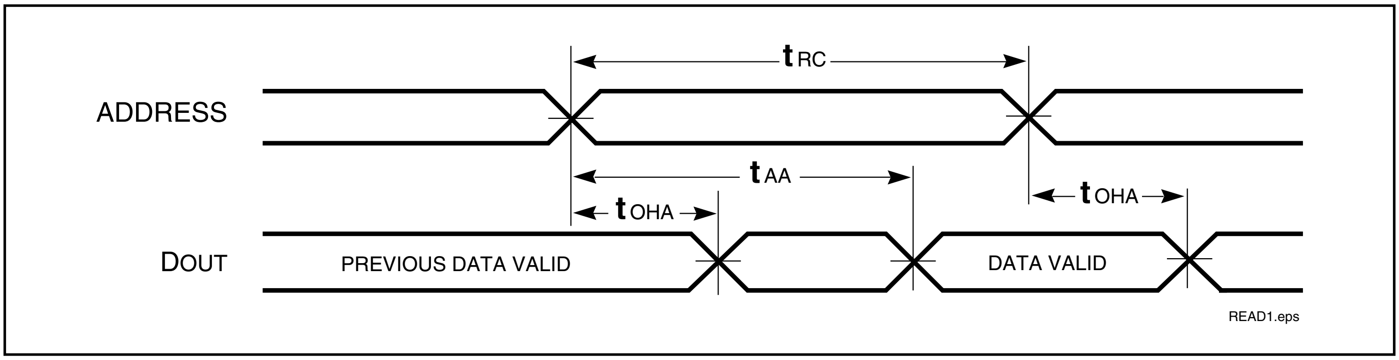


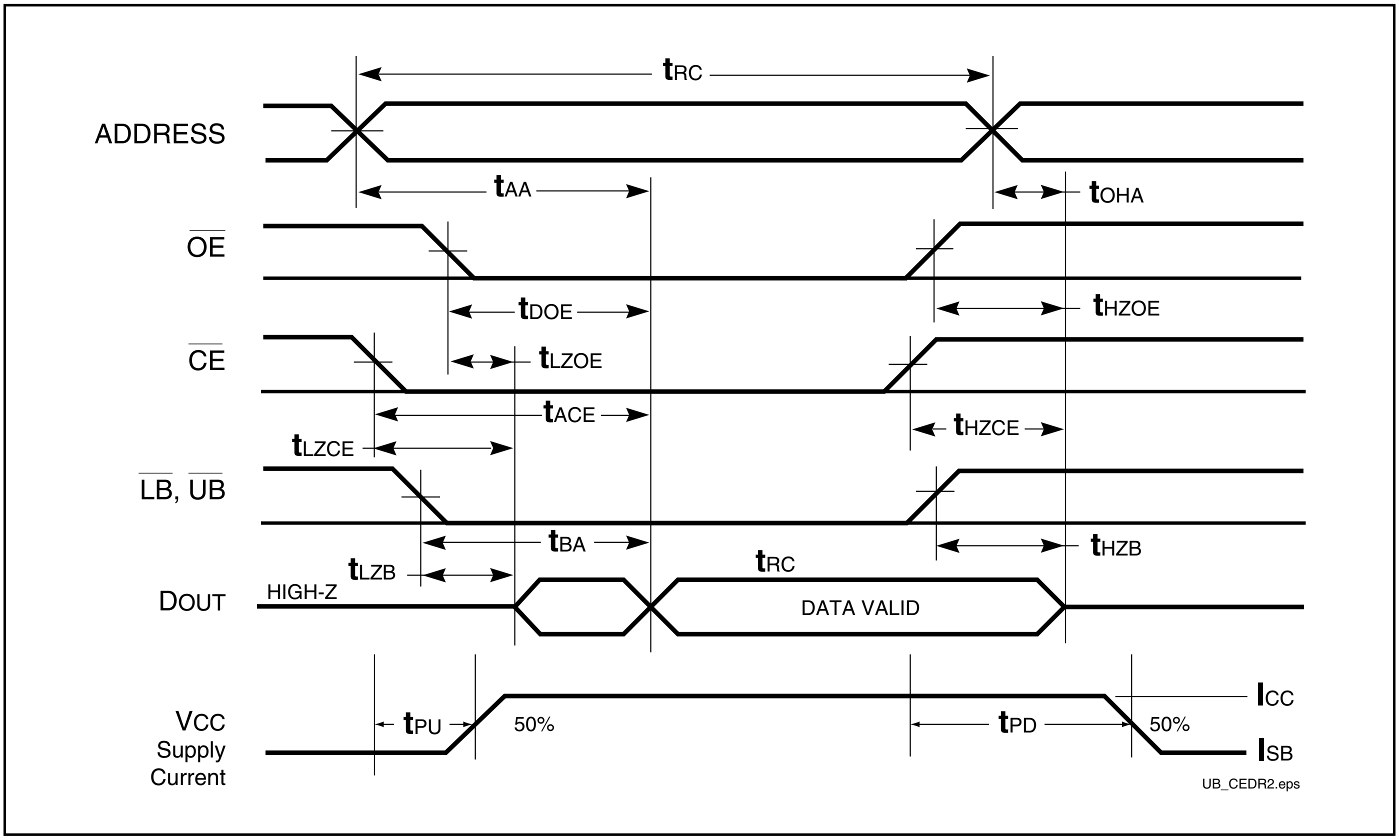
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1(1,2) (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2(1,3)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

Symbol	Parameter	-8 Min.	 Max.	-10 Min.	 Max.	-12 Min.	 Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	8	—	ns
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	6.5	—	8	—	8	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	6.5	—	8	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	6.5	—	10	—	12	—	ns
t_{SD}	Data Setup to Write End	4	—	6	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}(2)	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	—	6	ns
t_{LZWE}(2)	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	2	—	ns

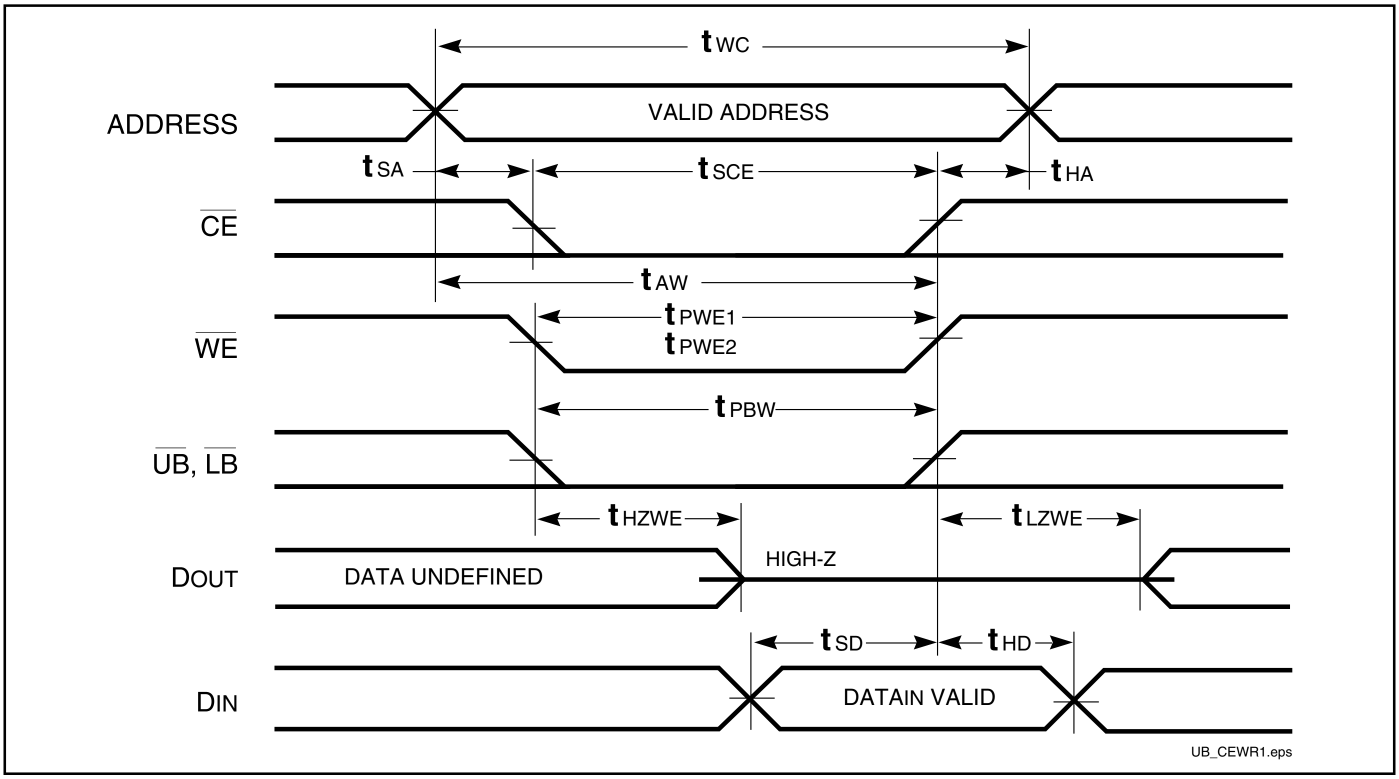
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

Shaded area product in development

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{\text{CE}}$ Controlled, $\overline{\text{OE}}$ is HIGH or LOW) (1)

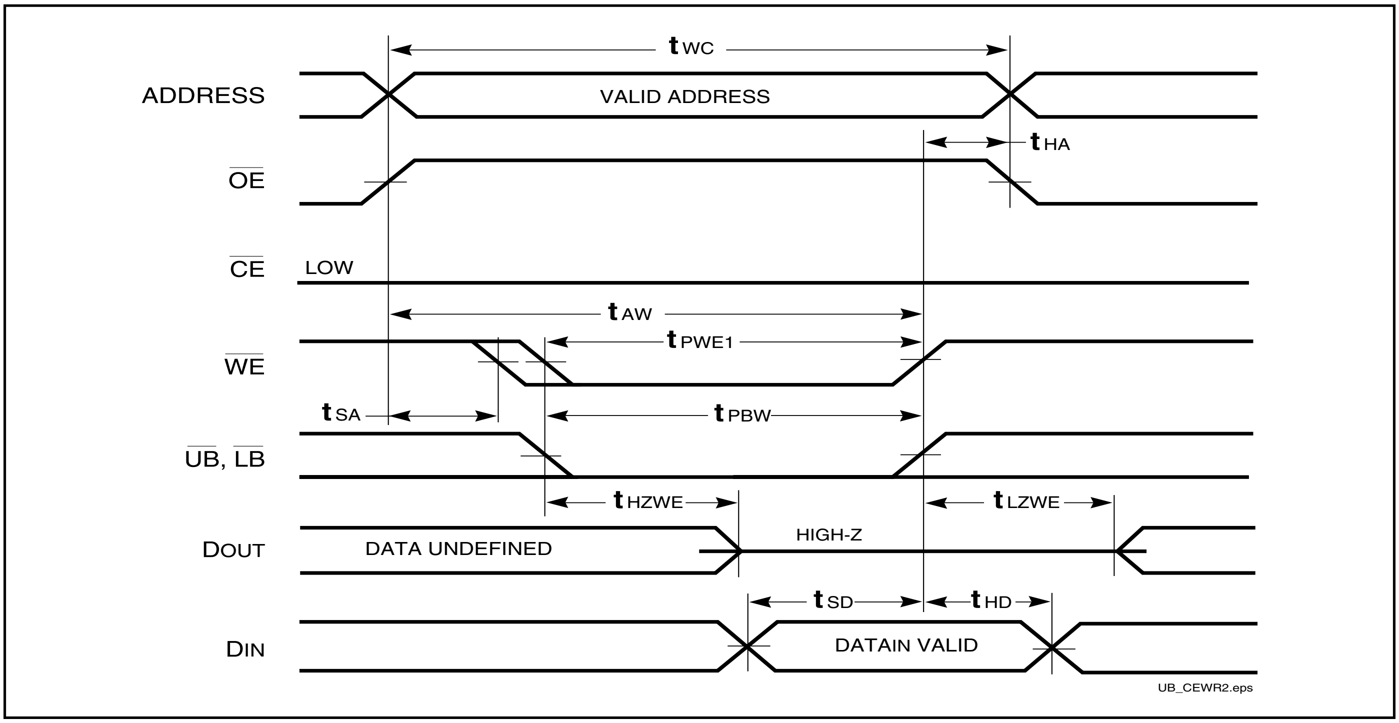


Notes:

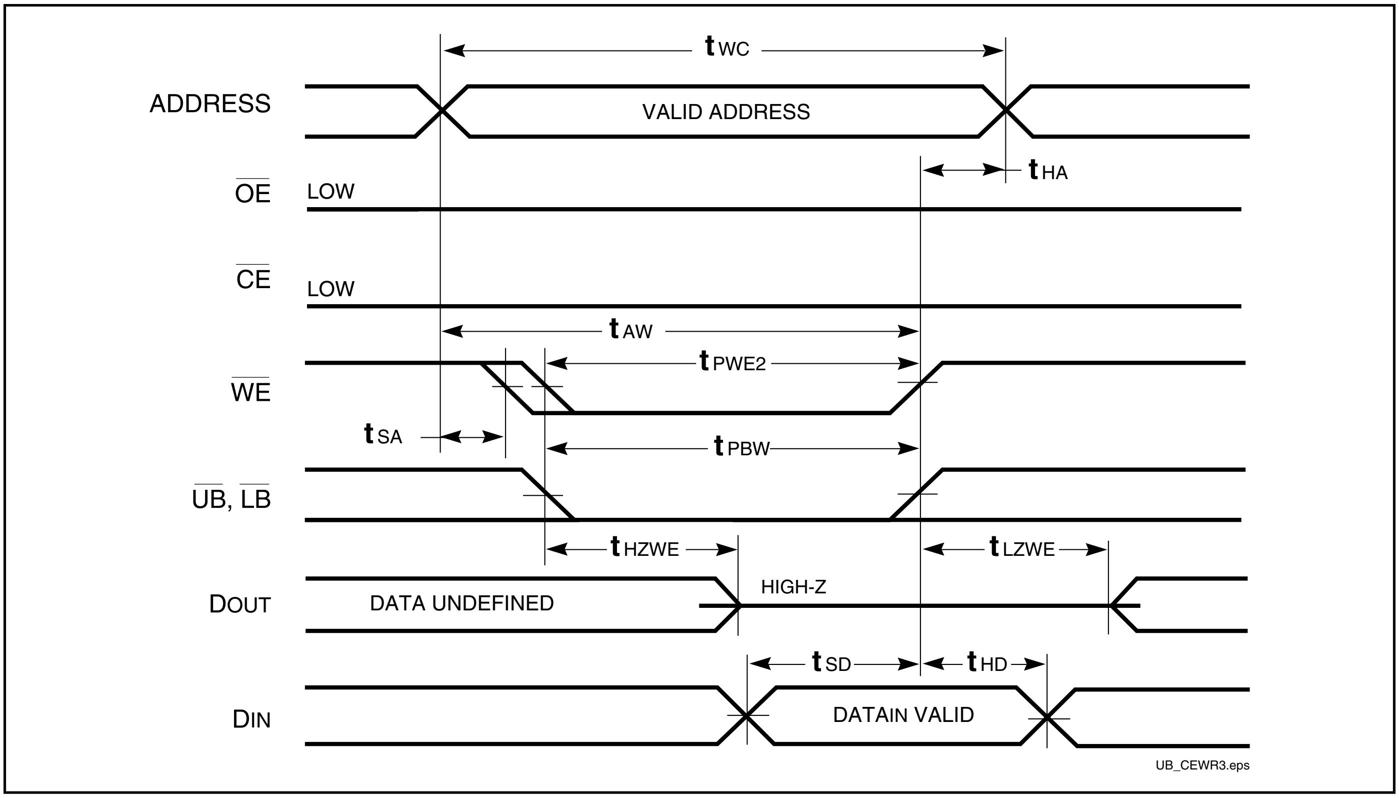
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ inputs and at least one of the $\overline{\text{LB}}$ and $\overline{\text{UB}}$ inputs being in the LOW state.
2. WRITE = ($\overline{\text{CE}}$) [($\overline{\text{LB}}$) = ($\overline{\text{UB}}$)] ($\overline{\text{WE}}$).

AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{\text{WE}}$ Controlled. $\overline{\text{OE}}$ is HIGH During Write Cycle) (1,2)

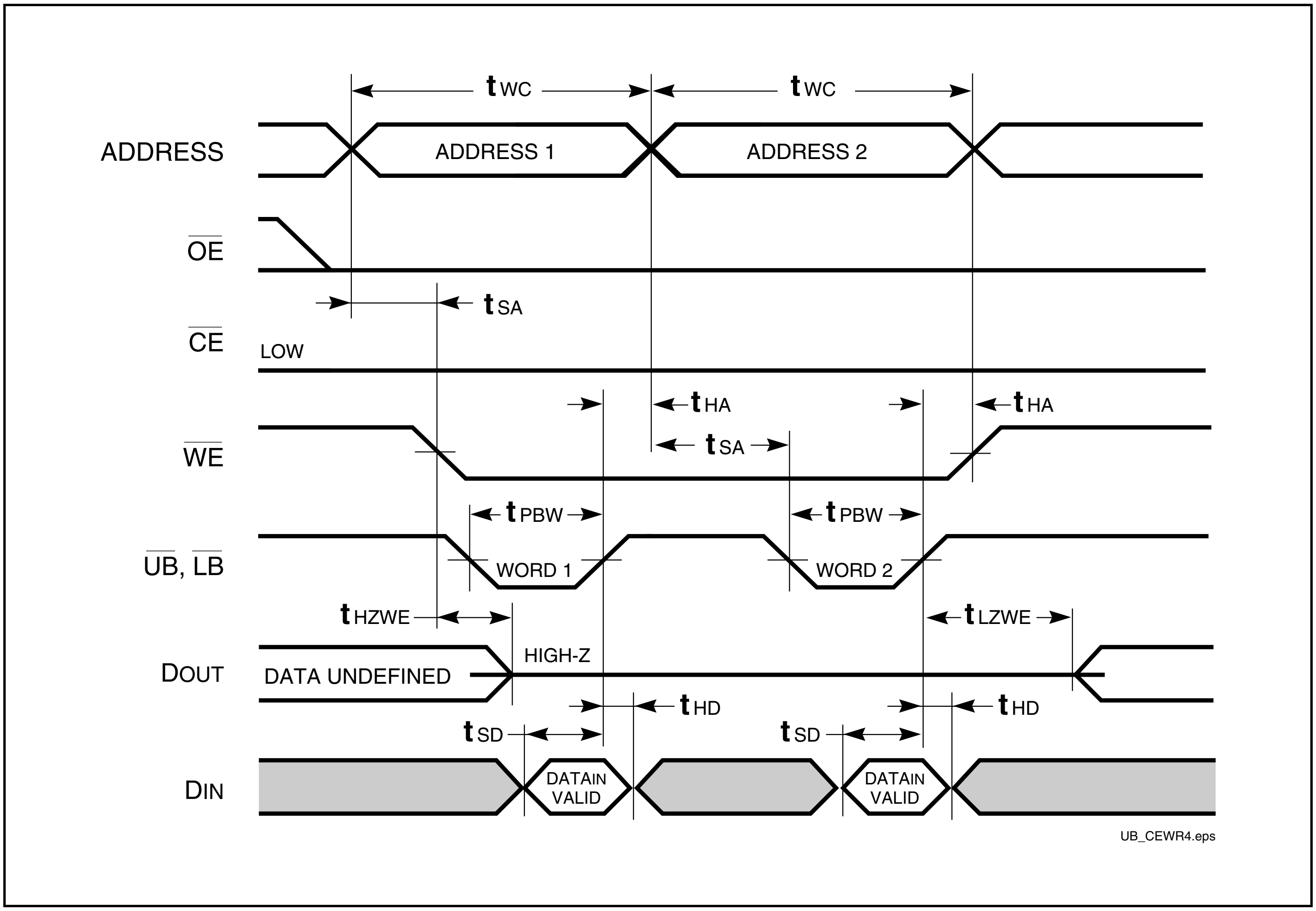


WRITE CYCLE NO. 3 ($\overline{\text{WE}}$ Controlled. $\overline{\text{OE}}$ is LOW During Write Cycle) (1)



AC WAVEFORMS

WRITE CYCLE NO. 4 ($\overline{LB}$, $\overline{UB}$ Controlled, Back-to-Back Write) (1,3)



Notes:

1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW, $\overline{UB}$ and/or $\overline{LB}$ = LOW, and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{LB}$, $\overline{UB}$ pins can be used to control the Write function.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
8	IS61LV51216-8T IS61LV51216-8B	TSOP (Type II) Mini BGA (10mm x 12mm)
10	IS61LV51216-10T IS61LV51216-10B	TSOP (Type II) Mini BGA (10mm x 12mm)
12	IS61LV51216-12T IS61LV51216-12B	TSOP (Type II) Mini BGA (10mm x 12mm)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS61LV51216-8TI IS61LV51216-8BI	TSOP (Type II) Mini BGA (10mm x 12mm)
10	IS61LV51216-10TI IS61LV51216-10BI	TSOP (Type II) Mini BGA (10mm x 12mm)
12	IS61LV51216-12TI IS61LV51216-12BI	TSOP (Type II) Mini BGA (10mm x 12mm)

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