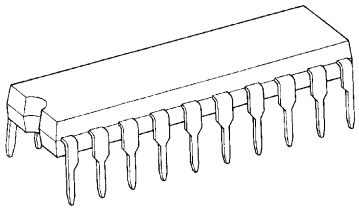
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62C851P,TD62C852P

8BIT SERIAL−IN PARALLEL−OUT SHIFT REGISTER / LATCH DRIVERS

The TD62C851P and TD62C852P are monolithic circuits designed to be used together with Bi−CMOS integrated circuits. The devices consist of a 8bit shift register, 8bit latches, and 8 output circuits (integral clamp diodes for switching inductive loads).



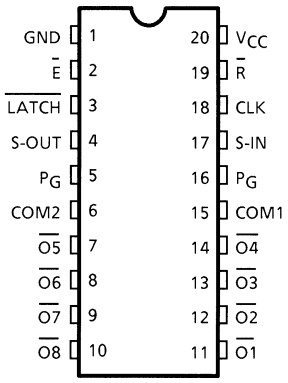
DIP20-P-300-2.54A

Weight: 2.25 g (Typ.)

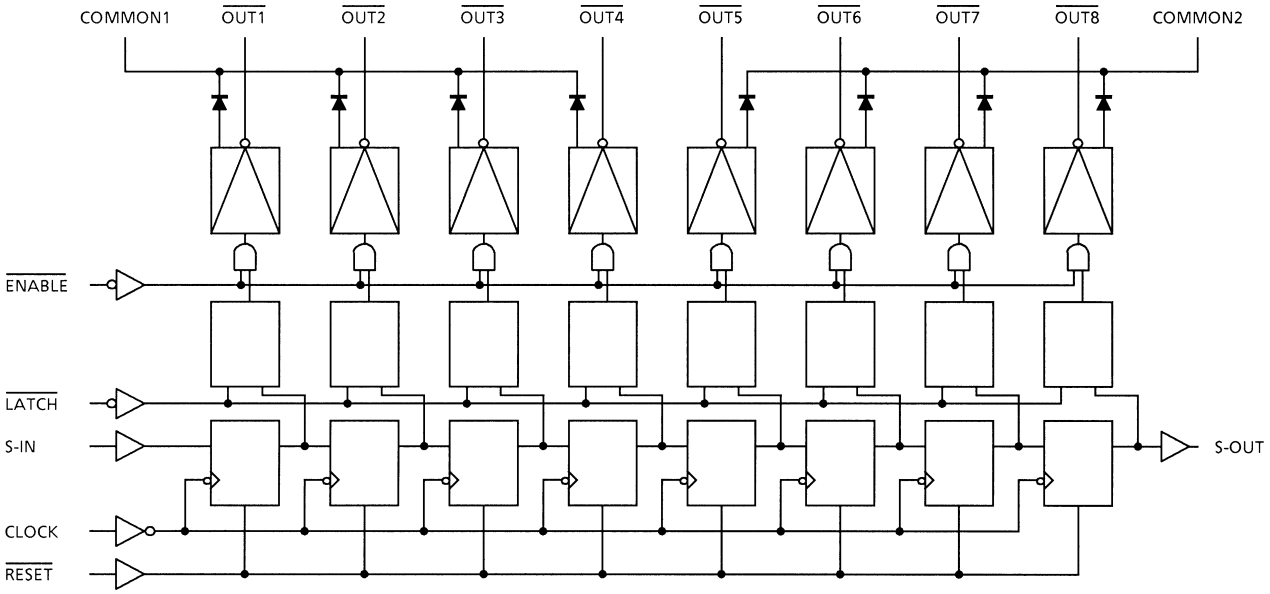
FEATURES

- 8bit serial−in parallel−out shift register / latch driver (Bi−CMOS process)
- Output sustaining voltage ; 50 V
- Output current ;
  TD62C851P 200 mA / ch (Low saturation type)
  TD62C852P 500 mA / ch (darlington type)
- Built−in output clamp diodes
- CMOS compatible inputs
- Package ; DIP20−P−300A

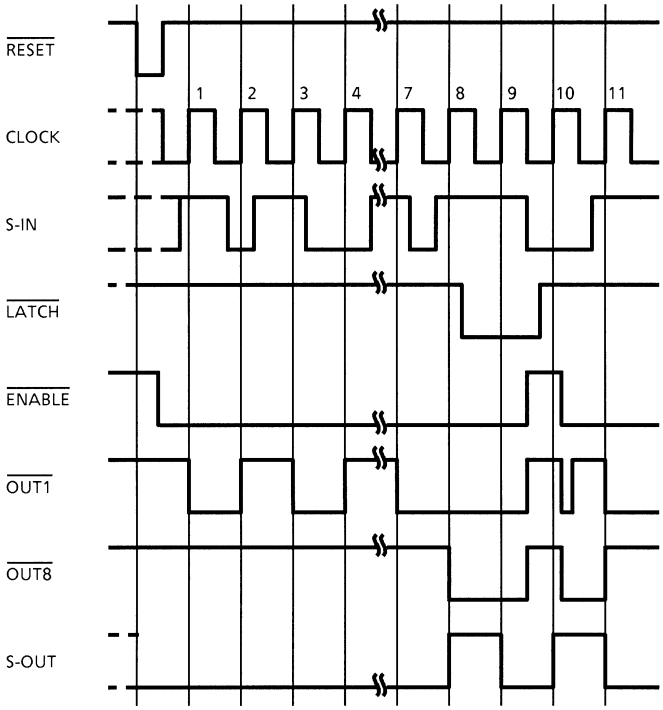
PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

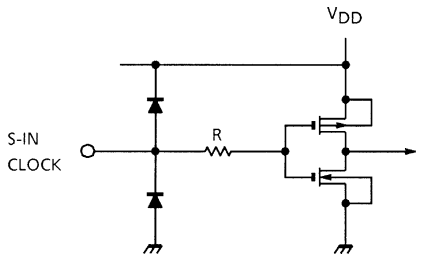


TIMING DIAGRAM

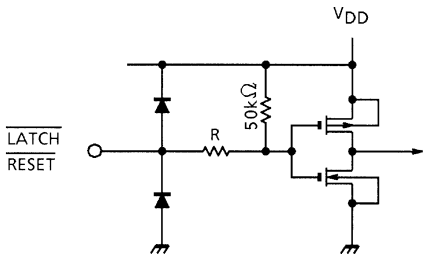


EQUIVALENT OF INPUTS AND OUTPUTS

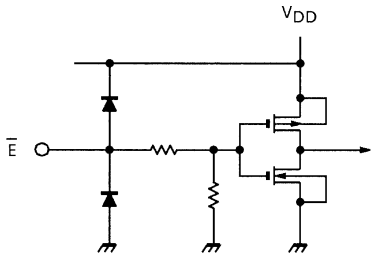
S−IN, clock terminal equivalent circuits



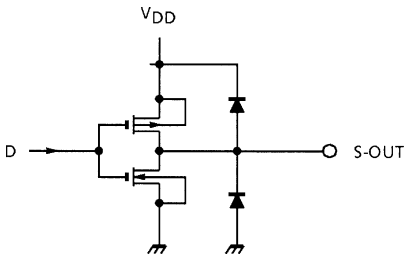
$\overline{\text{LATCH}}$, $\overline{\text{RESET}}$ terminal equivalent circuits



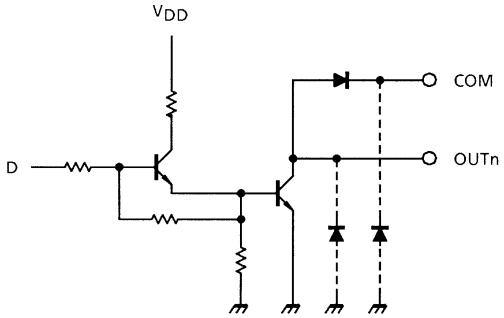
$\overline{\text{ENABLE}}$ terminal equivalent circuits



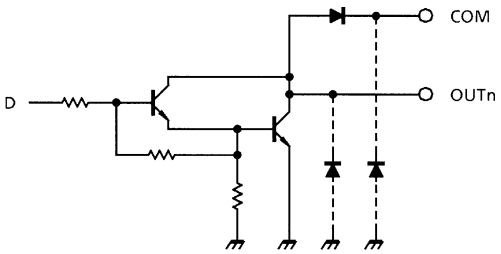
S−OUT terminal equivalent circuits



Output terminal equivalent circuits (TD62C851P)



Output terminal equivalent circuits (TD62C852P)



Note: The output parasitic diode cannot be used as clamp diode.

TRUTH TABLE

CK	$\overline{E}$	$\overline{R}$	$\overline{LATCH}$	S−IN	OUT		S−OUT
					$\overline{O1}$	$\overline{On}$	
↑	L	H	H	L	OFF	$\overline{On-1}$	Q_7
↑	L	H	H	H	ON	$\overline{On-1}$	Q_7
↑	L	H	L	(*)	NC	NC	Q_7
↑	H	H	(*)	(*)	OFF	NC	Q_7
↓	(*)	(*)	(*)	(*)	NC	NC	Q_7
(*)	(*)	L	H	(*)	OFF	OFF	L
(*)	H	⊓	L	(*)	NC	NC	L

CK = CLOCK
$\overline{E}$ = ENABLE
$\overline{R}$ = RESET
LATCH = LATCH
S−IN = SERIAL IN
OUT = PARALLEL OUT
S−OUT = SERIAL OUT

(*) = DON'T CARE
NC = NO CHANGE
L = LOW LEVEL
H = HIGH LEVEL

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	−0.3~7.0	V
Output Sustaining Voltage		$V_{CE\ (SUS)}$	−0.5~50	V
Output Current	TD62C851P	I_{OUT}	200	mA / ch
	TD62C852P		500	
Input Voltage		V_{IN}	~0.4~V_{DD} + 0.3	V
Power Dissipation		P_D	1.47	W
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C)

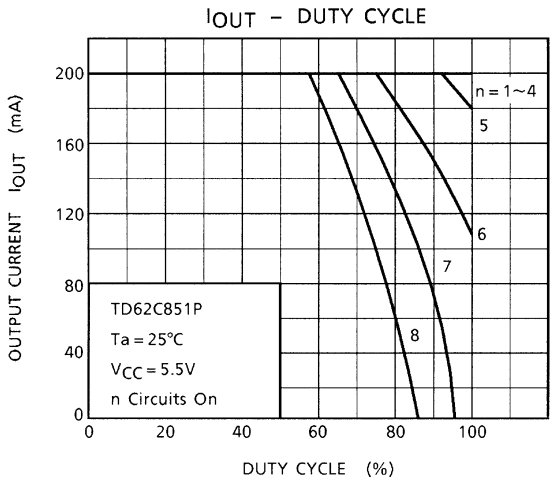
CHARACTERISTIC			SYMBOL	CONDITION		MIN	TYP.	MAX	UNIT
Supply Voltage			V_{DD}	—		4.5	5.0	5.5	V
Input Voltage			V_{IN}	—		0	—	V_{DD}	V
Output Current (“H” Level)		S−OUT	I_{OH}	Ta = 25°C		—	—	−0.4	mA
Output Voltage (“L” Level)		$\overline{On}$	V_{OH}	—		0	—	50	V
Output Current (“L” Level)		S−OUT	I_{OL}	—		—	—	0.4	mA / ch
	TD62C851P	$\overline{On}$		DC 1 circuit, Ta = 25°C		0	—	160	
				8 circuit on T_{pw} = 25 ms Ta = 85°C V_{DD} = 5.5 V	Duty = 10%	0	—	160	
					Duty = 40%	0	—	95	
	TD62C852P			D C 1 circuit, Ta = 25°C		0	—	400	
				8 circuit on T_{pw} = 25 ms Ta = 85°C V_{DD} = 5.5 V	Duty = 10%	0	—	400	
					Duty = 50%	0	—	170	
Clock Frequency			f_{CLOCK}	—		1.5	—	—	MHz
Clock Pulse Width			$f_{w\ CLOCK}$	—		0.33	—	—	μs
Data Set Up Time			t_{setup}	—		100	—	—	ns
Data Hold Time			t_{hold}	—		100	—	—	ns
Clamp Diode Reverse Voltage			V_R	—		0	—	50	V
Clamp Diode Forward Current		TD62C851P	I_F	—		0	—	160	mA
		TD62C852P		—		0	—	400	

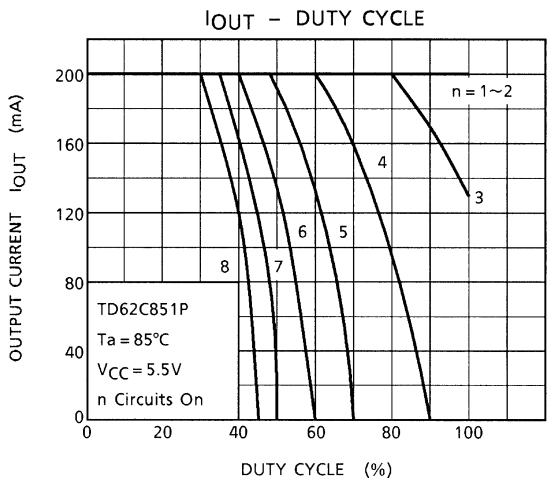
ELECTRICAL CHARACTERISTICS (Ta = −40~85°C)

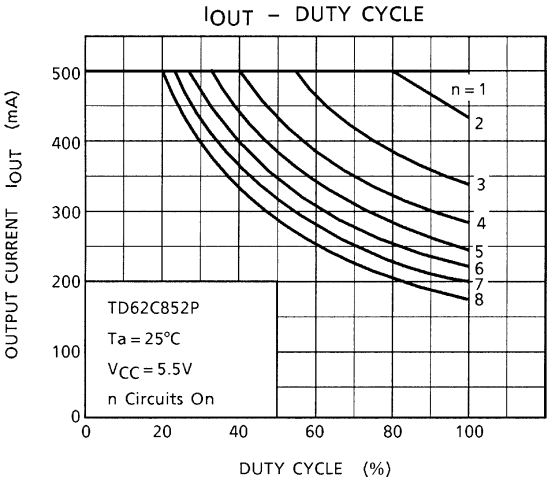
CHARACTERISTIC				SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage		“H” Level		V_{IH}	—	—		0.7 V_{DD}	—	—	V
		“L” Level		V_{IL}	—	—		—	—	0.3 V_{DD}	
Input Current		“H” Level		I_{IH}	—	ENABLE, V_{DD} = 5.5 V V_{IH} = V_{DD}		28	55	110	µA
		“L” Level		I_{IL}	—	LATCH, RESET V_{DD} = 5.5 V, V_{IL} = GND		−55	−110	−275	
				I_{IN}	—	CLOCK, S−IN V_{IN} = V_{CC} or GND		—	—	±1.0	
Output Voltage	“H” Level	S−OUT		V_{OH}	—	V_{DD} = 4.5 V I_{OH} = −10 µA		3.9	4.1	—	V
	“L” Level	S−OUT		V_{OL}	—	V_{DD} = 4.5 V	I_{OL} = 0.8 mA	—	0.2	0.4	V
		$\overline{On}$	TD62C 851P				I_{OL} = 100 mA	—	0.29	0.50	
							I_{OL} = 160 mA	—	0.39	0.65	
			TD62C 852P				I_{OL} = 250 mA	—	1.24	1.90	
							I_{OL} = 400 mA	—	1.54	2.30	
Output Current	“H” Level	$\overline{On}$		I_{OH}	—	V_{DD} = 5.5 V, V_{OH} = 50.0 V		—	—	100	µA
Operating Supply Current				I_{DD1}	—	V_{DD} = 5.5 V Ta = 25°C	ENABLE = “H”	—	130	200	mA
				I_{DD2}			f_{CLK} = 1 MHz Output open DATA = 1 / 2 f_{CLK}	—	2.0	5.0	
		TD62C851P		I_{DD3}			1 circuit on f_{CLK} = 1 MHz ENABLE = “L”	—	35	40	
		TD62C851P						—	1.0	1.5	
Clamp Diode Reverse Current				I_R	—	V_R = 50 V		—	—	50	µA
Clamp Diode Froward Voltage		TD62C851P		V_F	—	I_F = 160 mA		—	1.0	2.0	V
		TD62C852P				I_F = 400 mA		—	1.5	2.0	

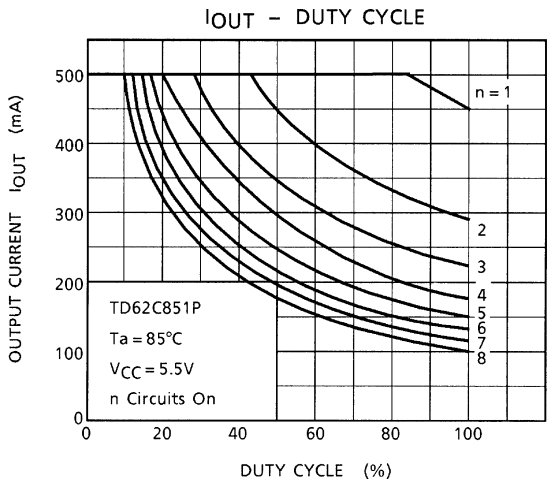
SWITCHING CHARACTERISTICS (Ta = 25°C)

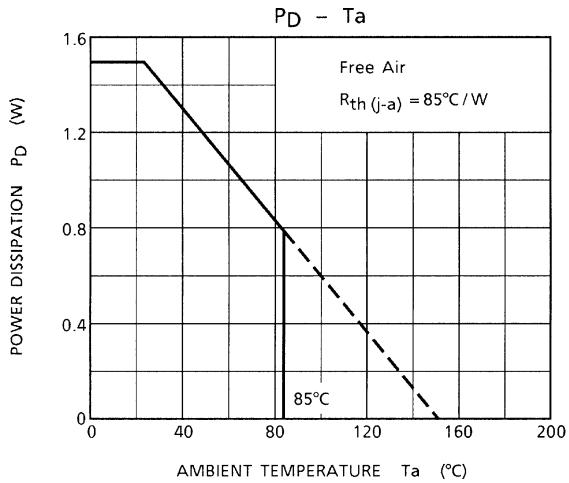
CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time	Low-to-High	CK-S-OUT	t_{pLH}	—	V_{DD} = 5.0 V, V_{IH} = 5.0 V V_{IL} = 0 V, Duty = 50% R_L = 300 Ω (TD62C851P) / 120 Ω (TD62C852P)	—	0.40	0.65	μs
		CK-$\overline{On}$				—	1.80	3.00	
		L-$\overline{On}$				—	2.10	3.50	
		R-$\overline{On}$				—	1.50	2.50	
		E-$\overline{On}$				—	1.50	2.50	
	High-to-Low	CK-S-OUT	t_{pHL}	—		—	0.33	0.55	
		CK-$\overline{On}$				—	0.41	0.70	
		L-$\overline{On}$				—	0.30	0.50	
		R-S-OUT				—	0.25	0.42	
		E-$\overline{On}$				—	0.21	0.35	
Maximum Clock Frequency			f_{MAX}	—		1.5	2.0	—	MHz
Minimum Pulse Width		CLOCK	t_{wCK}	—		—	250	330	ns
		$\overline{LATCH}$	t_{wL}			—	116	160	
		$\overline{RESET}$	t_{wR}			—	107	140	
Data Set Up Time			t_{setup}	—		—	30	60	ns
Data Hold Time			t_{hold}			—	14	40	
Maximum Clock Rise Time			t_r	—		—	70	—	ns
Maximum Clock Fall Time			t_f			—	70	—	

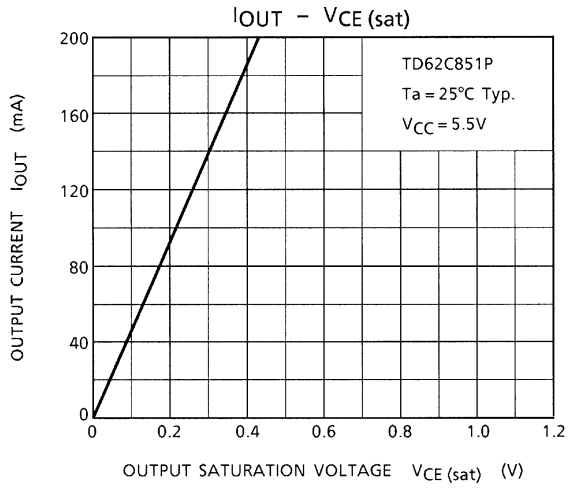

IOUT – DUTY CYCLE
OUTPUT CURRENT IOUT (mA)
DUTY CYCLE (%)
n = 1~4
5
6
7
8
TD62C851P
Ta = 25°C
VCC = 5.5V
n Circuits On

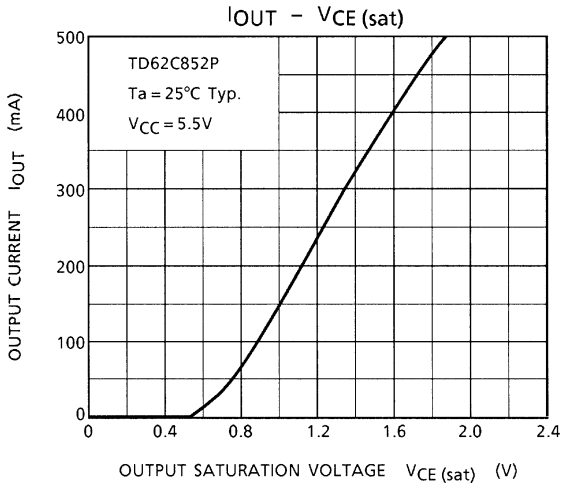

IOUT – DUTY CYCLE
OUTPUT CURRENT IOUT (mA)
DUTY CYCLE (%)
n = 1~2
3
4
5
6
7
8
TD62C851P
Ta = 85°C
VCC = 5.5V
n Circuits On

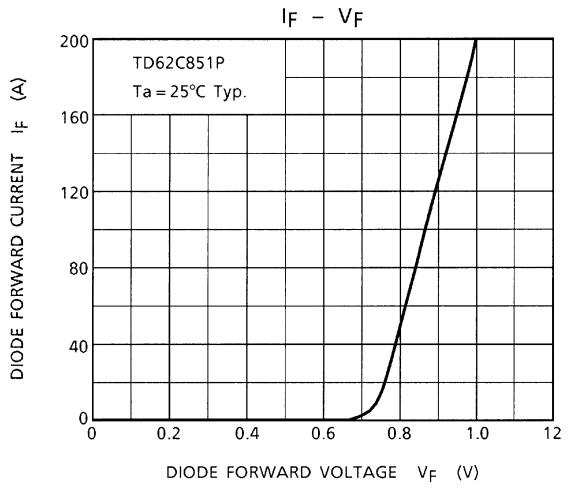

IOUT – DUTY CYCLE
OUTPUT CURRENT IOUT (mA)
DUTY CYCLE (%)
n = 1
2
3
4
5
6
7
8
TD62C852P
Ta = 25°C
VCC = 5.5V
n Circuits On

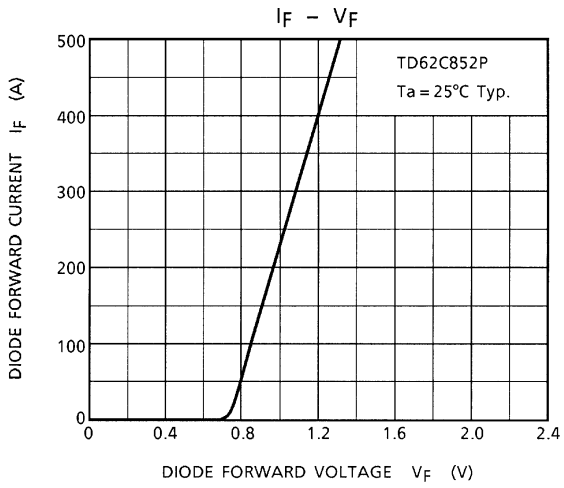

IOUT – DUTY CYCLE
OUTPUT CURRENT IOUT (mA)
DUTY CYCLE (%)
n = 1
2
3
4
5
6
7
8
TD62C851P
Ta = 85°C
VCC = 5.5V
n Circuits On


PD – Ta
POWER DISSIPATION PD (W)
AMBIENT TEMPERATURE Ta (°C)
Free Air
Rth (j-a) = 85°C / W
85°C







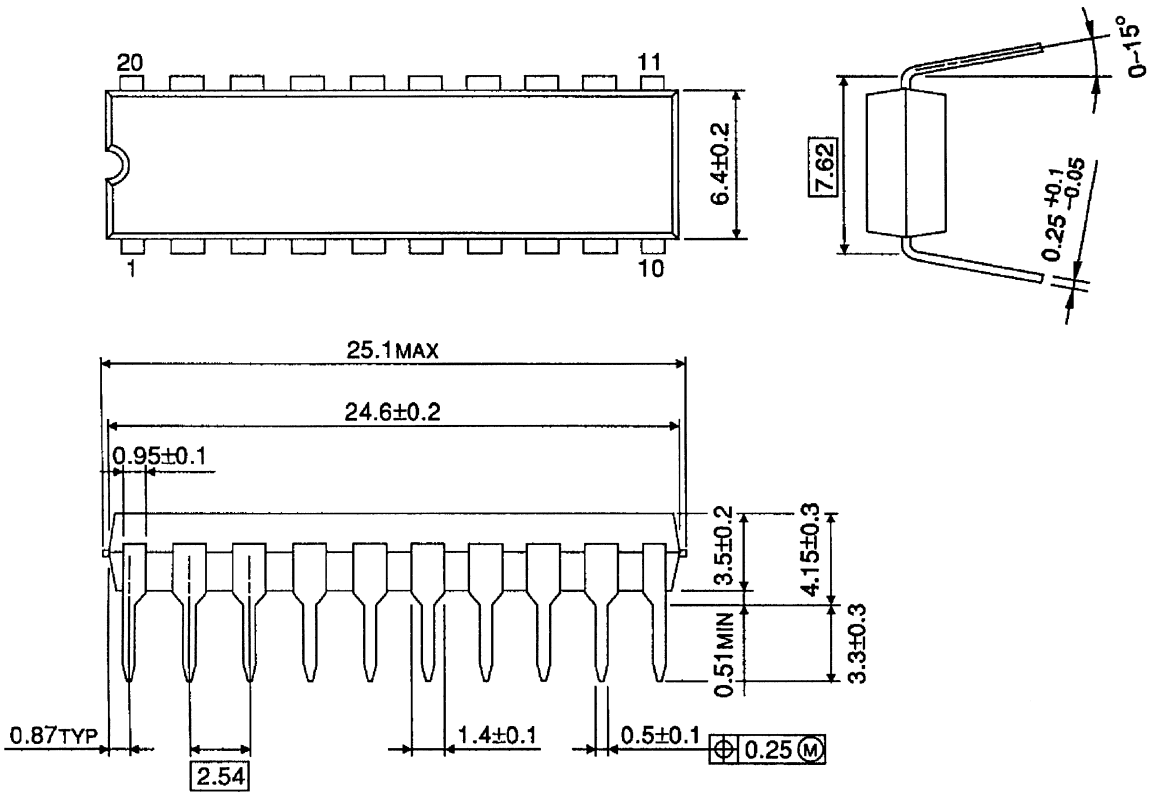


PRECAUTIONS FOR USING

This IC does not integrate protection circuits such as overcurrent and overvoltage protectors.
Thus, if excess current or voltage is applied to the IC, the IC may be damaged. Please design the IC so that excess current or voltage will not be applied to the IC.
Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short−circuit between outputs, air contamination fault, or fault by improper grounding.

PACKAGE DIMENSIONS

DIP20−P−300−2.54A Unit: mm



Weight: 2.25 g (Typ.)

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000707EBA

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