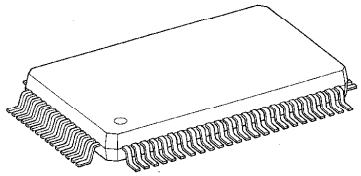
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62C805F

48BIT THERMAL HEAD DRIVER

The TD62805F is a general purpose 48bit driver IC consisting of 8 block 8bit shift register and 48bit drivers (Open Drain).
This device is best suited as a 48 dot thermal printer head drivers.



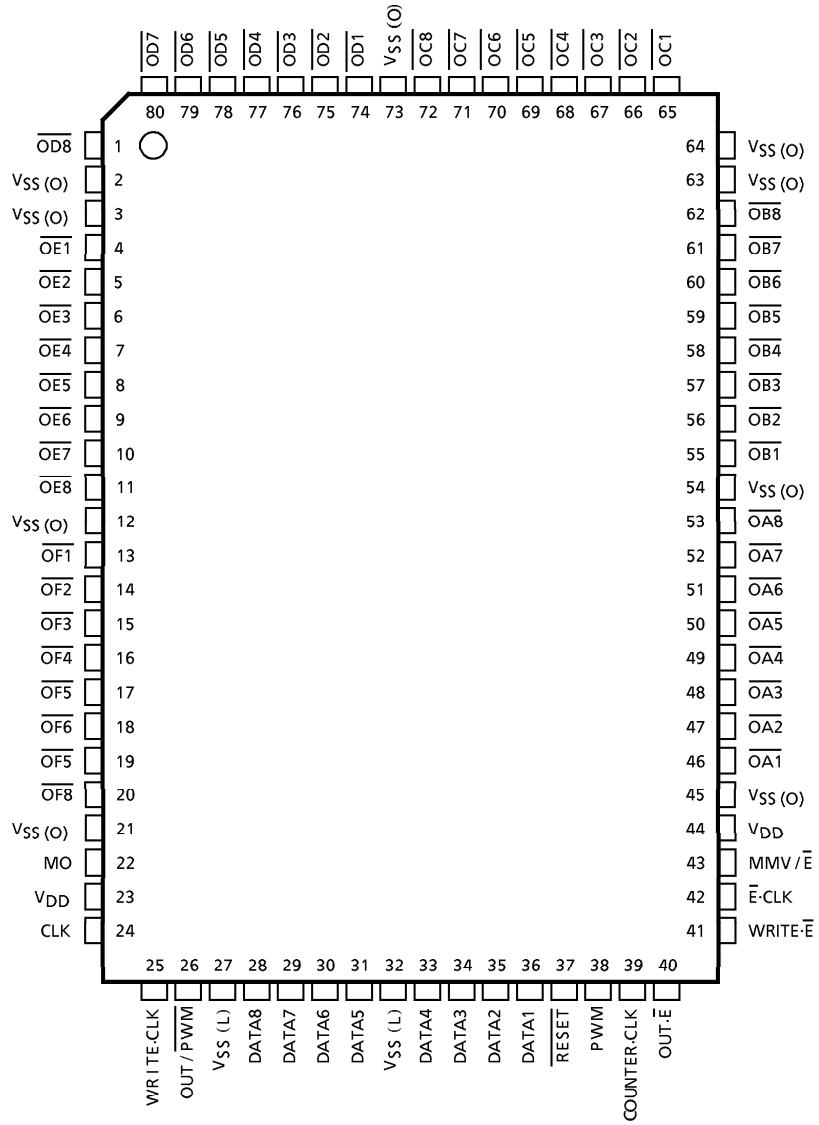
QFP80-P-1420-0.80C

Weight : 1.53g (Typ.)

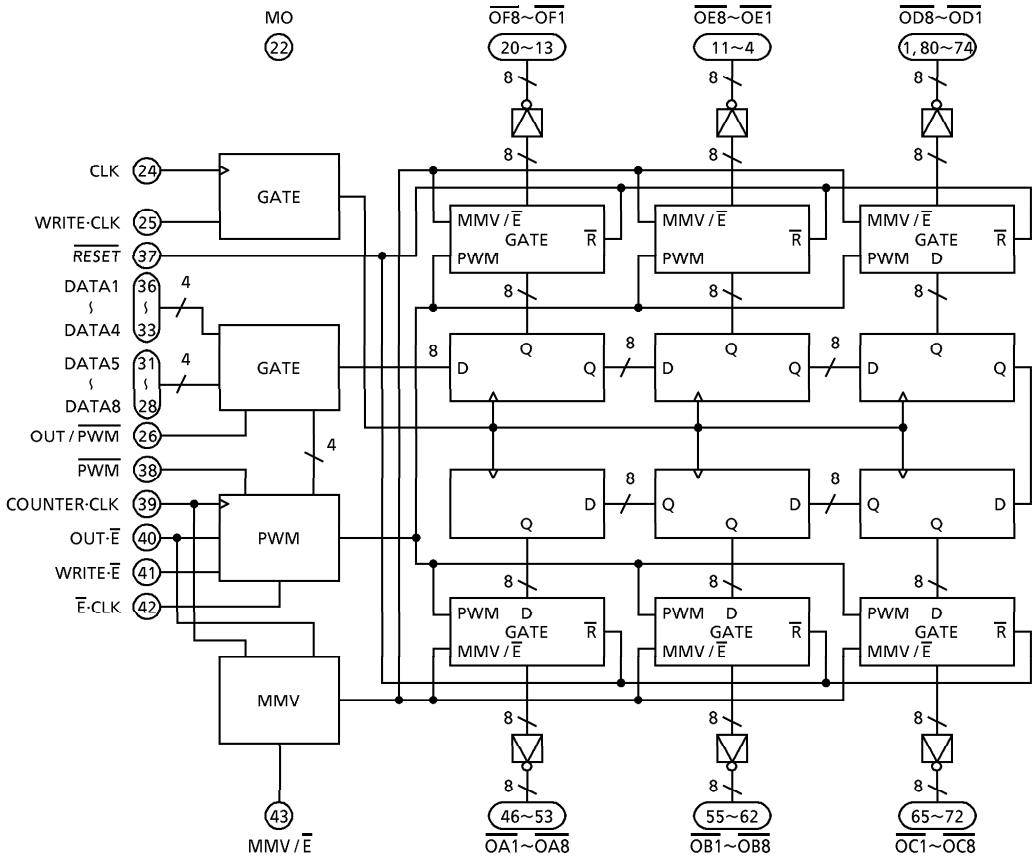
FEATURES

- 8bit parallel input and 6 block 8bit shift register
- CMOS compatible input.
- High driverability ... 30V / 100mA / ch
- Built in monostable multivibrator for head protection
- 16 steps gray scale operating with 4bit data
- 48bit open drain outputs
- Package μPFP-80PIN

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

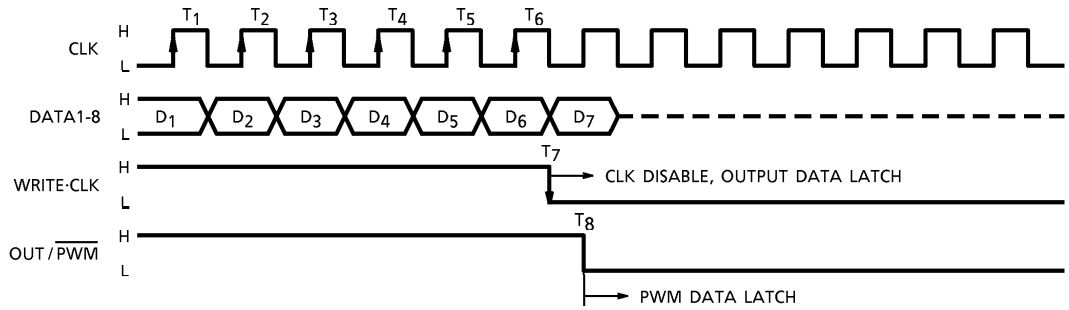


PIN FUNCTION

PIN No.	PIN NAME	FUNCTION
24	CLK	" ⌋ " : Data shift
25	WRITE·CLK	"H" : enable clock signal, "L" : disable clock signal pull-up input terminal
37	$\overline{\text{RESET}}$	"L" : all outputs "OFF", reset PWM counter reset PWM counter and MMV circuit Pull-up input terminal
28~36	DATA1~8	Input terminals for output data "H" : output "ON", "L" : output "OFF" And input terminals for PWM data
26	OUT / $\overline{\text{PWM}}$	"H" : enable output data for shift register "L" : enable PWM data for counter
38	$\overline{\text{PWM}}$	"L" : output enable (PWM operating)
39	COUNTER·CLOCK	Input terminal for clock of PWM counter and for trigger of MMV
40	OUT·$\overline{\text{E}}$	"L" : all outputs "ON"
42	$\overline{\text{E}}$·CLK	" ⌊ " : outputs "OFF" when OUT·E is "High". Outputs "ON" when OUT·E is "Low". Pull-up input terminal
41	WRITE·$\overline{\text{E}}$	"H" : enable E-CLK signal pull-up input terminal
43	MMV / E	CR connection terminal for MMV
22	MO	ON / OFF monitor terminal of output $\overline{\text{OF8}}$
23, 44	V_{DD}	Supply voltage terminal for control logic
—	$V_{SS\,(O)}$	GND terminals for driver PIN No. : 2, 3, 12, 21, 45, 54, 63, 64, 73
27, 32	$V_{SS\,(L)}$	GND terminals for control logic

(1) Data Input

D_1~D_6 of Input Dates are entered to shift Register by the clock signal with the timing of rise. Outputs are latched by holding the WRITE·CLK "Low" or to stop the clock signal.
PWM Data (DATA1~4) are latched by OUT / PWM signal "Low".

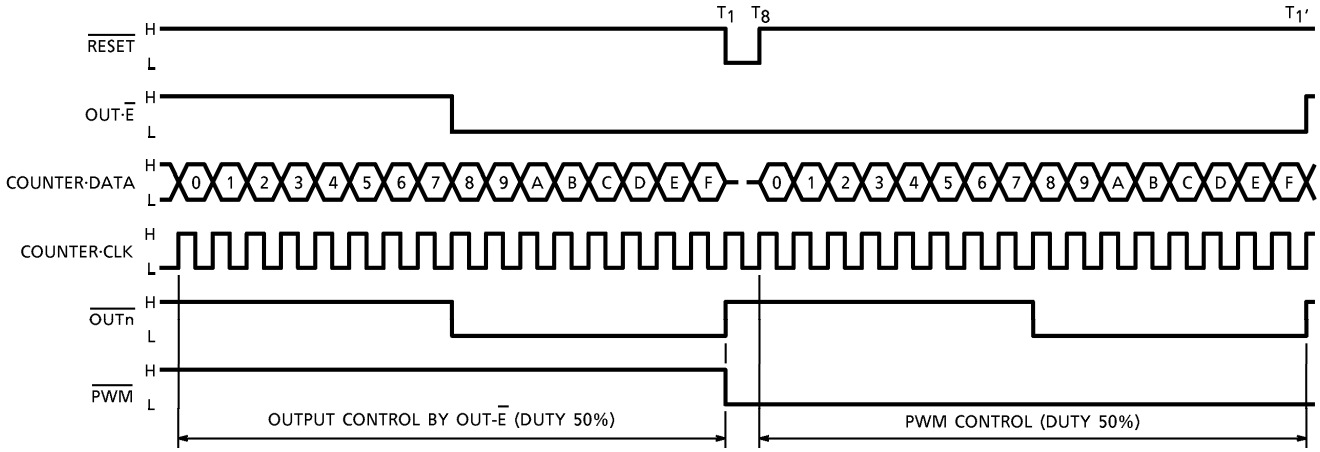


(2) Output Enable

Outputs become "OFF" at the first rising edge of E·CLK after the OUT·E to "High", and become "ON" at the first rising edge of E·CLK after the OUT·E to "Low".
Output ON / OFF duty is controlled by controlling OUT·E signal directly or to change the timing of WRITE·E and E·CLK.

(3) PWM Control

Outputs ON / OFF duty are controlled by OUT·$\overline{E}$ and PWM DATA of D_1~D_4 PWM control is performed by comparing the internal 4bit PWM Counter out and PWM DATA of D_1~D_4.
For example, when PWM DATA is 7, 50% Output Duty is obtained.
(Refer to tables below.)

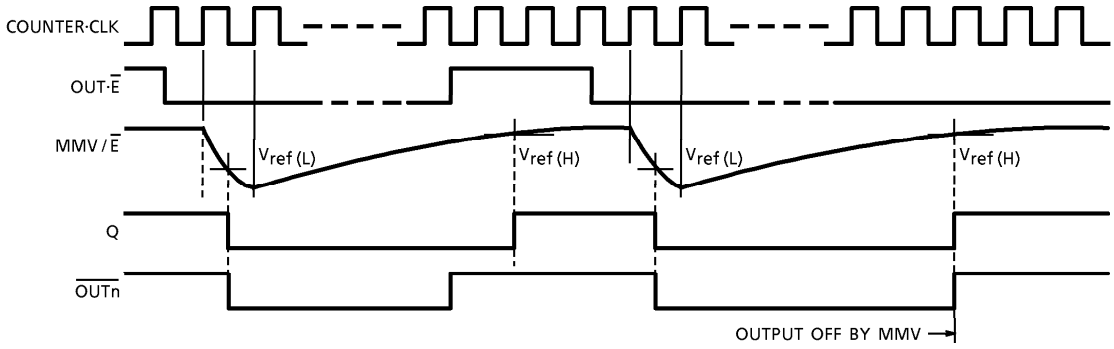


PWM DATA	0	1	2	3	4	5	6	7	8	9
Duty (%)	0	6.25	12.50	18.75	25.00	31.25	37.50	43.75	50.00	56.25

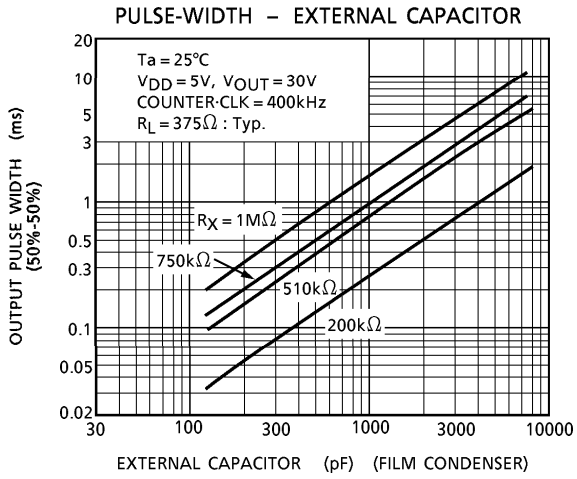
PWM DATA	A	B	C	D	E	F
Duty (%)	62.50	68.75	75.00	81.25	87.50	100.00

MMV OPERATION

MMV output of Q becomes "L" when the MMV / E voltage becomes less than $V_{ref\,(L)}$ after the first rising edge of INTERNAL CLOCK.
And becomes "H" when the MMV / E voltage above $V_{ref\,(H)}$ after re-charging of external capacitance connect to MMV / E. The external capacitance and Resistor connect to MMV / E control MMV Output "ON" period.
So Output Load is protected from burn-out. It's required enough discharging time of external capacitance. (Refer to figure below)

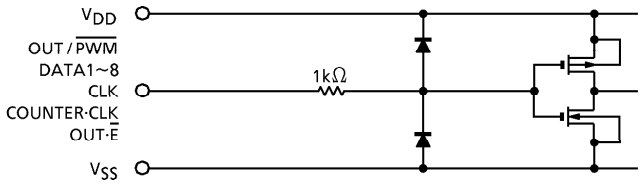


- Pulse width of MMV

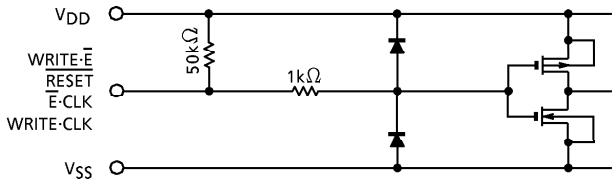


INPUT CIRCUIT

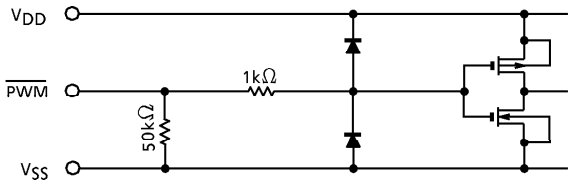
1. DATA1~8, CLK, COUNTER·CLK, OUT / $\overline{\text{PWM}}$, OUT·$\overline{\text{E}}$



2. $\overline{\text{E}}$·CLK, $\overline{\text{RESET}}$, WRITE·$\overline{\text{E}}$, WRITE·CLK

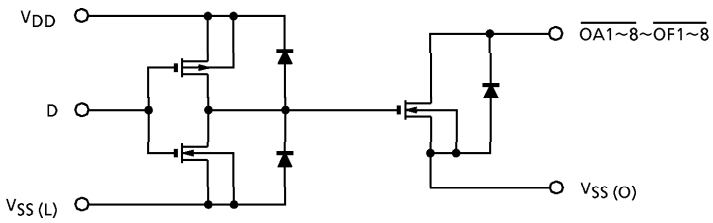


3. $\overline{\text{PWM}}$



OUTPUT CIRCUIT

1. $\overline{\text{OA1~8}}$~$\overline{\text{OF1~8}}$



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	7	V
Output Voltage		V_{DS}	30	V
Output Current		I_{DS}	100	mA / ch
Input Current		I_{IN}	± 5	mA
Input Voltage		V_{IN}	− 0.4~V_{DD} ± 0.4	V
Power Dissipation	Free Air	P_D	1.0	W
	On PCB (Note)		1.3	
Operating Temperature		T_{opr}	− 40~85	°C
Storage Temperature		T_{stg}	− 55~150	°C

(Note) On Glass Epoxy PCB (100 × 100 × 1.6mm, Cu 40%)

RECOMMENDED OPERATING CONDITIONS (Ta = − 40~85°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{DS}	—	—	—	26	V
Supply Voltage	V_{DD}	—	4.5	—	5.5	V
Output Current	I_{DS}	Duty 50%	—	—	33.3	mA / ch
		Duty 80%	—	—	26.4	
		Duty 100%	—	—	23.6	
Input Voltage	V_{IN}	—	GND	—	V_{DD}	V
Operating Clock Frequency	f_{CLK}	Duty 50%	—	—	5	MHz
Clock Pulse Width	t_w	COUNTER·CLK	50	—	—	ns
		CLK				
Data Set-Up Time	t_{setup}	—	20	—	—	ns
Data Hold Time	t_{hold}					

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 5.5V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—	—		3.5	—	V_{DD} + 0.4	V
	"L" Level	V_{IL}	—	—		− 0.4	—	1.5	
Input Current	WRITE·CLK $\overline{E}$·CLK, $\overline{RESET}$ WRITE·$\overline{E}$	I_{INH}	—	V_{IN} = 0V, V_{DD} = 5V		− 34	− 70	− 145	μA
	$\overline{PWM}$	I_{INL}	—	V_{IN} = 5V, V_{DD} = 5V		34	70	145	
Output Voltage		V_{DS}	—	OA1~OF8	I_{DS} = 80mA	—	—	960	mV
					I_{DS} = 50mA	—	—	600	
Output On Resistor		R_{ON}	—	I_{DS} = 50mA		—	—	12.0	Ω
Output Leak Current		I_{OZ}	—	V_{DS} = 30V		—	—	10	μA
Quiescent Current		I_{DD}	—	—		—	—	20	μA
Operating Supply Current		I_{DDopr}	—	V_{DD} = 5V, f_{CLK} = 5MHz Output OPEN		—	—	5	μA

SWITCHING CHARACTERISTICS (V_{DD} = 5.5V, V_{DS} = 26V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Operating Clock Frequency		f_{MAX}	Duty 50%	10	—	—	MHz
Propagation Delay Time "L"-"H"	CLK-$\overline{OUTn}$, WRITE·CLK-$\overline{OUTn}$	t_{pLH}	Duty 50% $V_{IN\,(H)}$ = 4.5V $V_{IN\,(L)}$ = 0V R_L = 375Ω C_L = 15pF	—	80	—	ns
	$\overline{RESET}$-$\overline{OUTn}$			—	100	—	
	COUNTER, CLK-OUTn (Note)			—	110	—	
	OUT·$\overline{E}$-$\overline{OUTn}$, WRITE·$\overline{E}$-$\overline{OUTn}$ $\overline{E}$·CLK-$\overline{OUTn}$			—	100	—	
	MMV / $\overline{E}$-$\overline{OUTn}$			—	130	—	
Propagation Delay Time "H"-"L"	CLK-$\overline{OUTn}$, WRITE·CLK-$\overline{OUTn}$	t_{pHL}		—	60	—	
	$\overline{RESET}$-$\overline{OUTn}$			—	100	—	
	COUNTER, CLK-OUTn (Note)			—	90	—	
	OUT·$\overline{E}$-$\overline{OUTn}$, WRITE·$\overline{E}$-$\overline{OUTn}$ $\overline{E}$·CLK-$\overline{OUTn}$			—	70	—	
	MMV / $\overline{E}$-$\overline{OUTn}$			—	80	—	
Minimum Clock Pulse Width		t_w		25		—	
Data Set Up Time	DATA-OUT / $\overline{PWM}$	t_{setup}	—	—	10	—	
	DATA-CLK						
	OUT·$\overline{E}$-$\overline{E}$·CLK						
Data Hold Time	DATA-OUT / $\overline{PWM}$	t_{hold}	—	—	10	—	
	DATA-CLK						
	OUT·$\overline{E}$-$\overline{E}$·CLK						
Maximum Rise Time	COUNTER·CLK	t_r	—	—	—	1	μs
	CLK						
Maximum Fall Time	COUNTER·CLK	t_f	—	—	—	1	
	CLK						
Output Rise Time	$\overline{OUTn}$	t_{or}	—	—	0.02	1	
Output Fall Time		t_{of}	—	—	0.05	0.4	
MMV Pulse Width		t_{MMV}	—	—	3	—	ms

(Note) COUNTER DATA = F

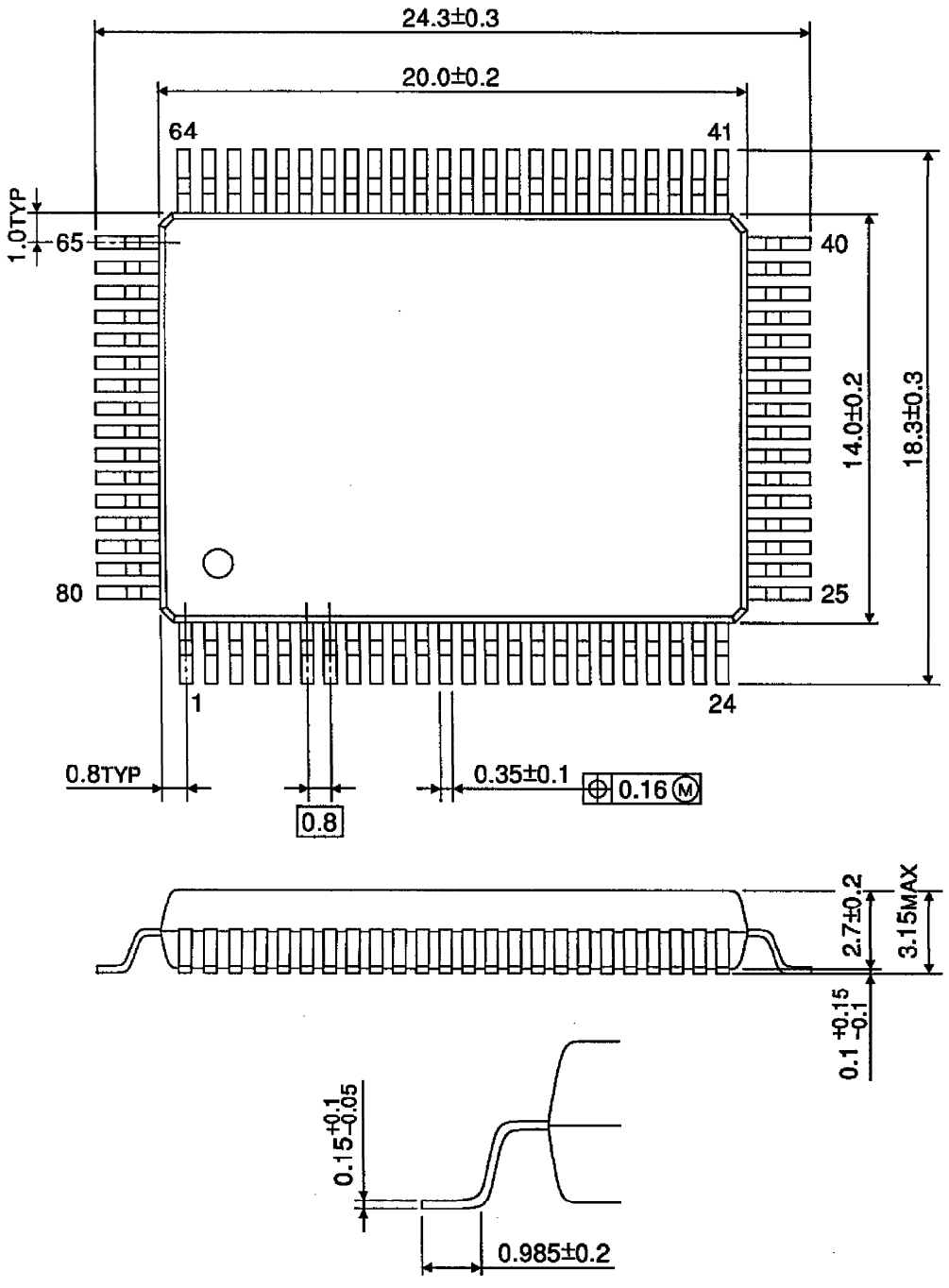
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

QFP80-P-1420-0.80C

Unit : mm



Weight : 1.53g (Typ.)