TOSHIBA Silicon Monolithic
Bi-Polor Digital Integrated Circuit

TD62C851P
TD62C852P

8 Bit Serial-In Parallel-Out Shift Register/Latch Drivers

TD62C851P
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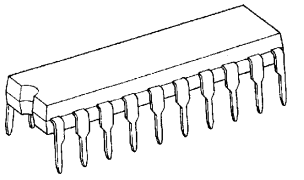

Weight DIP20-P-300A: 2.25g (Typ.)

Product Description:

These products are monolithic circuits designed to be used together with Bi-CMOS integrated circuits. The devices consist of an 8 bit shift register, 8 bit latches, and 8 output circuits (integral clamp diodes for switching inductive loads).

Features:

- 8 bit serial-in parallel-out shift register / latch driver (Bi-CMOS process)
- Output current:
  TD62C851P - 200mA / ch (Low saturation type)
  TD62C852P - 500mA / ch (Darlington type)
- Sustaining voltage output: 50V
- Built in output clamp diodes
- CMOS compatible inputs
- Package: DIP20-P-300A

MAXIMUM RATINGS (Ta = 25°C unless otherwise noted.)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	7	V
Output Sustaining Voltage		$V_{CE(SUS)}$	−0.5~50	V
Output Current	TD62C851P	I_{OUT}	200	mA / ch
	TD62C852P		500	
Input Voltage		V_{IN}	0.4~V_{DD} + 0.3	V
Power Dissipation		P_D	1.47	W
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C

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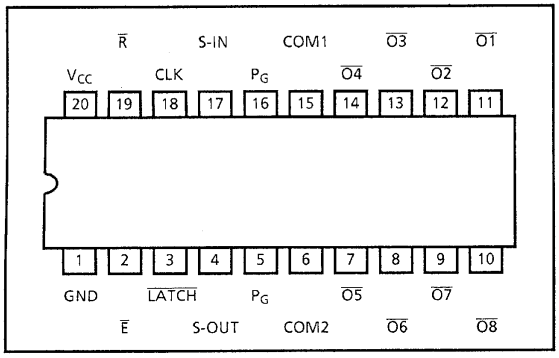
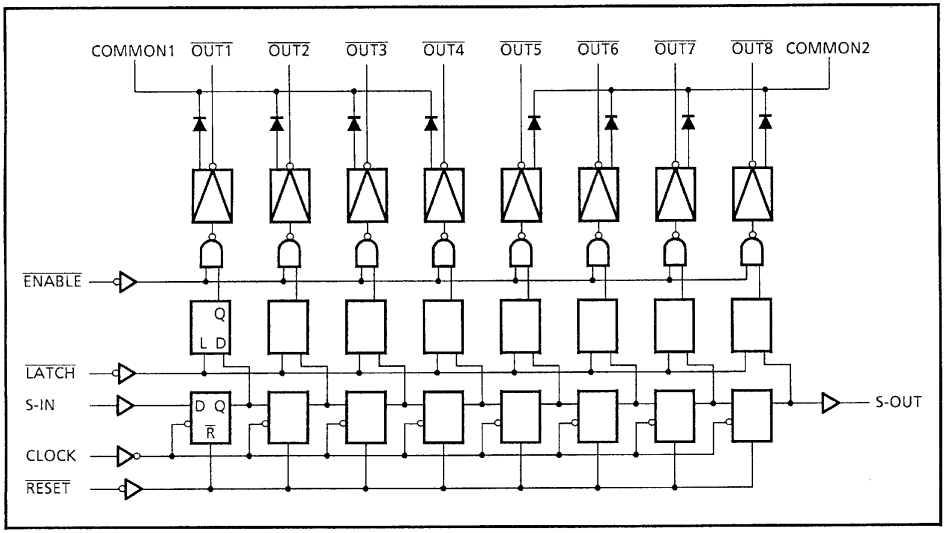
PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



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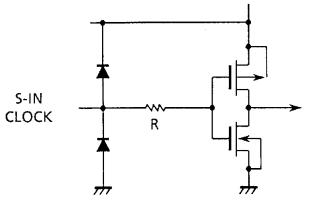
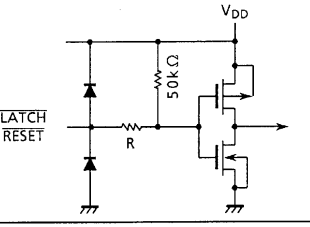
EQUIVALENT OF INPUTS AND OUTPUTS

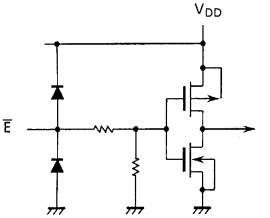
S-IN, CLOCK TERMINAL EQUIVALENT CIRCUITS



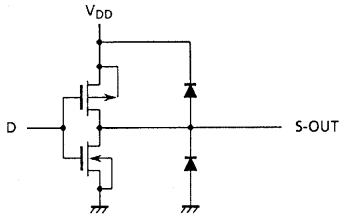
$\overline{LATCH}$, $\overline{RESET}$ TERMINAL EQUIVALENT CIRCUITS



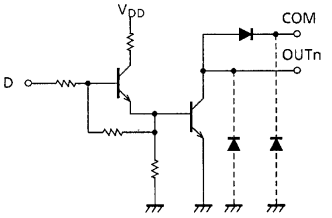
$\overline{ENABLE}$ TERMINAL EQUIVALENT CIRCUITS



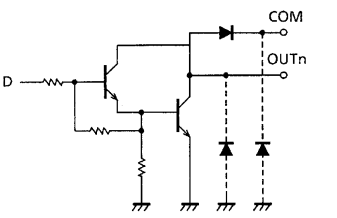
S-OUT TERMINAL EQUIVALENT CIRCUITS



OUTPUT TERMINAL EQUIVALENT CIRCUITS
(TD62C851P)



OUTPUT TERMINAL EQUIVALENT CIRCUITS
(TD62C852P)



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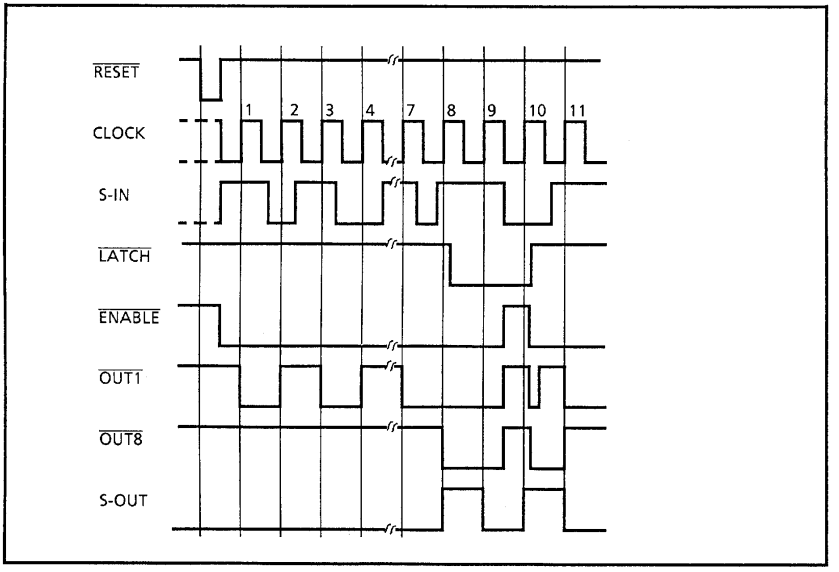
TRUTH TABLE

CK	$\overline{E}$	$\overline{R}$	$\overline{LATCH}$	S-IN	OUT		S-OUT
					$\overline{O1}$	$\overline{On}$	
∫	L	H	H	L	OFF	$\overline{On-1}$	Q7
∫	L	H	H	H	ON	$\overline{On-1}$	Q7
∫	L	H	L	*	NC	NC	Q7
∫	H	H	*	*	OFF	OFF	Q7
∫	*	*	*	*	NC	NC	Q7
*	*	L	H	*	OFF	OFF	L
*	L	⊓	L	*	NC	NC	L

CK=CLOCK
$\overline{E}$=$\overline{ENABLE}$
$\overline{R}$=$\overline{RESET}$
$\overline{LATCH}$=$\overline{LATCH}$
S-IN=SERIAL IN
OUT=PARALLEL OUT
S-OUT=SERIAL OUT

*=DON'T CARE
NC=NO CHANGE
L=LOW LEVEL
HIGH=LEVEL

TIMING DIAGRAM



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RECOMMENEDED OPERATING CONDITIONS (Ta = −40~85°C)

CHARACTERISTIC			SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage			V_{DD}			4.5	5.0	5.5	V
Input Voltage			V_{IN}			0	—	V_{DD}	V
Output Current ("H"LEVEL)	S-OUT		I_{OH}	Ta = 25°C		—	—	−0.4	mA
Output Voltage ("L"LEVEL)	$\overline{On}$		V_{OH}			0	—	5.0	V
Output Current ("L"LEVEL)	S-OUT		I_{OL}			—	—	0.4	mA/ch
	TD62C851P	$\overline{On}$		DC 1 CIRCUIT, Ta = 25°C		0	—	160	
				8 CIRCUIT ON, Tpw = 25ms, Ta = 85°C, V_{CC} = 5.5V	Duty = 10%	0	—	160	
					Duty = 40%	0	—	95	
	TD62C852P			DC 1 CIRCUIT, Ta = 25°C		0	—	400	
				8 CIRCUIT ON, Tpw = 25ms, Ta = 85°C, V_{DD} = 5.5V	Duty = 50%	0	—	400	
					Duty = 50%	0	—	170	
Clock Frequency			f_{CLOCK}			1.5	—	—	MHz
Clock Plus Width			$f_{W\ CLOCK}$			0.33	—	—	μs
Data Set up Time			$t_{set\ up}$			100	—	—	ns
Data Hold Time			t_{hold}			100	—	—	ns
Clamp Diode Reverse Voltage			V_R			0	—	50	V
Clamp Diode Forward Current	TD62C851P		I_F			0	—	160	mA
	TD62C852P					0	—	400	

ELECTRICAL CHARACTERISTICS (Ta = −40~85°C)

CHARACTERISTIC			SYM-BOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" LEVEL		V_{IH}	—			0.7 V_{DD}	—	—	V
	"L" LEVEL		V_{IL}	—			—	—	0.3 V_{DD}	
Input Current	"H" LEVEL		I_{IH}	—	ENABLE, V_{DD} = 5.5V, V_{IH} = V_{DD}		28	55	110	μA
	"L" LEVEL		I_{IL}	—	LATCH, RESET, V_{DD} = 5.5V, V_{IL} = GND		−55	−110	−275	
			I_{IN}	—	CLOCK, S-IN, V_{CC} or GND		—	—	±1.0	
Output Voltage ("H" LEVEL)	S-OUT		V_{OH}	—	V_{DD} = 4.5V	I_{OH} = −10μA	4.0	—	—	V
						I_{OH} = −400μA	3.9	4.1	—	
Output Current ("H" LEVEL)	$\overline{On}$		I_{OH}	—	V_{DD} = 4.5V, V_{OH} = 2.4V		—	—	100	
Output Voltage ("L" LEVEL)	S-OUT		V_{OL}	—	V_{DD} = 4.5V	I_{OL} = 8.0mA	—	0.2	0.4	V
	TD62C851P	$\overline{On}$				I_{OL} = 100mA	—	0.29	0.50	
						I_{OL} = 160mA	—	0.39	0.65	
	TD62C852P					I_{OL} = 250mA	—	1.24	1.90	
						I_{OL} = 400mA	—	1.54	2.30	
Supply Current			I_{DD1}	—	V_{DD} = 5.5V, Ta = 25°C	ENABLE = "H"	—	130	200	mA
Opereating Supply Current			I_{DD2}			f_{CLK} = 1MHz, DATA = 1/2f_{CLK}	—	2.0	5.0	
	TD62C851P		I_{DD3}			1 CIRCUIT ON	—	35	40	
	TD62C852P						—	1.0	1.5	
Clamp Diode Reverse Current			I_R	—	V_R = 50V		—	—	50	μA
Clamp Diode Forward Voltage	TD62C851P		V_F	—	I_F = 160mA		—	1.00	1.30	V
	TD62C852P				I_F = 400mA		—	1.50	2.00	

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SWITTING CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC			SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propa-gation Delay Time	Low-to-High	CK-S · OUT	t_{pLH}	—	V_{DD} = 5.5V, V_{IH} = 5.0V V_{IL} = 0V, Duty = 50% RL = 300Ω (TD62C851P) RL = 120Ω (TD62C852P)	—	0.40	0.65	µs
		CK-$\overline{On}$				—	1.80	3.00	
		L-$\overline{On}$				—	2.10	3.50	
		$\overline{R}$-$\overline{On}$				—	1.50	2.50	
		$\overline{E}$-$\overline{On}$				—	1.50	2.50	
	High-to-Low	CK-S · OUT	t_{pHL}	—		—	0.33	0.55	µs
		CK-$\overline{On}$				—	0.41	0.70	
		L-$\overline{On}$				—	0.30	0.50	
		R-S · OUT				—	0.25	0.42	
		$\overline{E}$-$\overline{On}$				—	0.21	0.35	
Maximam Clock Frequency			f_{max}	—		1.5	2.0	—	MHz
Mimimun Pulse Width		$\overline{CLOCK}$	t_{WCK}	—		—	250	330	ns
		$\overline{LATCH}$	t_{WL}	—		—	116	160	
		$\overline{RESET}$	t_{WR}	—		—	107	140	
Data Set up Time			$t_{set\ up}$	—		—	30	60	ns
Data Hold Time			t_{hold}	—		—	14	40	ns
Maximum Clock Rise Time			t_r	—		—	70	—	ns
Maximum Clock Fall Time			t_f	—		—	70	—	ns

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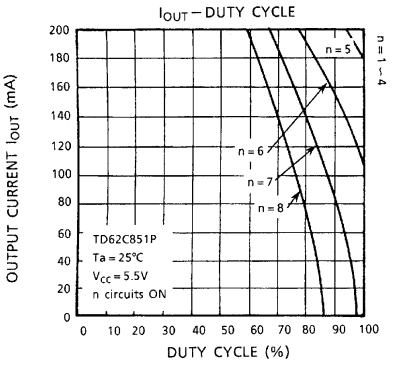

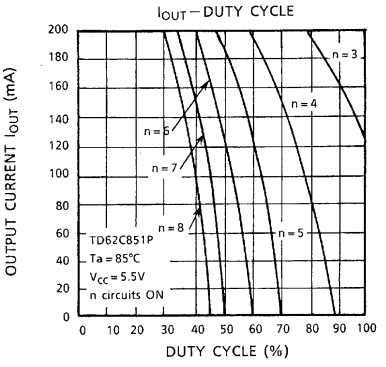

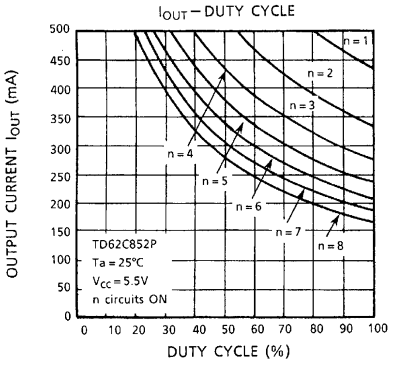

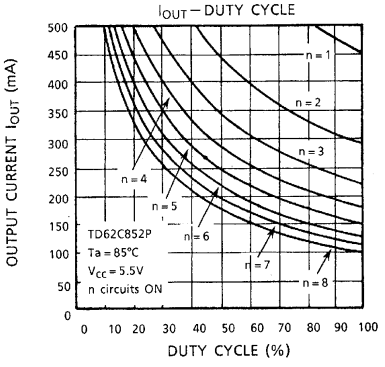

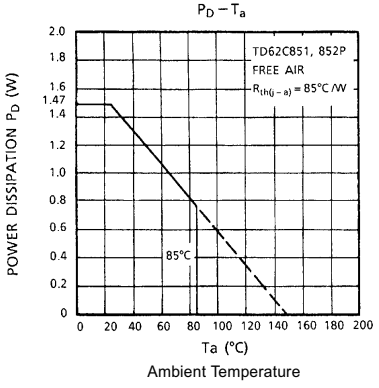

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